## **MHR Series**

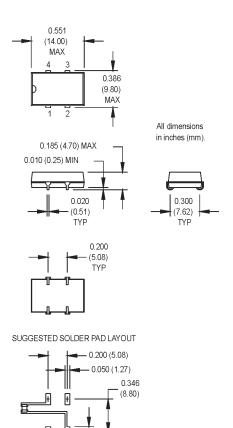
## 9x14 mm, 5.0 Volt, HCMOS/TTL, Clock Oscillator







## This product is not recommended for new designs



NOTE: A capacitor of value 0.01  $\mu\text{F}$  or greater between Vdd and Ground is recommended.

## **Pin Connections**

0.118 (3.00)

PIN	FUNCTION			
1	N/C or Tristate			
2	Gro und			
3	Output			
4	+Vdd			

	MHR	1	3	Ţ	A	J	-R	00.000 MHz
Product Series Temperature Range 1: 0°C to +70°C 6: -20°C to +70°C		 85°C						
3: ±100 ppm 6: ±25 ppm Output Type	*8: ±20 ppm		_					
F: Fixed Symmetry/Logic Con A: 40/60 TTL/HCM0 *B: 45/55 TTL *C: 45/55 TTL *C: 45/55 TTL *G: 40/60 TTL (50.00 G: 40/60 HCMOS (6)	T: Tristate n patibility —— DS (Standard for 11 to 67.000 MH;	z)		0.000	MHz)			
Package/Lead Config J: J Lead RoHS Compliance — -R: RoHS Compliant Frequency (custome	jurations———				_			

<sup>\*</sup> Consult factory regarding availability of "B" and "C" symmetry codes, and "8"

	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes		
	Frequency Range	F	1		80	MHz			
	Operating Temperature	TA	(See ordering information)						
	Storage Temperature	Ts	-55		+125	°C			
	Frequency Stability	ΔF/F	(S	(See ordering information)					
	Aging					Í			
	1st Year		-5		+5	ppm			
	Thereafter (per year)		-5		+5	ppm			
	Input Voltage	Vdd	4.5	5.0	5.5	V			
	Input Current	ldd			30	mA	1.000 to 40.000 MHz		
					50	mΑ	40.001 to 50.000 MHz		
ПS					55	mA	50.001 to 80.000 MHz		
ectrical Specifications	Output Type						HCMOS/TTL		
lca	Load						See Note 1		
ŠĊ.	1 to 50 MHz		10 TTL or 50 pF						
Š	50.001 to 67 MHz		5 TTL or 30 pF						
a	67.001 to 80 MHz			15 pF	*******************************				
ri:	Symmetry (Duty Cycle)		(See ordering information)				See Note 2		
9	Logic "1" Level	Voh	90% Vdd			V	HCMOS Load		
ū			Vdd-0.5			V	TTL Load		
	Logic "0" Level	Vol			10% Vdd	V	HCMOS Load		
					0.5	V	TTL Load		
	Output Current				±12	mA			
	Rise/Fall Time	Tr/Tf					See Note 3		
	1 to 40 MHz				10	ns			
	40.001 to 50 MHz				8	ns			
	50.001 to 80 MHz				6	ns			
	Tristate Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z						
	04-4 Ti		Input Logic	"U": outpi					
	Start up Time	D:		-	10	ms	4.0:		
	Random Jitter	Rj	<u> </u>	5	12	ps RMS	1-Sigma		
ta	Mechanical Shock MIL-STD-202, Method 213, C (100 g's)								
lel	Vibration		STD-202, Method 201 & 204 (10 g/s) from 10-2000 Hz)						
Environmental	Thermal Cycle	MIL-STD-883, Method 1010, B (-55°C to +125°C, 15							
Ş	Hermeticity		MIL-STD-865, Method 1010, B (-55°C to +125°C, 15°C to +125°C to +1				min awell, 10 cycles)		
l 🖺	Solderability		Per EIAJ-STD-002						
	Max Soldering Conditions		See solder profile, Figure 1						
	1. TTL load - see Load Circuit Diagram #1. HCMOS load - see Load Circuit Diagram #2.								
	1. TTE Toda - See Ebda Gricuit Diagrafii #1. Horivos toda - See Ebda Gricuit Diagrafii #2.								

- 2. Symmetry is measured at 1.4 V with TTL load and at 50% Vdd with HCMOS load.
- 3. Rise/Fall times are measured between 0.5 V and 2.4 V for TTL load, and between 10% and 90% Vdd for HCMOS load.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.





