P54/74FCT646/A/C (P54/74PCT646/A/C)
P54/74FCT648/A/C (P54/74PCT648/A/C)
OCTAL TRANSCEIVER/REGISTER

FEATURES

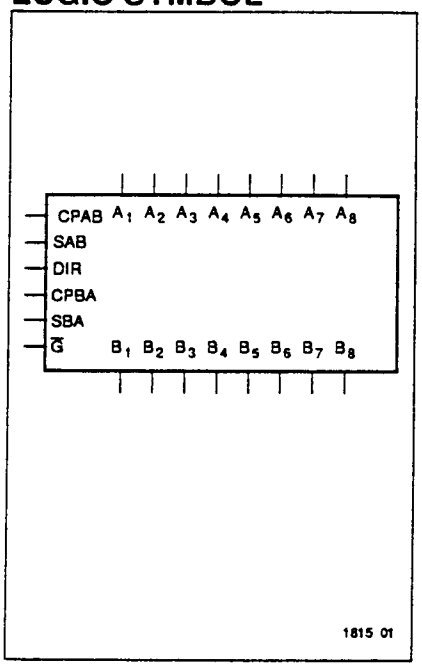
- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-C speed at 5.4ns max. (Com'l)
  FCT-A speed at 6.3ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'l), 48 mA (Mil)
  15 mA Source Current (Com'l), 12 mA (Mil)
- Independent Register for A and B Buses
- Choice of Non-Inverting and Inverting Data Paths
- Multiplexed Real-Time and Stored Data
- 3-State Output
- Manufactured in 0.8 micron PACE Technology™

DESCRIPTION

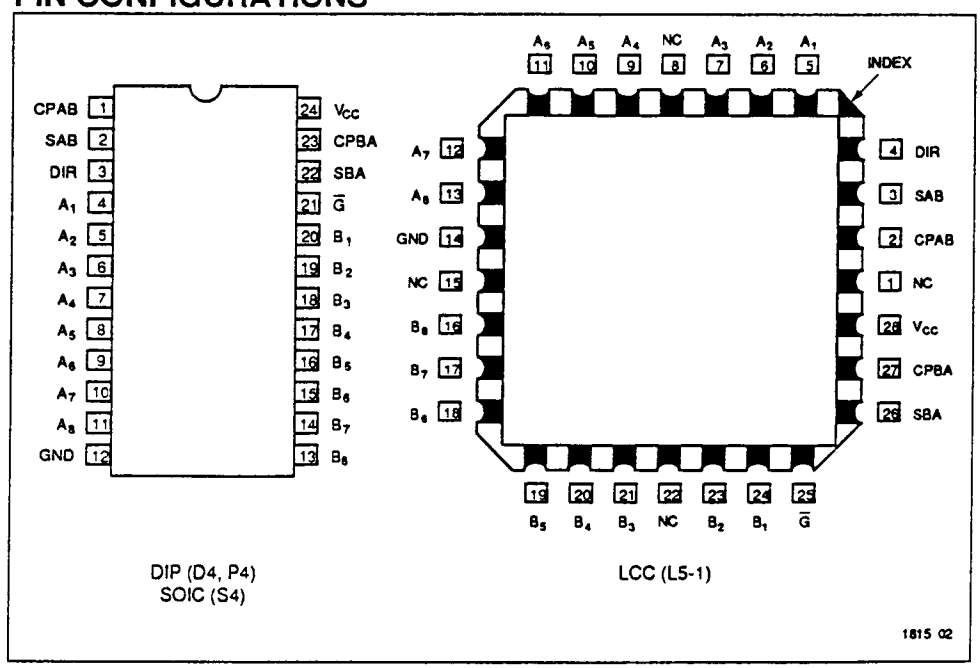
The 'FCT646 and 'FCT648 consist of a bus tranceiver circuit with 3-state, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function.

In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

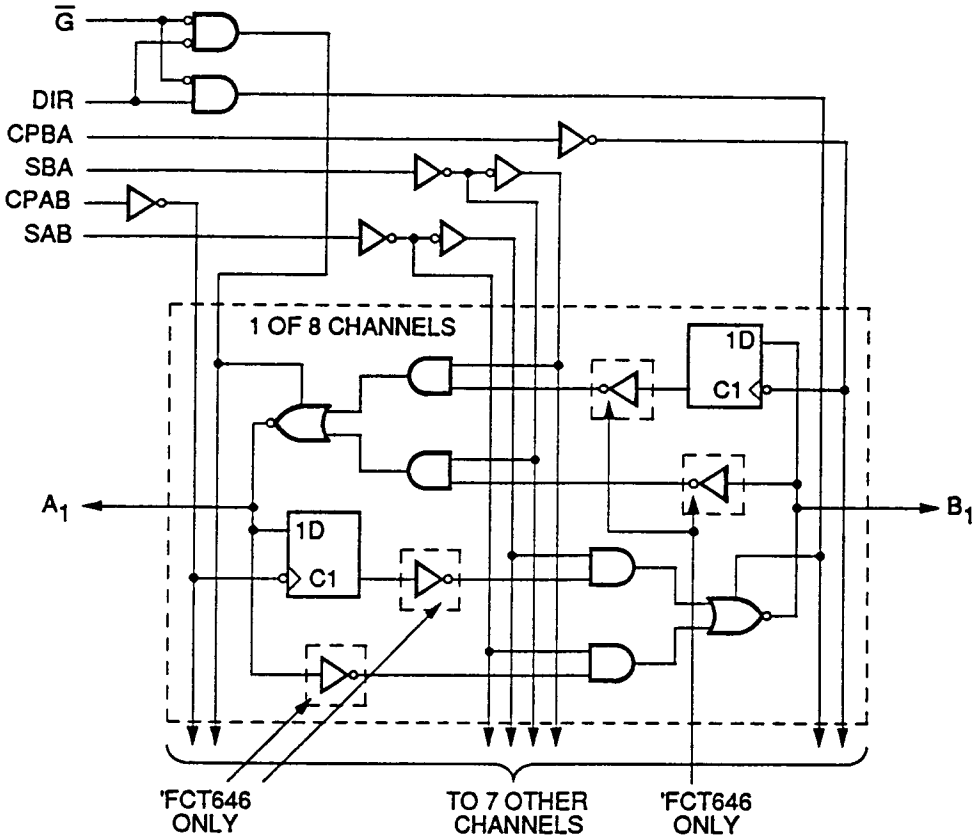
LOGIC SYMBOL



PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



1815 03

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

1815 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1815 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1815 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1815 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2	V_{CC}		V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.4			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V		GND	0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial (TTL)		0.3	0.55	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (I/O Pins only)				15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (I/O Pins only)				–15	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120		mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

1815 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, Outputs Open, f_1 = 0, V_{IN} = 3.4V
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$ = GND, and DIR = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, 50% Duty Cycle, $\overline{G}$ = GND, DIR = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, 50% Duty Cycle, $\overline{G}$ = GND, DIR = GND, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling, DIR = GND, $\overline{G}$ = GND, f_1 = 5 MHz, 50% Duty Cycle, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling, DIR = GND $\overline{G}$ = GND, f_1 = 5 MHz, 50% Duty Cycle, V_{IN} = 3.4V, V_{IN} = GND

1815 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} * D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'FCT646	'FCT648
H H	X X	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus

Notes: 1815 Tbl 07

1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are alwaysenabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
2. H = HIGH, L = LOW, X = Don't Care, ↓ = LOW-to-HIGH Transition

AC CHARACTERISTICS

Symbol	Parameter	'FCT646/648				'FCT646A/648A				'FCT646C/648C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	9.0	2.0	8.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A or B	2.0	10.5	2.0	8.5	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus and Direction to Bus	2.0	10.5	2.0	8.5	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	11.0	2.0	9.5	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 5

1815 Tbl 08

Note:

1. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

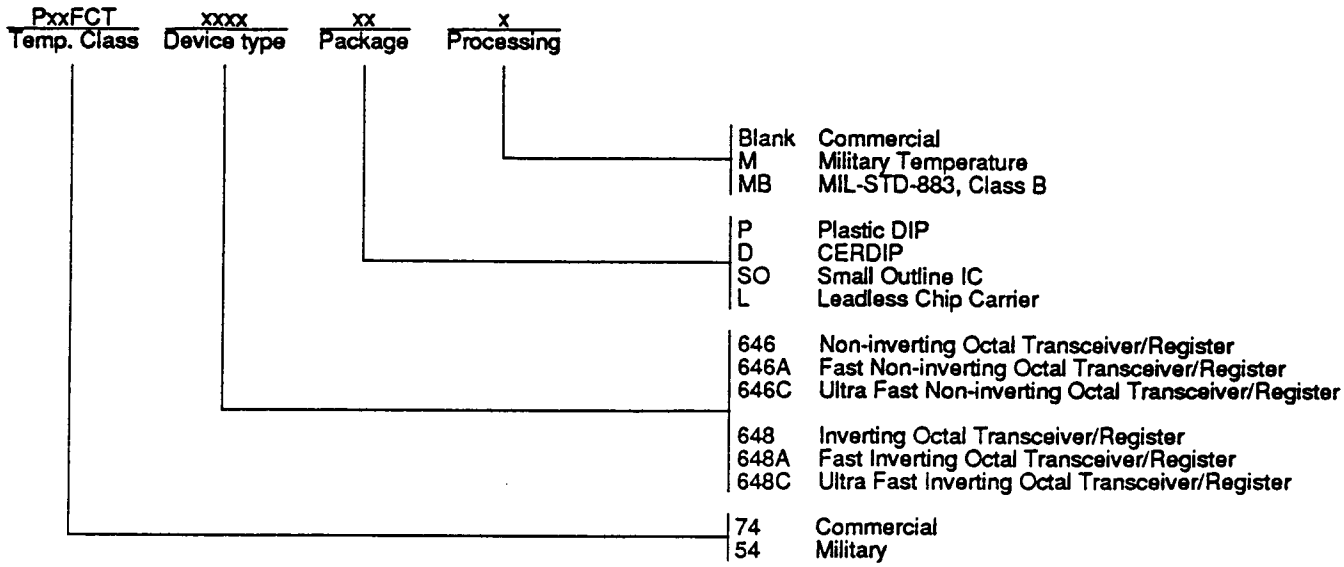
AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT646/648				'FCT646A/648A				'FCT646C/648C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	-	4.0	-	2.0	-	2.0	-	2.0	-	2.0	-	ns	4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	-	2.0	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW	6.0	-	6.0	-	5.0	-	5.0	-	5.0	-	5.0	-	ns	5

Note: 1815 Tbl 09

1. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION



1815 04

032281