M74HC113P/FP/DP

DUAL J-K FLIP-FLOP WITH SET

DESCRIPTION

The M74HC113 is a semiconductor integrated circuit consisting of of two negative-edge triggered J-K flip flops with independent control inputs.

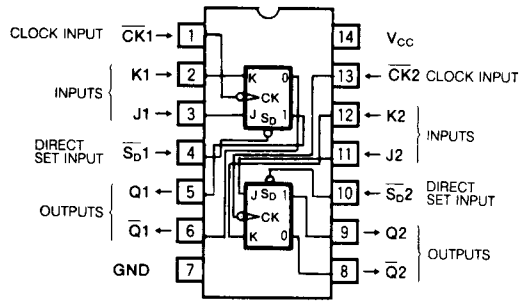
FEATURES

- High-speed: 50MHz clock frequency typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4, 14P2N, 14P2P

FUNCTIONAL DESCRIPTION

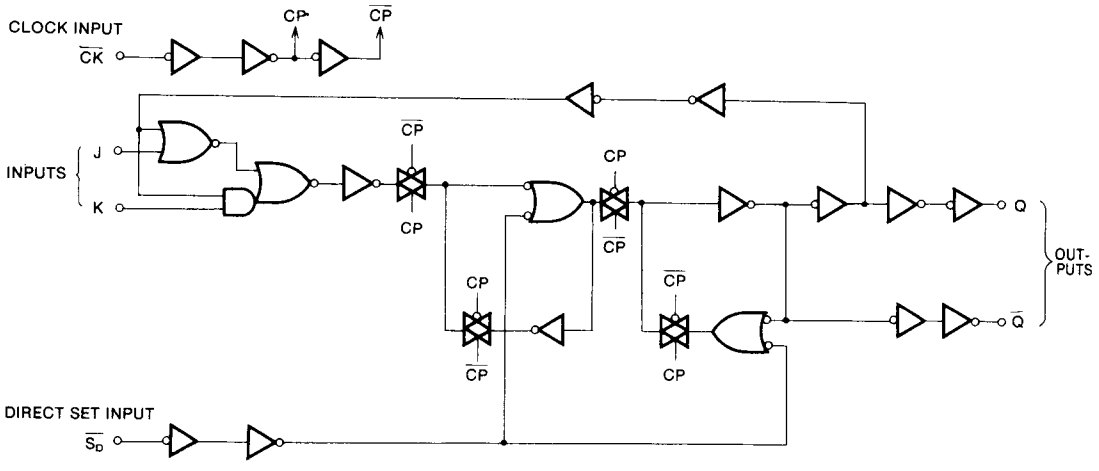
Use of silicon gate technology allows the M74HC113 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS113.

The M74HC113 contains two edge-triggered J-K flip flops, each circuit with independent clock input $\overline{CK}$, direct set input $\overline{S_D}$, and both inputs J and K.

When $\overline{CK}$ is high, the J and K signals can be read.

When $\overline{CK}$ changes from high-level tb low-level, the signals just previously input at J and K appear at outputs Q and $\overline{Q}$ in accordance with the function table given. When $\overline{S_D}$ is low, Q and $\overline{Q}$ will become high and low respectively, irrespective of other inputs. When used as a J-K flip flop, $\overline{S_D}$ should be maintained at high-level.

LOGIC DIAGRAM (EACH FLIP FLOP)



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FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{CK}$	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q^0	$\overline{Q}^0$
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$
H	↑	X	X	Q^0	$\overline{Q}^0$

Note 1 : ↑ : Change from low to high
↓ : Change from high to low
X : Irrelevant
Q^0 : Output state before clock input changed
$\overline{Q}^0$: Output state before clock input changed
Toggle : Inversion state before clock input changed

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC113FP, T_a = −40∼+60℃ and T_a = 60∼85℃ are derated at −6mW/℃.
M74HC113DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)				21	ns
t_{PHL}					21	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)				26	ns
t_{PHL}					26	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

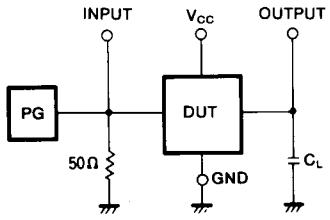
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	31			24		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CK}$ − Q, $\overline{Q}$)		2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			126		160	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{S_D}$ − Q, $\overline{Q}$)		2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
t_{PHL}			2.0			165		210	ns
			4.5			33		41	
			6.0			28		35	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				52				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

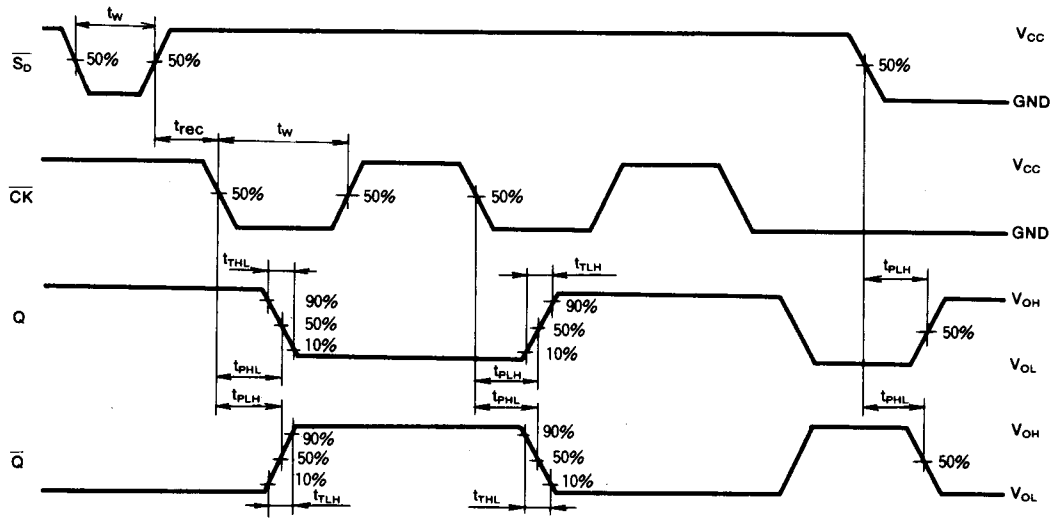
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	$\overline{CK}$, $\overline{S_D}$ pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	J, K setup time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	J, K hold time with respect to $\overline{CK}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	$\overline{S_D}$ recovery time with respect to $\overline{CK}$		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		

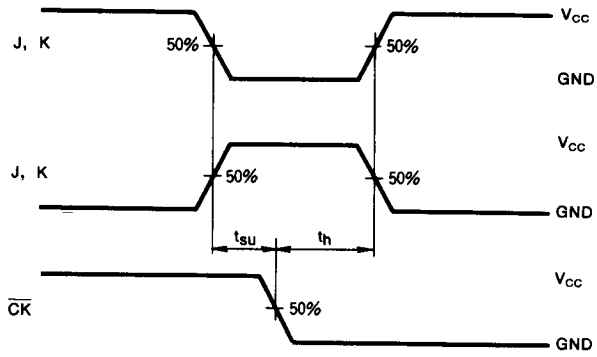
Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





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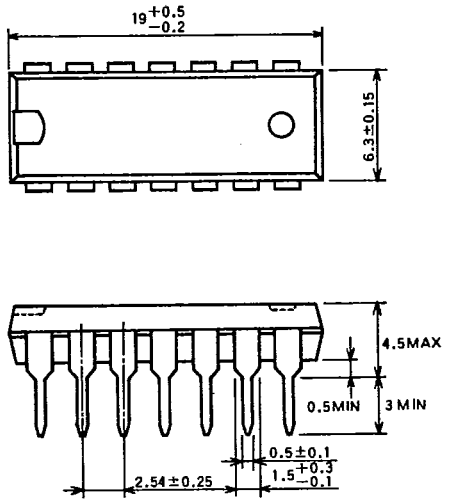
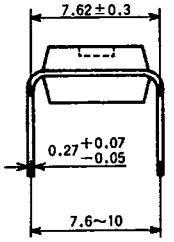
PACKAGE OUTLINES

TYPE 14P4 14-PIN MOLDED PLASTIC DIP

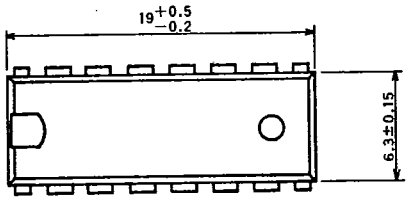
Dimension in mm

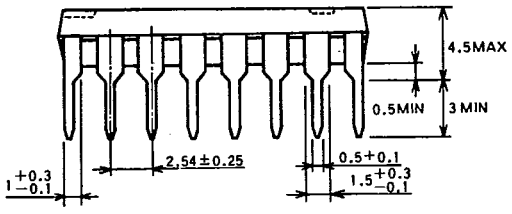


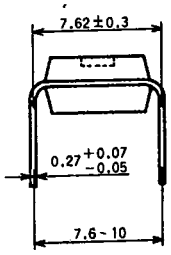


TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm





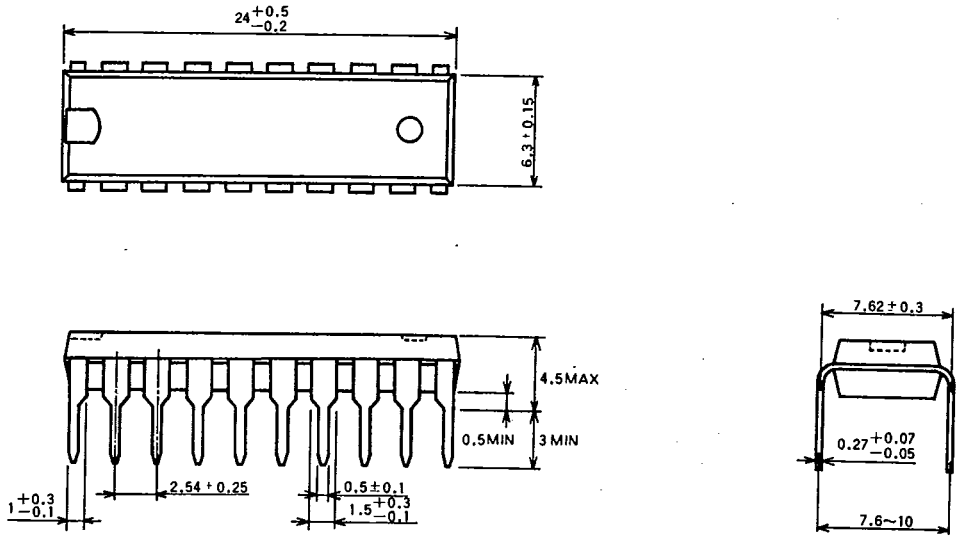


MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

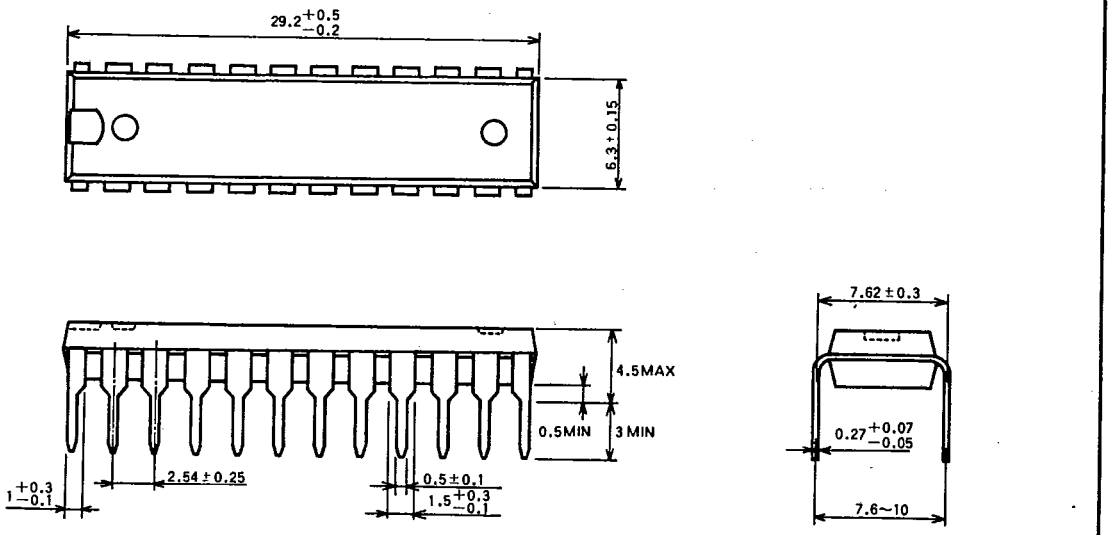
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



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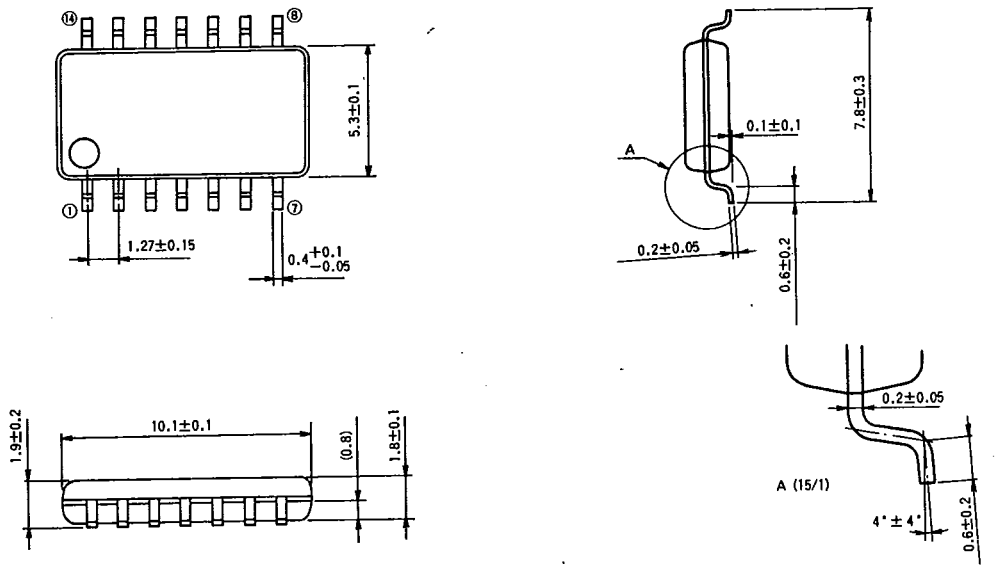
PACKAGE OUTLINES

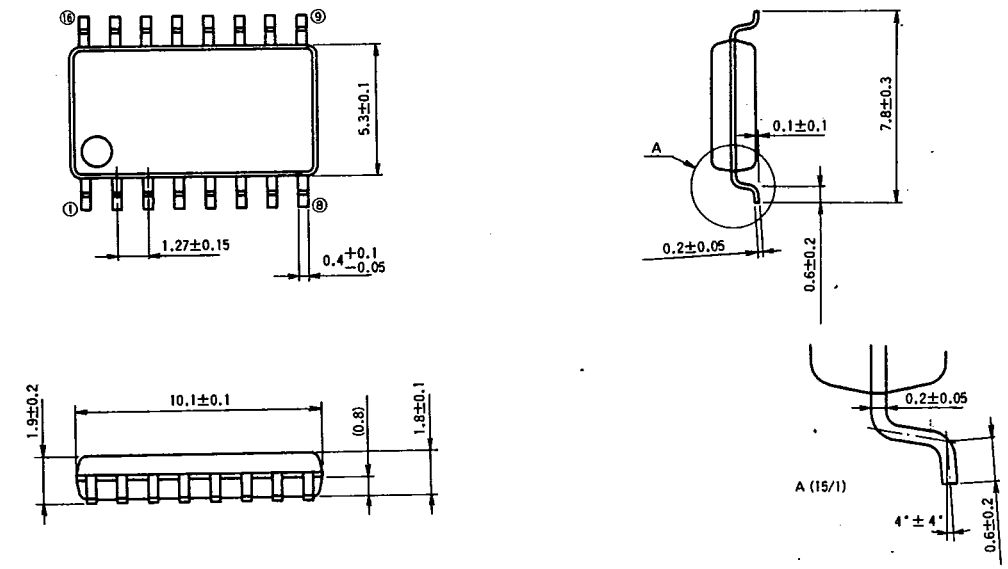
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

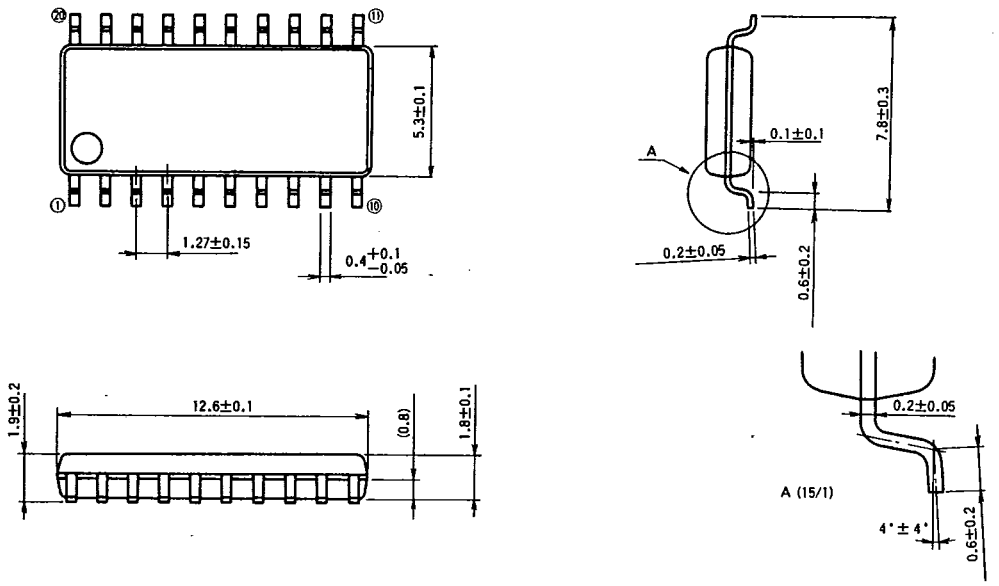
Dimension in mm



PACKAGE OUTLINES

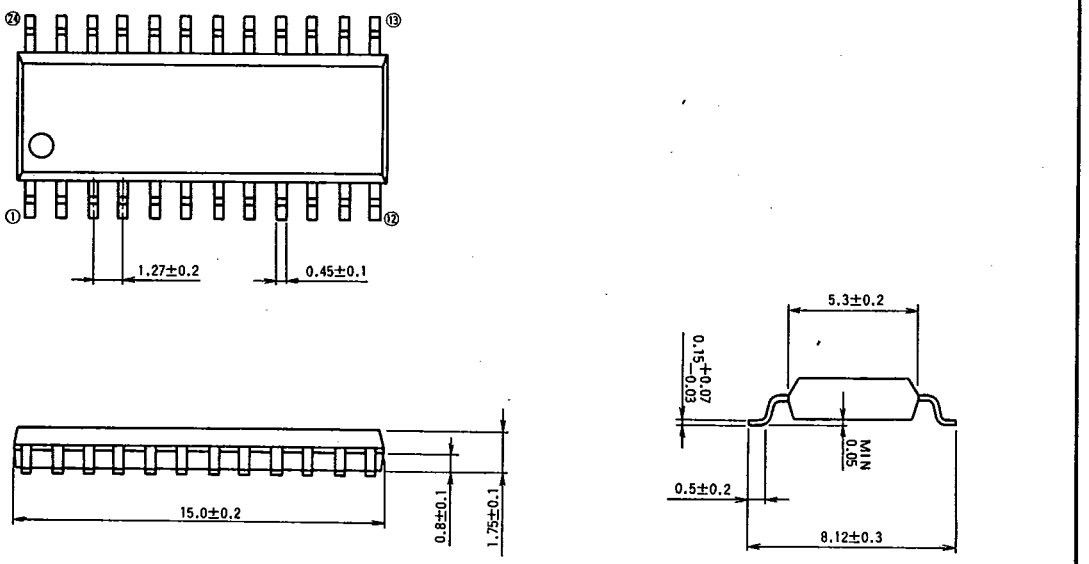
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm



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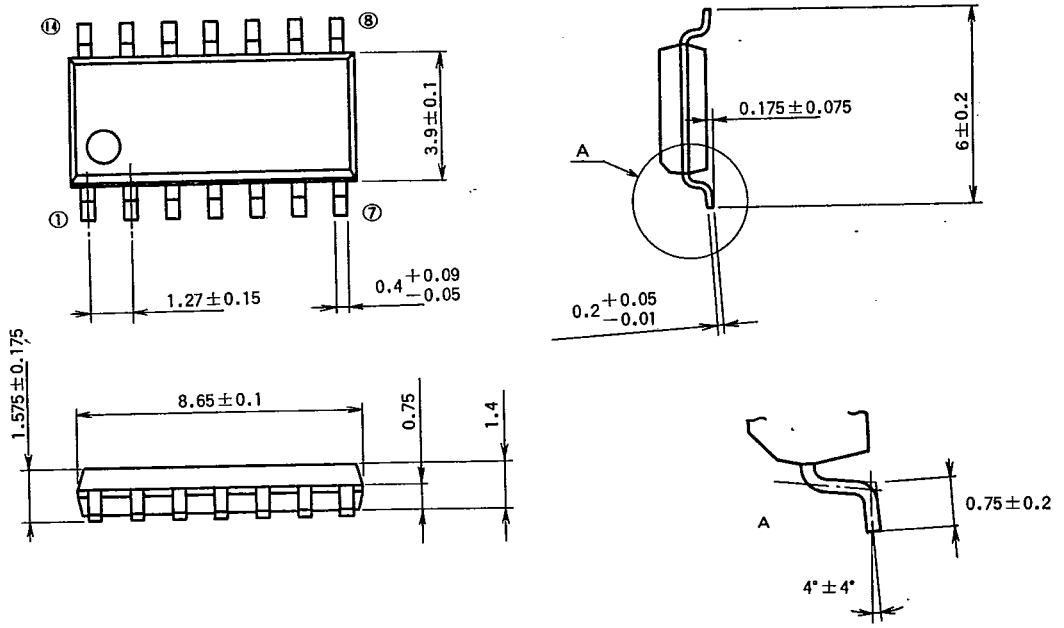
PACKAGE OUTLINES

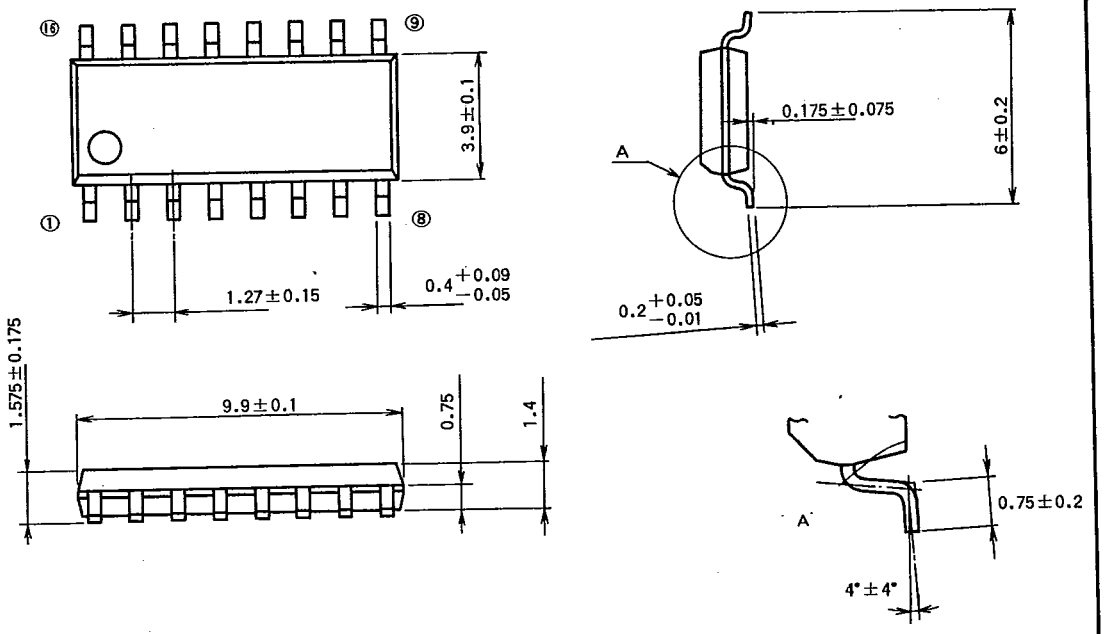
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm