Dual N-Channel JFET Low Noise Amplifier

calogic CORPORATION

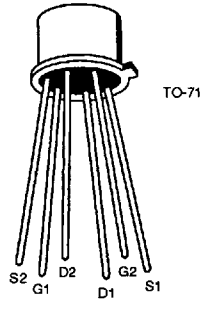
T-27-27

2N5515 – 2N5524

FEATURES

- Tight Temperature Tracking
- Tight Matching
- High Common Mode Rejection
- Low Noise

PIN CONFIGURATION



6037 - 2N5515-19
6019 - 2N5520-24

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current (Note 1) 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

	One Side	BothSides
Power Dissipation (T_A = 85°C)	250mW	375mW
Derate above 25°C	2.0mW/°C	3.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ORDERING INFORMATION

Part	Package	Temperature Range
2N5515	Hermetic TO-71	-55°C to +150°C
2N5516	Hermetic TO-71	-55°C to +150°C
2N5517	Hermetic TO-71	-55°C to +150°C
2N5518	Hermetic TO-71	-55°C to +150°C
X2N5518	Sorted Chips in Carriers	-55°C to +150°C
2N5519	Hermetic TO-71	-55°C to +150°C
X2N5519	Sorted Chips in Carriers	-55°C to +150°C
2N5520	Hermetic TO-71	-55°C to +150°C
2N5521	Hermetic TO-71	-55°C to +150°C
2N5522	Hermetic TO-71	-55°C to +150°C
2N5523	Hermetic TO-71	-55°C to +150°C
X2N5523	Sorted Chips in Carriers	-55°C to +150°C
2N5524	Hermetic TO-71	-55°C to +150°C
X2N5524	Sorted Chips in Carriers	-55°C to +150°C

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current			-250	pA	V_{GS} = -30V, V_{DS} = 0	
				-250	nA		T_A = 150°C
BV_{GSS}	Gate-Source Breakdown Voltage		-40		V	I_G = -1μA, V_{DS} = 0	
V_P	Gate-Source Pinch-Off Voltage		-0.7	-4		V_{DS} = 20V, I_D = 1nA	
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)		0.5	7.5	mA	V_{DS} = 20V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)		1000	4000	μs		f = 1kHz
g_{oss}	Common-Source Output Conductance			10			
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3)			5	pF		f = 1MHz
C_{iss}	Common-Source Input Capacitance (Note 3)			25			
$\bar{e}_n$	Equivalent Input Noise Voltage (Note 3)	2N5515-19		30	nV/√Hz	V_{DG} = 20V, I_D = 200μA	f = 10Hz
		2N5520-24		15			
		2N5515-24		10			f = 1kHz
I_G	Gate Current			-100	pA		
				-100	nA		T_A = 125°C
V_{GS}	Gate-Source Voltage		-0 2	-3.8	V		
g_{fs}	Common-Source Forward Transconductance (Note 1)		500	1000	μs		f = 1kHz
g_{oss}	Common-Source Output Conductance			1	μs		

MATCHING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I_{DSS1} / I_{DSS2}	Drain Current Ratio at Zero Gate Voltage (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1		V_{DS} = 20V, V_{GS} = 0
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current (+125°C)		10		10		10		10		10	nA	V_{DG} = 20V, I_D = 200μA
g_{fs1} / g_{fs2}	Transconductance Ratio (Note 1)	0 97	1	0.97	1	0.95	1	0.95	1	0.90	1		V_{DG} = 20V, I_D = 200μA, f = 1kHz
$\lvert g_{oss1} - g_{oss2} \rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μs	V_{DG} = 20V, I_D = 200μA, f = 1kHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV	V_{DG} = 20V, I_D = 200μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = -55°C to +125°C)		5		10		20		40		80	$\frac{\mu V}{^\circ C}$	V_{DG} = 20V, I_D = 200μA
CMRR	Common Mode Rejection Ratio (Note 2, 3)	100		100			90					dB	V_{DG} = 10 to 20V, I_D = 200μA

NOTES: 1. Pulse duration of 28ms used during test.
2. CMRR = 20 $\log_{10}\Delta V_{DD}/\Delta\lvert V_{GS1}-V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10V)
3. For design reference only, not 100% tested