



**Low Power CMOS
32Kx8 SRAM
with Common I/O**

**QS83285
PRELIMINARY**

FEATURES/BENEFITS

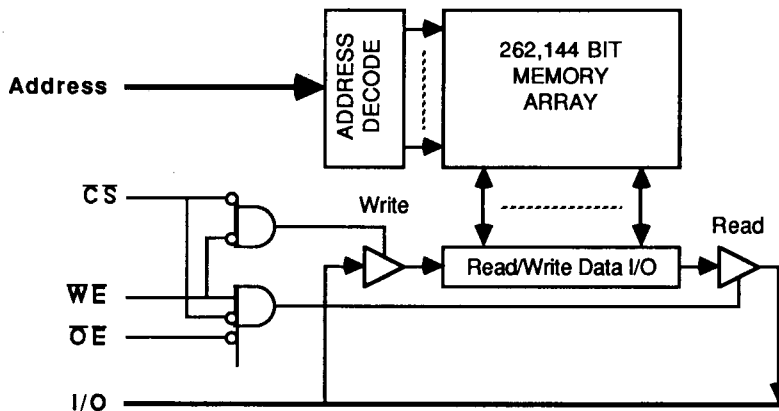
- Ultra low stby. power for battery backup applications
- 70ns/85ns/100ns/120ns Commercial
- 85ns/100ns/120ns Military
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- TTL compatible I/O
- JEDEC standard pinout
- Available in 28-pin 300/600-mil PDIP

DESCRIPTION

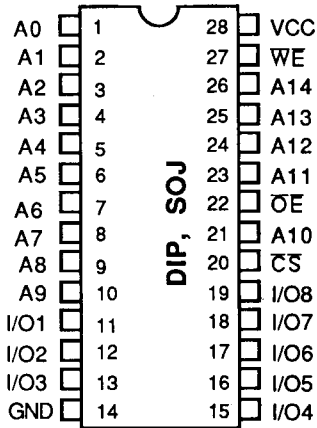
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The QS83285 is a high-speed 256K SRAM organized as 32K words of 8 bits. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83285 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ALL PINS TOP VIEW

PIN DESCRIPTION

| Pin Name | I/O | Function |
|-----------------|-----|---------------|
| A | I | Address |
| I/O1 - I/O8 | I/O | Data |
| \overline{CS} | I | Chip Select |
| \overline{WE} | I | Write Enable |
| \overline{OE} | I | Output Enable |

FUNCTION TABLE

| Function | \overline{CS} | \overline{WE} | \overline{OE} | I/O | Power |
|----------------|-----------------|-----------------|-----------------|----------|---------|
| Deselect | H | X | X | High Z | Standby |
| Read | L | H | L | Data out | Active |
| Write | L | L | X | Data In | Active |
| Output Disable | L | H | H | High Z | Active |

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
 DC Output Voltage V_O -0.5V to $V_{CC} + 0.5V$
 DC Input Voltage V_I -0.5V to $V_{CC} + 0.5V$
 AC Input Voltage (for a pulse width ≤ 20 ns)..... -3.0V
 DC Output Current Max. sink current/pin..... 50 mA
 DC Output Current Max. source current/pin..... 30 mA
 T_{BIAS} Temperature Under Bias, COM..... -65° to +125°C
 T_{STG} Storage Temperature, COM..... -65° to +125°C
 T_{BIAS} Temperature Under Bias, MIL..... -65° to +135°C
 T_{STG} Storage Temperature, MIL..... -65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

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CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1$ MHz

| Name | Description | Conditions | Typ | Max | Unit |
|------|--------------------|---------------------------|-----|-----|------|
| Cin | Input Capacitance | $V_{in} = 0$ V PDIP Pkg. | 3 | 6 | pF |
| Cin | Input Capacitance | $V_{in} = 0$ V SOJ Pkg. | 2.5 | 5 | pF |
| Cout | Output Capacitance | $V_{out} = 0$ V PDIP Pkg. | | 7 | pF |
| Cout | Output Capacitance | $V_{out} = 0$ V SOJ Pkg. | | 7 | pF |

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

| Symbol | Parameter | Test Conditions | Commercial | | Military | | Unit |
|--------|-----------------------|--|------------|-----|----------|-----|-------|
| | | | Min | Max | Min | Max | |
| Vih | Input HIGH Voltage | Logic High for All Inputs | 2.2 | 6.0 | 2:2 | 6.0 | Volts |
| Vil | Input LOW Voltage (1) | Logic Low for All Inputs | | 0.8 | | 0.8 | |
| Voh | Output HIGH Voltage | Ioh = -1 mA, Vcc = MIN | 2.4 | | 2.4 | | |
| Vol | Output LOW Voltage | Iol = 2.1 mA, Vcc = MIN | | 0.4 | | 0.4 | |
| Ii | Input Leakage | Vcc = MAX, Vin = GND to Vcc | | 2 | | 4 | µA |
| Io | Output Leakage | Vcc = MAX, Vout = GND to Vcc Chip deselected | | 2 | | 4 | |

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

| Symbol | Parameter | Max COM. | Max MIL. | Unit |
|--------|---|----------|----------|------|
| Icc1 | Operating Current, CS = Vil, WE = Vih, Other inputs = Vih/Vil Vcc = MAX Outputs open f = max, 70/85ns | 55 | 60 | mA |
| Icc2 | Operating Current, CS = Vil, WE = Vih, Other inputs = Vih/Vil Vcc = MAX Outputs open f = max, 100-150 ns | 45 | 50 | |
| Icb1 | Standby Current, Vcc = MAX Outputs open CS ≥ Vih | 3.0 | 4.0 | |

| Symbol | Parameter | Max COM. | Max MIL. | Unit |
|--------|---|----------|----------|------|
| Icb2 | Standby Current, Vcc = 2.0-5.5V CS ≥ Vcc-0.2V Vin ≤ 0.2V or Vin ≥ Vcc -0.2V | 1.0 | 5.0 | µA |
| Icb3 | Standby Current, Vcc = 2.0V CS ≥ Vcc-0.2V Vin ≤ 0.2V or Vin ≥ Vcc -0.2V | 0.5 | 3.0 | |

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

| Symbol | Parameter (1) | 70ns | | 85ns | | 100ns | | 120ns | |
|-------------------|-------------------------------------|------|-----|------|-----|-------|-----|-------|-----|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| READ CYCLE | | | | | | | | | |
| t RC | Read Cycle Time | 70 | - | 85 | - | 100 | - | 120 | - |
| t AA | Address Access Time | - | 70 | - | 85 | - | 100 | - | 120 |
| t ACS | Chip Select Access Time | - | 70 | - | 85 | - | 100 | - | 120 |
| t OH | Output Hold from Address | 5 | - | 5 | - | 5 | - | 5 | - |
| t CLZ | Chip Select to Output in Low Z (2) | 10 | - | 10 | - | 10 | - | 10 | - |
| t CHZ | Chip Select to Output in High Z (2) | - | 30 | - | 30 | - | 35 | - | 40 |
| t OE | Output Enable Access Time | | 35 | | 45 | | 50 | | 60 |
| t OHZ | Output enable to output in High Z | - | 30 | - | 30 | - | 35 | - | 40 |
| t OLZ | Output enable to output in Low Z | 5 | - | 5 | - | 5 | - | 5 | - |
| t PU | Chip select to Power-Up Time (2) | 0 | - | 0 | - | 0 | - | 0 | - |
| t PD | Chip select to Power-Down Time | - | 70 | - | 85 | - | 100 | - | 120 |

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

QS83285

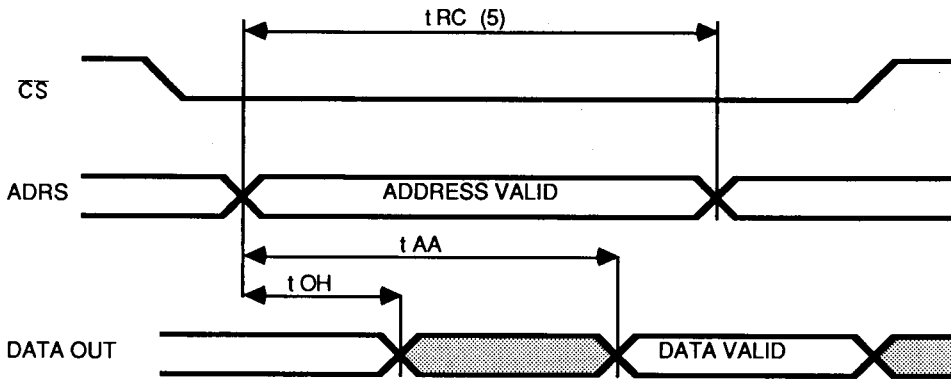
Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

| Symbol | Parameter (1) | 70ns | | 85ns | | 100ns | | 120ns | |
|--------------------|---|------|-----|------|-----|-------|-----|-------|-----|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| WRITE CYCLE | | | | | | | | | |
| tWC | Write Cycle Time | 70 | | 85 | | 100 | | | 120 |
| tCW | Chip Select Valid to End of Write | 65 | | 75 | | 90 | | 100 | |
| tAS | Address Setup Time | 0 | | 0 | | 0 | | 0 | |
| tWP | Write Pulse width | 55 | | 65 | | 70 | | 80 | |
| tWR | Write Recovery Time | 0 | | 0 | | 0 | | 0 | |
| tDW | Data Valid to End of Write | 35 | | 40 | | 45 | | 50 | |
| tDH | Data Hold Time | 0 | | 0 | | 0 | | 0 | |
| tWZ | Write Enable to Output in High Z (2) | - | 30 | - | 30 | - | 35 | - | 40 |
| tOW | Output Active from End of Write (2) | 5 | | 5 | | 5 | | 5 | |
| tAW | Address Valid to End of Write | 65 | | 75 | | 90 | | 100 | |

Notes:

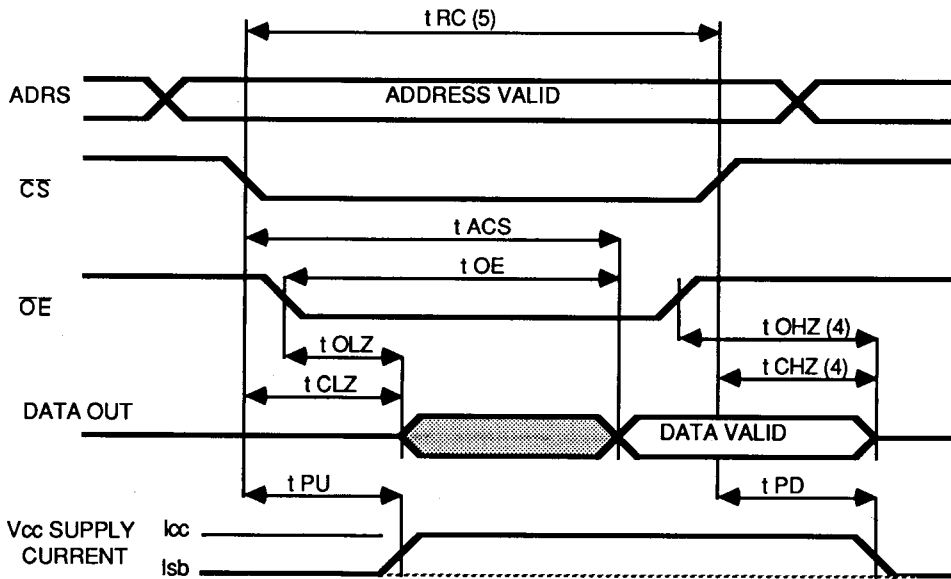
- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2,3)



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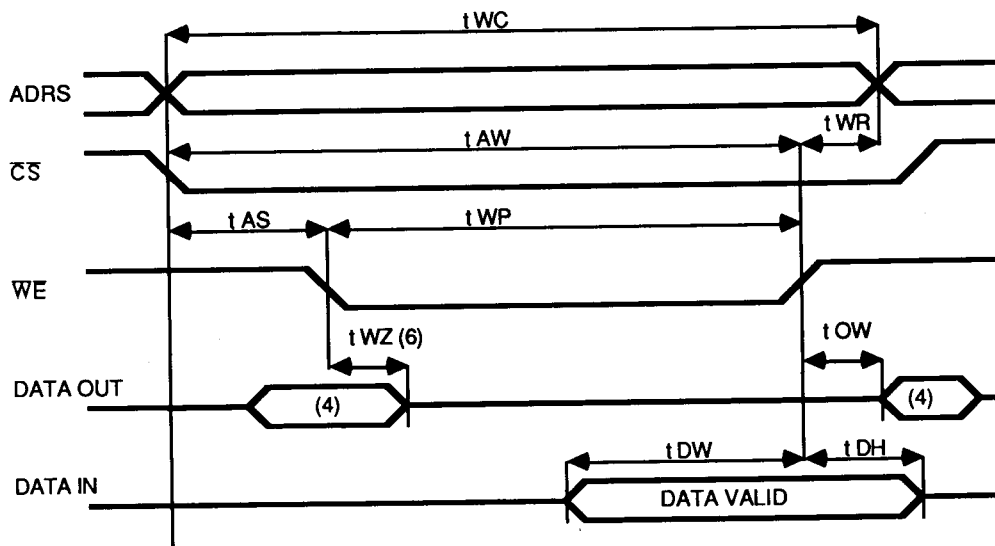
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



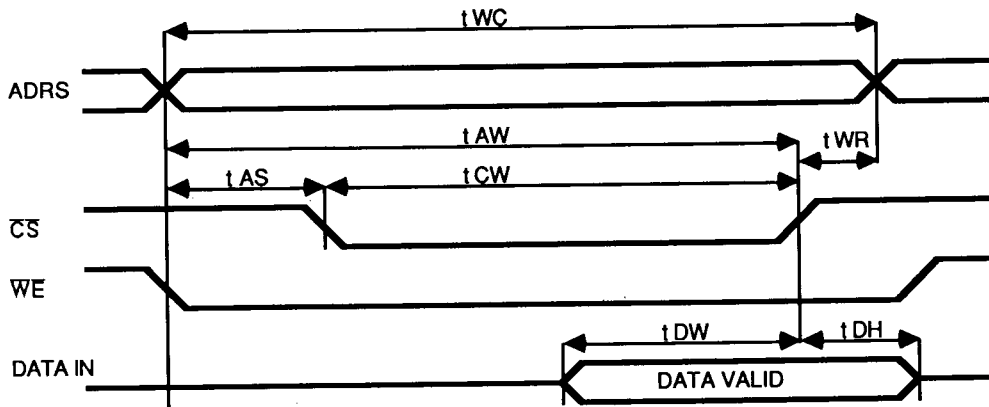
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. t_{WR} is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.