

## 54F/74F823

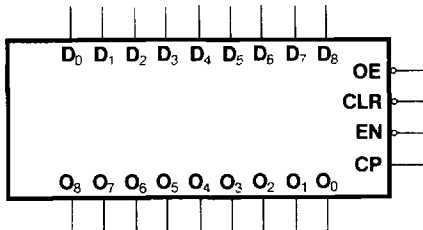
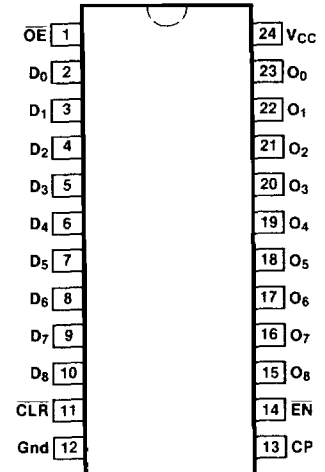
## 9-Bit D-Type Flip Flop

**Description**

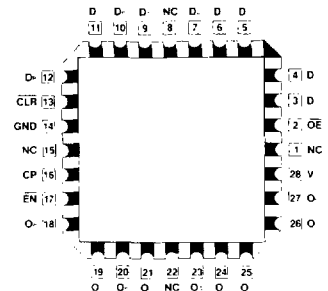
The 'F823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

The 'F823 is fully compatible with AMD's Am29823.

**Ordering Code:** See Section 3

**Logic Symbol****Connection Diagrams**

**Pin Assignment  
for DIP and SOIC**



**Pin Assignment  
for LCC and PCC**

**Input Loading/Fan-Out:** See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D <sub>0</sub> -D <sub>8</sub>	Data Inputs	0.5/0.375
O <sub>0</sub> -O <sub>8</sub>	Data Outputs	75/15 (12.5)
$\overline{OE}$	Output Enable	0.5/0.375
CLR	Clear	0.5/0.375
CP	Clock Input	0.5/0.75
$\overline{EN}$	Clock Enable	0.5/0.375

### Functional Description

The 'F823 device consists of nine D-type edge-triggered flip-flops. It has 3-state true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the  $\overline{OE}$  LOW the contents of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 'F823 has Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins. This device is ideal for parity bus interfacing in high performance systems.

When the  $\overline{CLR}$  is LOW and the  $\overline{OE}$  is LOW, the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW to HIGH clock transition. When the  $\overline{EN}$  is HIGH, the outputs do not change state regardless of the data or clock inputs transitions.

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### Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↑	L	L	Z	High Z
H	X	L	↑	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↑	L	L	Z	Load
H	H	L	↑	H	H	Z	Load
L	H	L	↑	L	L	L	Load
L	H	L	↑	H	H	H	Load

H = HIGH Voltage Level

L = LOW Voltage Level

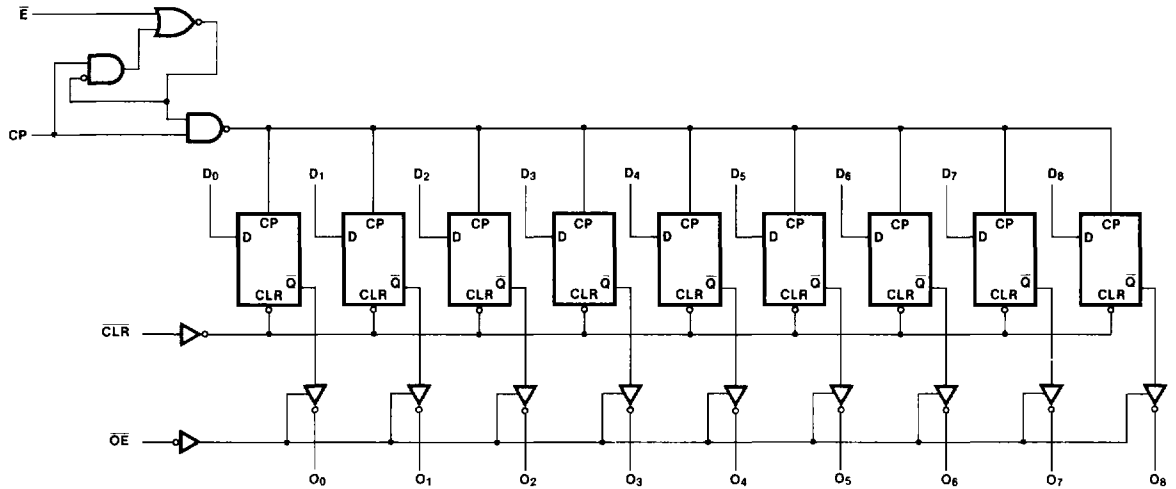
X = Immaterial

Z = High Impedance

↑ = LOW-to-HIGH Transition

NC = No Change

**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**DC Characteristics over Operating Temperature Range (unless otherwise specified)**

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
$I_{CC}$	Power Supply Current			110	mA	$V_{CC} = \text{Max}$

**AC Characteristics:** See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F		54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min		
$f_{\text{max}}$	Maximum Clock Frequency	100						MHz	3-1
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $O_n$		7.5					ns	3-1 3-7
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{CLR}}$ to $O_n$		15.0					ns	3-1 3-9
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time $\overline{\text{OE}}$ to $O_n$		11.5					ns	3-1 3-12
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time $\overline{\text{OE}}$ to $O_n$		7.0						
			5.5						3-13

**AC Operating Requirements:** See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$	$T_A, V_{CC} =$ Mil	$T_A, V_{CC} =$ Com		
		Min Typ Max	Min Max	Min Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_n$ to CP	2.0 2.0			ns	3-5
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $D_n$ to CP	2.0 2.0				
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{EN}}$ to CP	3.0 3.0			ns	3-5
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{EN}}$ to CP	0 0				
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width HIGH or LOW	5.0 5.0			ns	3-7
$t_w(\text{L})$	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0			ns	3-9
$t_{\text{rec}}$	$\overline{\text{CLR}}$ Recovery Time	5.0			ns	3-11