

MB82208-25/-35

CMOS 4M-BIT HIGH SPEED SRAM

524,288-WORD x 8-BIT HIGH SPEED STATIC RANDOM ACCESS MEMORY

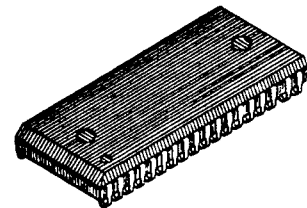
The Fujitsu MB82208 is 524,288-word x 8-bit high speed static random access memory fabricated with CMOS technology.

To obtain smaller chip size, cells consists of NMOS transistors and resistors. MB82208 has 400mil plastic SOJ as package option. All pins are TTL compatible and single 5volt power supply is required.

The MB82208 is ideally suited for use in large computer and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 524,288 words x 8 bits
- Static operation: no clocks or timing strobe required
- Fast access time: $t_{AA}=t_{ACS} = 25\text{ns max. (MB82208-25)}$
 $t_{AA}=t_{ACS} = 35\text{ns max. (MB82208-35)}$
- Low power consumption: 825.0mW max. (TTL Standby)
27.5mW max. (CMOS Standby)
- Single +5V supply $\pm 10\%$ tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- All inputs and outputs have protection against static charge
- Standard 36-pin 400mil SOJ package (Suffix: PJ)

PRELIMINARY



PLASTIC PACKAGE
(LCC-36P-M01)

PIN ASSIGNMENT (TOP VIEW)

A14	1	36	NC
A15	2	35	A13
A16	3	34	A12
A17	4	33	A11
A18	5	32	A10
CS1	6	31	OE
I/O5	7	30	I/O4
I/O6	8	29	I/O3
VCC	9	28	GND
GND	10	27	VCC
I/O7	11	26	I/O2
I/O8	12	25	I/O1
WE	13	24	A0
A1	14	23	A9
A2	15	22	A8
A3	16	21	A7
A4	17	20	A6
A5	18	19	CS2

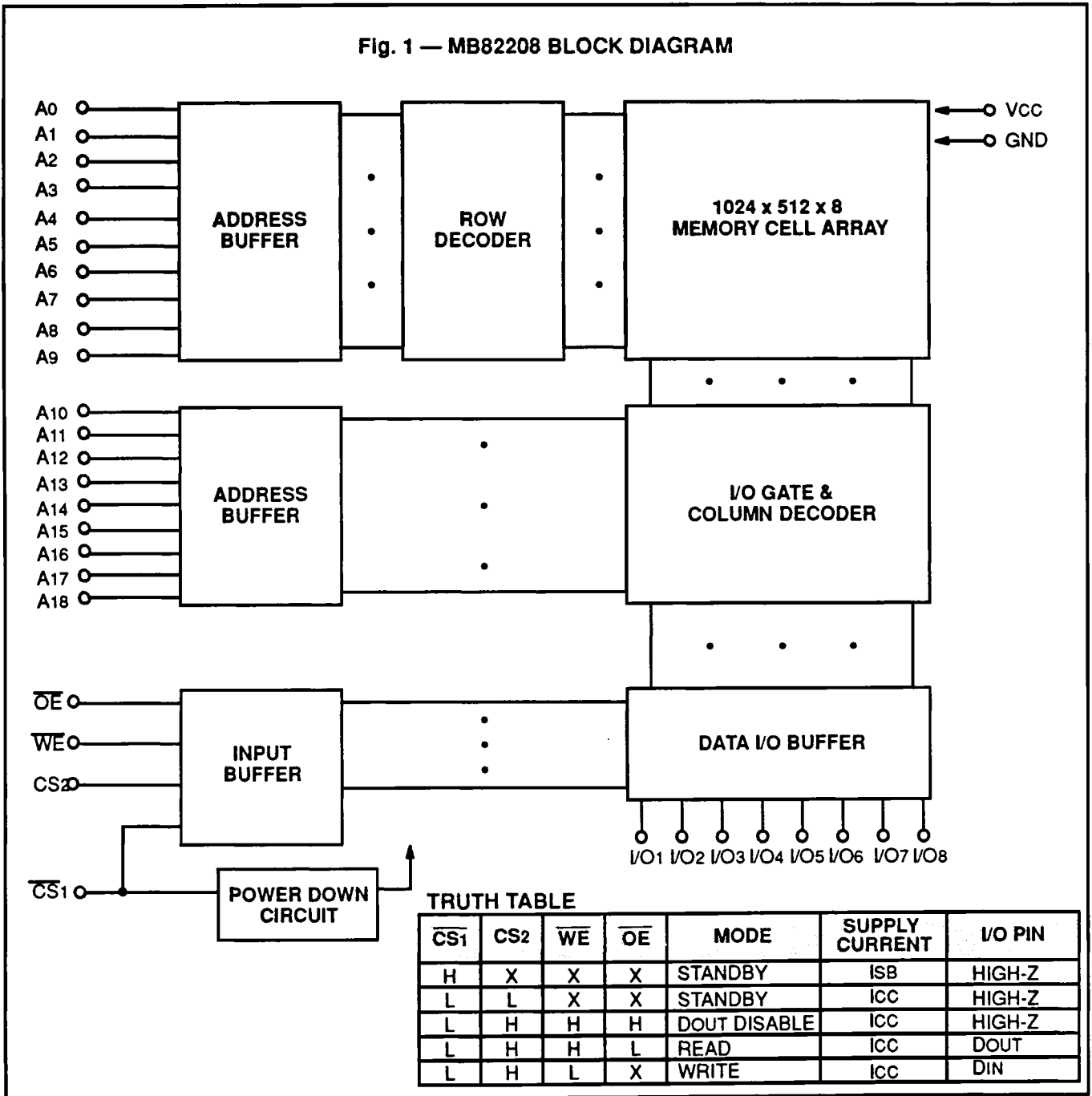
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage on any pin with respect to GND	VIN	-0.5 to VCC+0.5	V
Output Voltage on any I/O pin with respect to GND	VOUT	-0.5 to VCC+0.5	V
Output Current	IOUT	± 20	mA
Power Dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature Range	TSTG	-40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB82208 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS1}$	CS2	\overline{WE}	\overline{OE}	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	STANDBY	ISB	HIGH-Z
L	L	X	X	STANDBY	ICC	HIGH-Z
L	H	H	H	DOUT DISABLE	ICC	HIGH-Z
L	H	H	L	READ	ICC	DOUT
L	H	L	X	WRITE	ICC	DIN

CAPACITANCE ($T_A = 25^\circ C, f = 1MHz$)

Parameter	Symbol	Min	Typ	Max	Unit
Capacitance, A0 – A18 ($V_1 = 0V$)	C1			6	pF
Capacitance, other pins ($V_2 = 0V$)	C2			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Standby Supply Current	ISB1	$\overline{CS1} \geq VCC - 0.2V$, $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$		5	mA
	ISB2	$VCC = \text{min. to max.}$, $\overline{CS1} = VIH$, $t_{Cyc} = \text{min.}$		25	mA
Operating Supply Current	ICC1	$I_{OUT} = 0mA$, $\overline{CS1} = VIL$, $t_{Cyc} = \text{min.}$ $VIN = VIL$ or VIH		150	mA
Input Leakage Current	ILI	$VIN = 0V$ to VCC , $VCC = \text{Max.}$	-10	10	μA
Output Leakage Current	ILO	$\overline{CS1} = VIH$, $V_{OUT} = 0V$ to VCC , $VCC = \text{max.}$	-10	10	μA
Input Low Voltage	VIL		-0.5*1	0.8	V
Input High Voltage	VIH		2.2	$VCC + 0.3$	V
Output High Voltage	VOH	$I_{OH} = -4mA$	2.4		V
Output Low Voltage	VOL	$I_{OL} = 8mA$		0.4	V

Note: *1 -2.0V Min. for pulse width less than 10ns. (VIL min. = -0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: 2ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input :VIL=0.8V, VIH=2.2V
Output :VOL=0.8V, VOH=2.2V

• Output Load:
+5V
R1
DOUT(I/O)
CL*1
R2

*1 Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480k Ω	255 Ω	30pF	except tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ
Load II	480k Ω	255 Ω	5pF	tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ

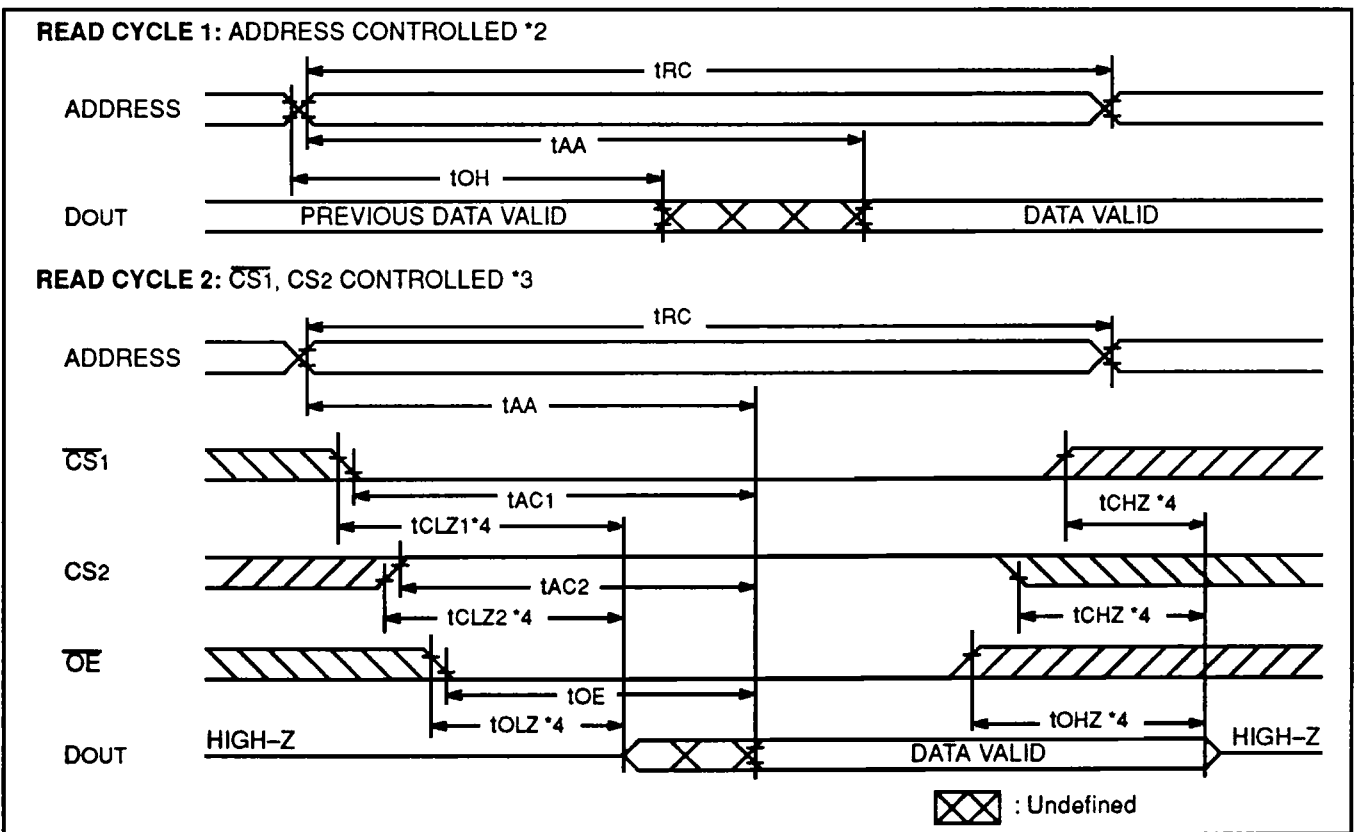
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82208-25		MB82208-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	25		35		ns
Address Access Time *2	tAA		25		35	ns
CS1 Access Time *3	tAC1		25		35	ns
CS2 Access Time *3	tAC2		15		20	ns
Output Enable to Output Valid	tOE		15		20	ns
Output Hold from Address Change	tOH	5		5		ns
CS1 to OutputLow-Z *4	tCLZ1	5		5		ns
CS2 to OutputLow-Z *4	tCLZ2	2		2		ns
Output Enable to Output Low-Z *4	tOLZ	2		2		ns
Chip Select to Output High-Z *4	tCHZ		12		15	ns
Output Enable to Output High-Z *4	tOHZ		12		15	ns

READ CYCLE TIMING DIAGRAM *1



- Notes: *1 WE is high for Read Cycle.
 *2 Device is continuously selected, CS1 = OE = VIL, CS2 = VIH.
 *3 Address valid prior to or coincident with CS1 transition low, CS2 transition high.
 *4 Transition is measured at the point of ±500mV from steady state voltage with load II as specified in Fig. 2.

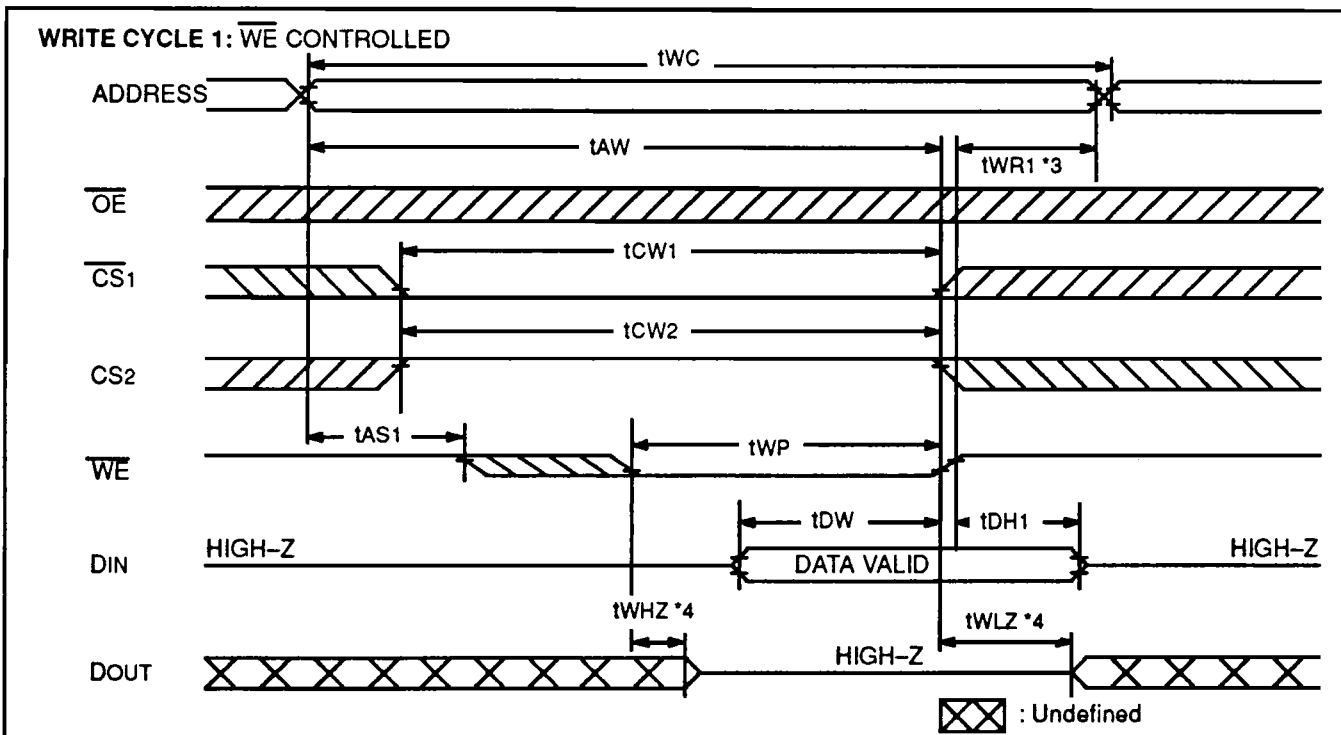
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE *1 *2

Parameter	Symbol	MB82208-25		MB82208-35		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	25		35		ns
Address Valid to End of Write	tAW	17		25		ns
CS1 to End of Write	tCW1	17		25		ns
CS2 to End of Write	tCW2	12		15		ns
Data Valid to End of Write	tDW	15		18		ns
Data Hold Time	tDH1	0		0		ns
Data Hold Time for CS2	tDH2	2		2		ns
Write Pulse Width	tWP	17		25		ns
Address Setup Time 1	tAS1	0		0		ns
Address Setup Time 2	tAS2	5		5		ns
Write Recovery Time *3	tWR1	3		3		ns
Write Recovery Time for CS2	tWR2	5		5		ns
Write Enable to Output Low-Z *4	tWLZ	0		0		ns
Write Enable to Output High-Z *4	tWHZ	0	12	0	15	ns

WRITE CYCLE TIMING DIAGRAM *1 *2

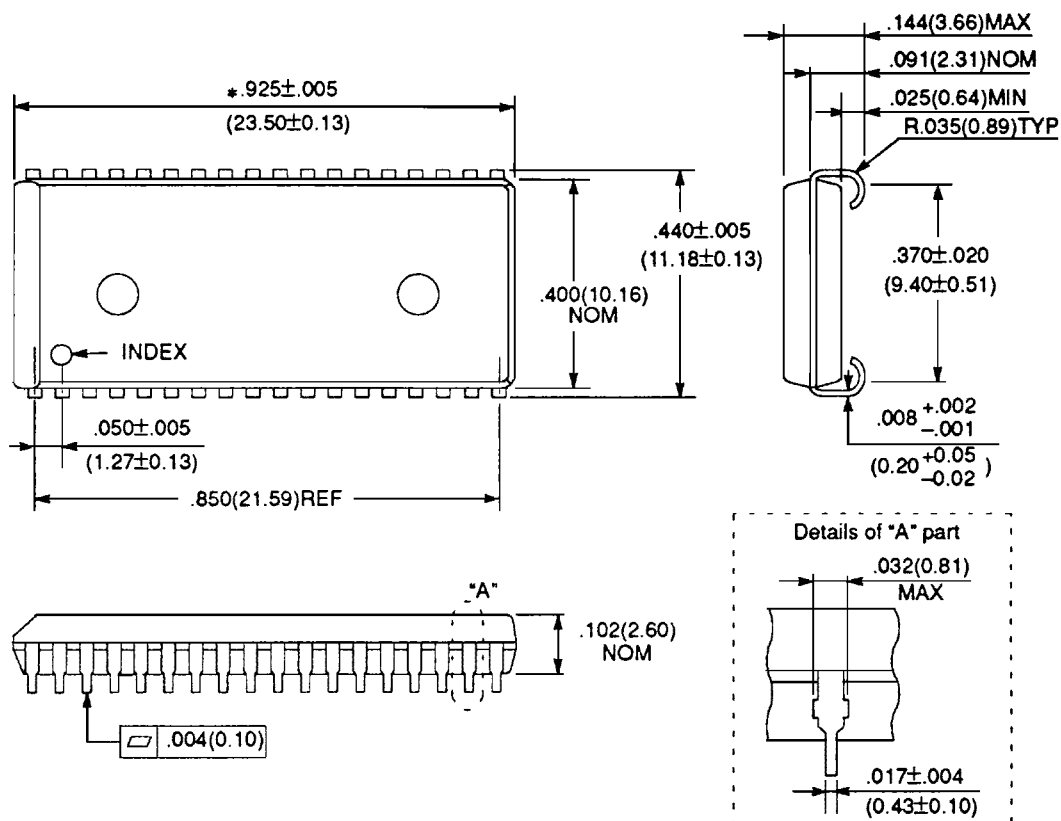


- Notes:**
- *1 If \overline{OE} , $\overline{CS1}$ and $\overline{CS2}$ are in the READ Mode during this period, the I/O pins are in the output state and the input signals of opposite phase to the outputs must not be applied.
 - *2 If $\overline{CS1}$ goes high or $\overline{CS2}$ goes low simultaneously with \overline{WE} high, the output remains in high impedance state.
 - *3 t_{WR} is defined from the end point of WRITE Mode.
 - *4 Transition is measured at the point of $\pm 500\text{mV}$ from steady state voltage with Load II as specified in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: PJ)

36-LEAD PLASTIC LEADED CHIP CARRIER (CASE No.: LCC-36P-M01)



*Resin protrusion. (Each side: $.006$ (0.15) MAX.)

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Dimensions in
inches (millimeters)

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