DG421/423/425
Low-Power – High-Speed Latchable CMOS Analog Switches

Siliconix incorporated

T-51-11

FEATURES

- Latched Inputs
- ±15 Volt Input Range
- On-Resistance <35 Ω
- Fast Switching Action t_{ON} <250 ns
- Micropower Requirements (P_D <35 µW)
- TTL, CMOS Compatible

BENEFITS

- Wide Dynamic Range
- µP Compatible
- Reduced Component Count
- low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Battery Operation

APPLICATIONS

- High Performance Data Bus Switching
- Precision Sample and Hold Circuits
- Digital Filters
- µP Controlled Analog Systems
- Portable Instruments

DESCRIPTION

The DG421 series of dual monolithic analog switches features latchable logic inputs which simplify interfacing with microprocessors. This series combines fast switching speed (t_{ON} <250 ns), and low ON-resistance ($r_{DS(ON)}$ <35 Ω) making it ideally suited for battery powered industrial and military applications that require µP compatible analog switches.

To achieve high-voltage ratings and superior switching performance, the DG421 series is built on Siliconix's high voltage silicon gate CMOS process. Break-before-make is guaranteed for the DG423. An epitaxial layer prevents latchup.

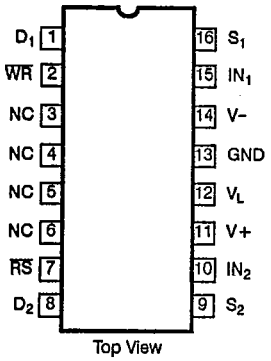
Each switch conducts equally well in both directions when ON and blocks up to 30 volts peak-to-peak when OFF. ON-resistance is nearly flat over the full ±15 V analog range, rivaling JFET performance without the inherent dynamic range and supply voltage limitations.

When $\overline{WR}$ is set LOW the input data latches become transparent. When $\overline{WR}$ goes HIGH the latches store the logic control data. The $\overline{RS}$ pin is used to reset all the switches in the circuit to the default value (all inputs LOW) when it is set LOW.

This family offers three devices, which are differentiated by switch action as shown in the functional block diagrams. Packaging includes 16-pin plastic DIP and CerDIP. Performance grades include both the Industrial, D suffix (-40 to 85°C) and the military, A suffix (-55 to 125°C) temperature ranges. Additionally, a 20-pin PLCC is available for the DG423.

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES

Dual-In-Line Package

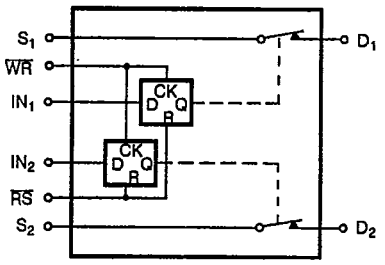


Top View

Order Numbers:

CerDIP: DG421AK, DG421AK/883
Plastic: DG421DJ

DG421



Two SPST Switches per Package

Truth Table*

WR	RS	IN_X	Switch
0	1	0	OFF
		1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES

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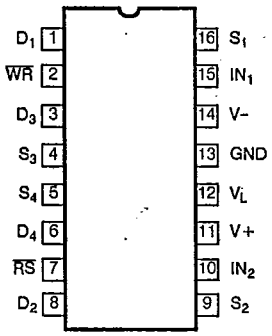
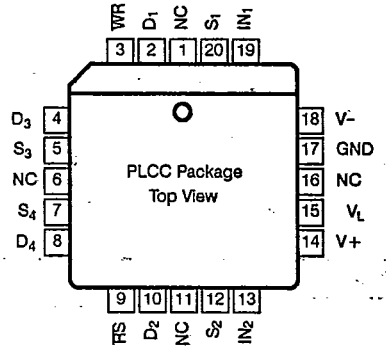
Dual-In-Line Package



Top View

Order Numbers:

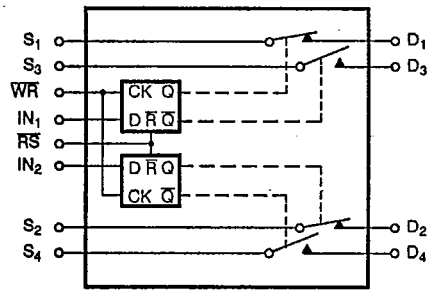
CerDIP: DG423AK, DG425AK
DG423AK/883, DG425AK/883
Plastic: DG423DJ, DG425DJ



Order Number:

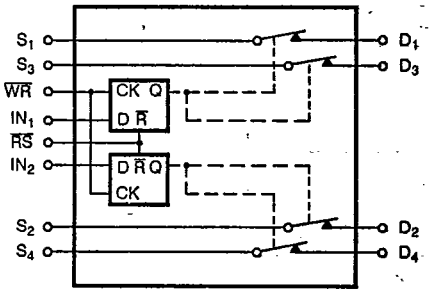
DG423DN

DG423



Two SPDT Switches per Package

DG425



Two DPST Switches per Package

Truth Table

$\overline{WR}$	$\overline{RS}$	IN_X	SW 1, 2	SW 3, 4
0	1	0 1	OFF ON	ON OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

Truth Table

$\overline{WR}$	$\overline{RS}$	IN_X	Switch
0	1	0 1	OFF ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

Latch Operation Truth Table

IN_X	$\overline{RS}$	$\overline{WR}$	Latch/Switch X
X	1	0	Transparent Latch Operation
X	1	⌐	Control Data Latched-in, Switches On or Off as Selected by Last IN_X
X	0	X	All Latches Reset, Switches On or OFF as When IN_X = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 1
X	⌐	X	

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DG421/423/425

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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–
V+ ..... 44 V
GND ..... 25 V
V_L ..... (GND –0.3 V) to (V+) +0.3 V
Digital Inputs[1] V_S, V_D ..... V– minus 2 V to (V+ pius 2 V) or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 40 mA
Current, S or D (Pulsed 1 ms, 10% duty) ..... 100 mA
Storage Temperature (A Suffix) ..... –65 to 150°C
(D Suffix) ..... –65 to 125°C
Operating Temperature (A Suffix) ..... –55 to 125°C
(D Suffix) ..... –40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 470 mW
16-Pin CerDIP*** ..... 900 mW
20-Pin PLCC**** ..... 800 mW

*All leads welded or soldered to PC Board.
**Derate 6 mW/°C above 75°C.
***Derate 12 mW/°C above 75°C.
****Derate 10 mW/°C above 75°C.

[1]Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V– = –15 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX –55 to 125°C MIN[b]	A SUFFIX –55 to 125°C MAX[b]	D SUFFIX –40 to 85°C MIN[b]	D SUFFIX –40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		–15	15	–15	15	V
Drain-Source ON-Resistance[a]	$r_{DS(ON)}$	I_S = –200 mA, V_D = ±8.5 V V+ = 13.5 V, V– = –13.5 V	Room Full	25		35 45		35 45	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V– = –16.5 V V_D = –15.5 V, V_S = 15.5 V	Room Full	–0.01	–0.25 –20	0.25 20	–0.25 –20	0.25 20	nA
	$I_{D(OFF)}$	V_D = 15.5 V, V_S = –15.5 V	Room Full	–0.01	–0.25 –20	0.25 20	–0.25 –20	0.25 20	
Channel ON Leakage Current	$I_{D(ON)}$	V+ = 16.5 V, V– = –16.5 V	Room Full	–0.04	–0.4 –40	0.4 40	–0.4 –40	0.4 40	
DIGITAL CONTROL									
Input Current with V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V all other = 2.4 V	Full	0.005	–0.5	0.5	–0.5	0.5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V all other = 0.8 V	Full	0.005	–0.5	0.5	–0.5	0.5	
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Switching Time Test Circuit	Room Full	170		250 300		250	ns
Turn-OFF Time	t_{OFF}		Room Full	140		200 200		200	
Latch Timing	t_{WW}	R_L = 300 Ω, C_L = 35 pF V_S = ±10 V	Room Full		200 200		200		
	t_{DW}		Room Full		100 100		100		
	t_{WD}		Room Full		60 100		60		
Break-Before-Make Time Delay	t_D	DG423 ONLY R_L = 300 Ω, C_L = 35 pF	Room	25	5		5		
Charge Injection[c]	Q	C_L = 10 nF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	60					pC
OFF Isolation Reject Ratio		R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	65					dB

SPECIFICATIONS[a]

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PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)									
Crosstalk (Channel-to-Channel)		Between Any Two Channels R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	76					dB
Source Off	$C_{S(OFF)}$	f = 1 MHz	Full	9					pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Full	9					
Channel ON Capacitance	$C_{D+S(ON)}$		Full	18					
POWER SUPPLY									
Positive Supply Current	I+	V+ = 16.5 V, C- = -16.5 V V_{IN} = 0 or 5 V	Room Full	0.0001		1 5		1 5	µA
Negative Supply Current	I-		Room Full	-0.0001	-1 -5		-1 -5		
Logic Supply Current	I_L		Room Full	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Full	-0.0001	-1 -5		-1 -5		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY

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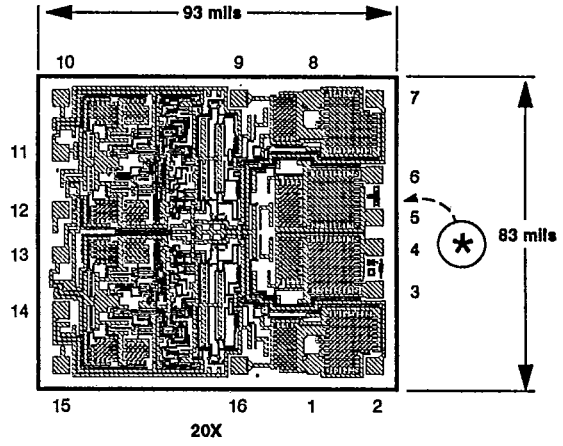

Pad No.	Function DG423/5	Function DG421
1	D_1	D_1
2	$\overline{WR}$	$\overline{WR}$
3	D_3	NC
4	S_3	NC
5	S_4	NC
6	D_4	NC
7	$\overline{RS}$	$\overline{RS}$
8	D_2	D_2
9	S_2	S_2
10	IN_2	IN_2
11	V+ (substrate)	V+ (substrate)
12	V_L	V_L
13	GND	GND
14	V-	V-
15	IN_1	IN_1
16	S_1	S_1

CSHD-I*

126 NMOS
114 PMOS
16 Capacitors
12 Diodes
12 Resistors

***A = DG421 or DG423**
B = DG421 or DG425

DG421/423/425

Siliconix incorporated

TYPICAL CHARACTERISTICS

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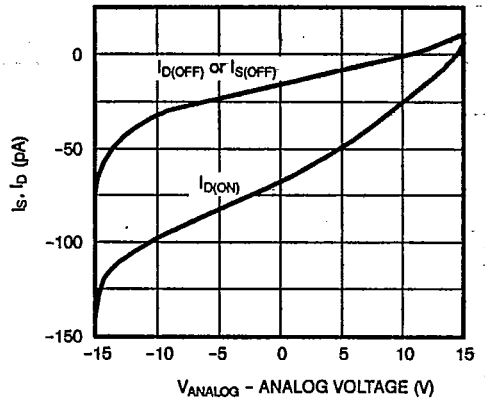
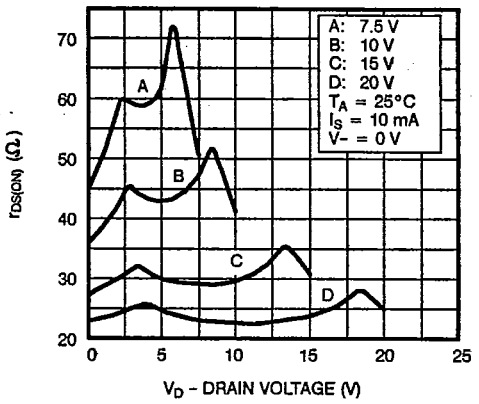
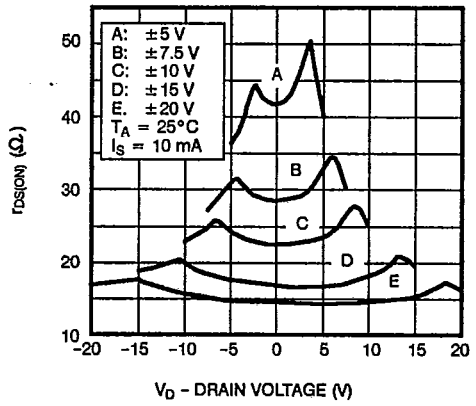
Leakage Currents vs. Analog Voltage



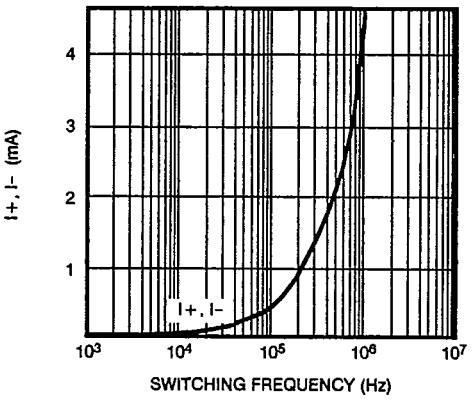
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



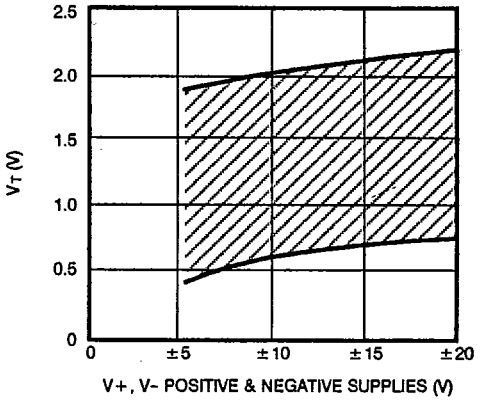
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



Supply Currents vs. Switching Frequency



Input Switching Threshold vs. V+ and V- Supply Voltages



TEST CIRCUITS

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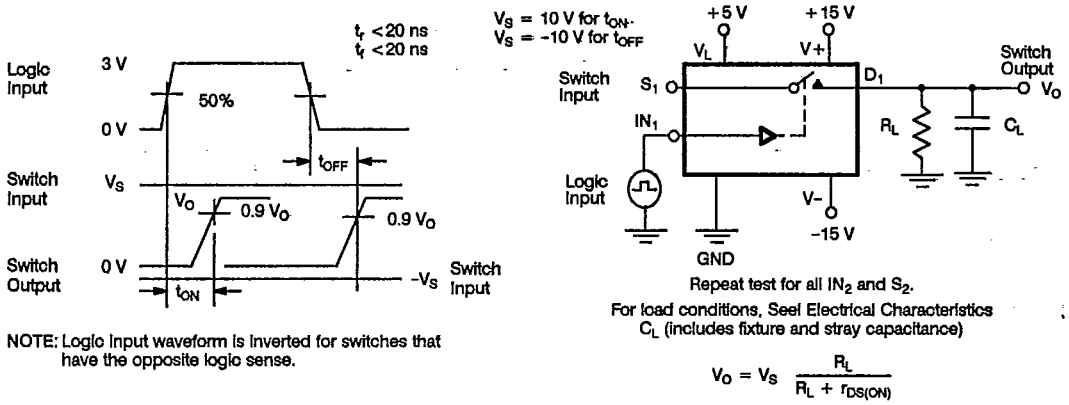
V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

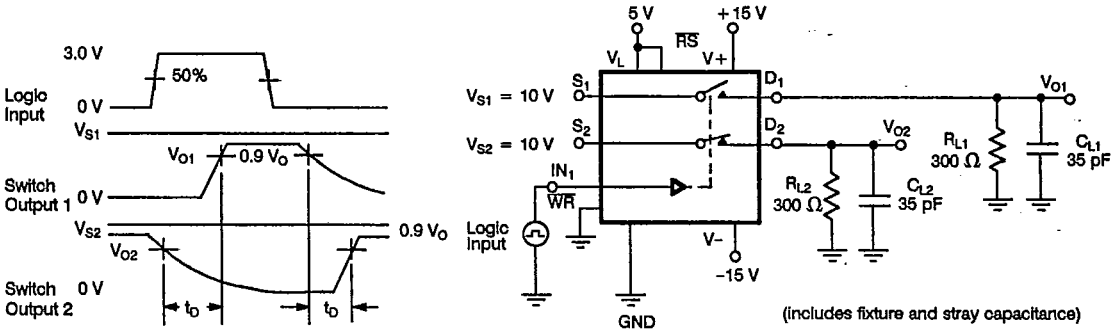


Figure 2. Break-Before-Make

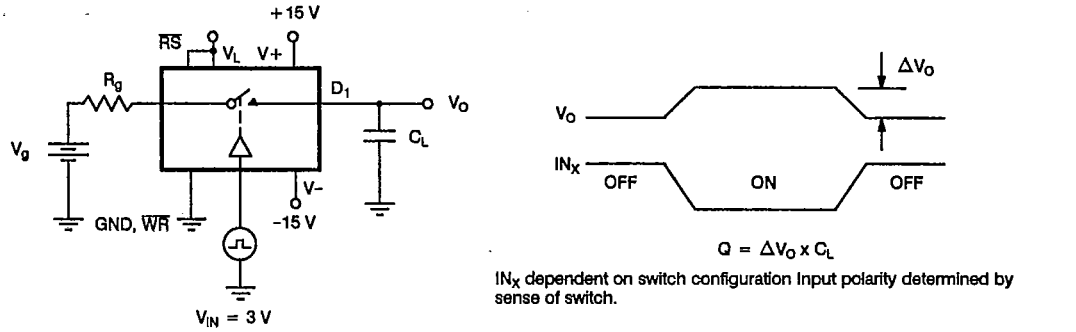


Figure 3. Charge Injection

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DG421/423/425

Siliconix incorporated

TEST CIRCUITS (Cont'd)

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Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

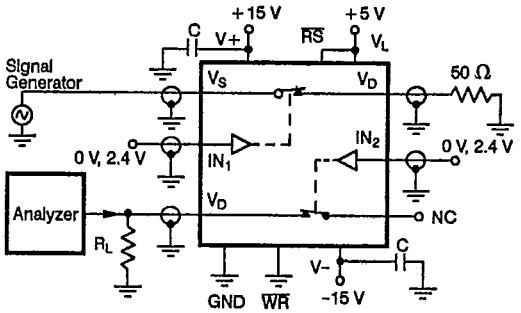


Figure 4. Crosstalk

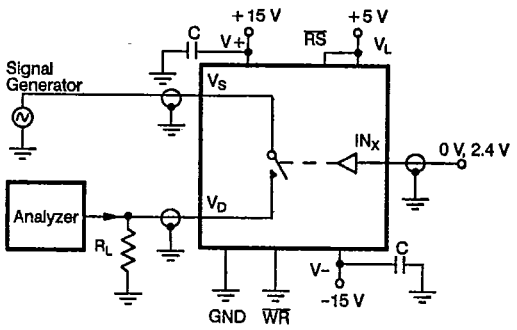


Figure 5. Off Isolation

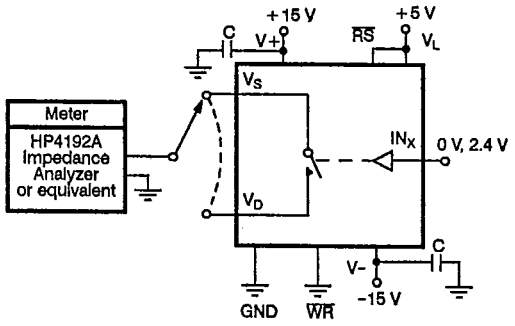


Figure 6. Source/Drain Capacitances

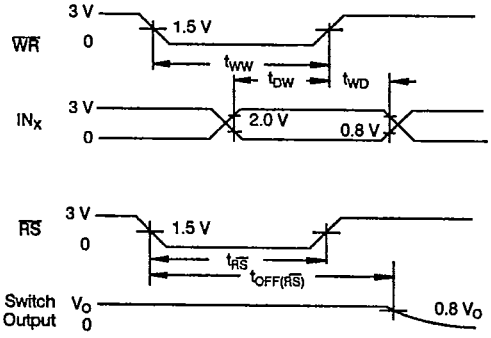


Figure 7. Latch Timing

BURN-IN CIRCUIT

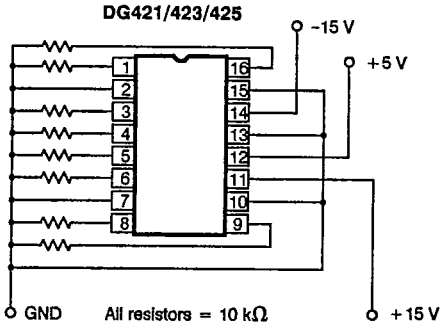
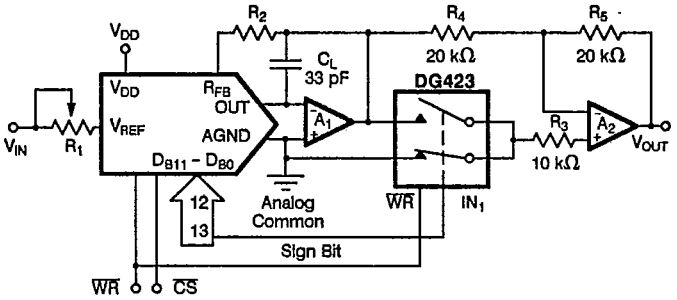


Figure 8.

Figure 9 shows a circuit configured to increase the effective resolution of the 12-bit DAC to 13 bits. The circuit operates with a sign plus magnitude code. A sign bit of "0" connects R_3 to GND, giving 12-bit resolution per quadrant.



12-Bit Plus Sign Magitude Code Table

Sign Bit	Digital Input MSB LSB	Analog Output (V_{OUT})
0	1111 1111 1111	+(4095/4096)V_{IN}
0	0000 0000 0000	0 Volts
1	0000 0000 0000	0 Volts
1	1111 1111 1111	+(4095/4096)V_{IN}

Figure 9. 12-Bit Plus Sign Magnitude D/A Converter

When switch S_1 of Figure 10 is closed, the op amp is placed in the familiar unity-gain non-inverting configuration. When switch S_2 is closed and S_1 is open the gain is given by:

$$Av = 1 + \frac{R_1}{R_2}$$

The microprocessor system $\overline{WR}$ must gate the decoder output to ensure proper timing.

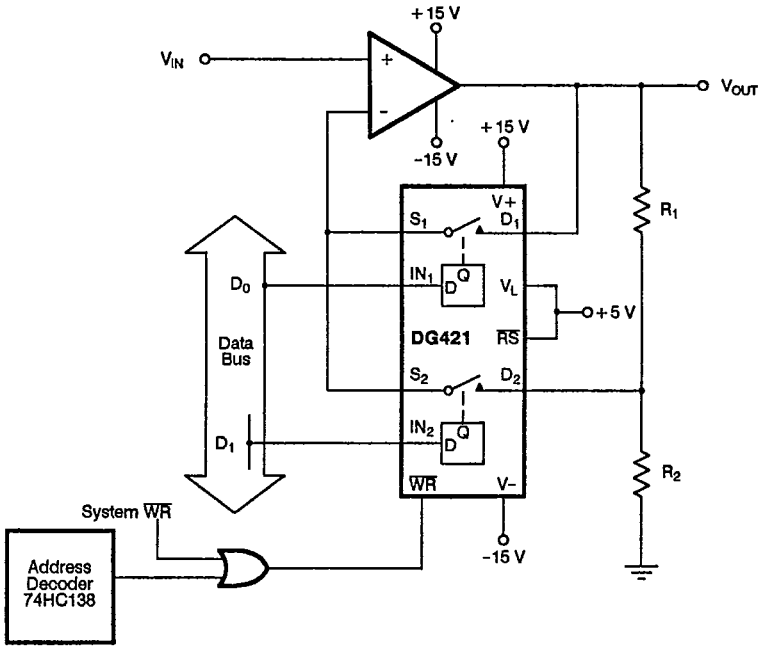


Figure 10. Bus-Controlled Precision Gain-Ranging Circuit

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DG421/423/425

Siliconix incorporated

APPLICATIONS (Cont'd)

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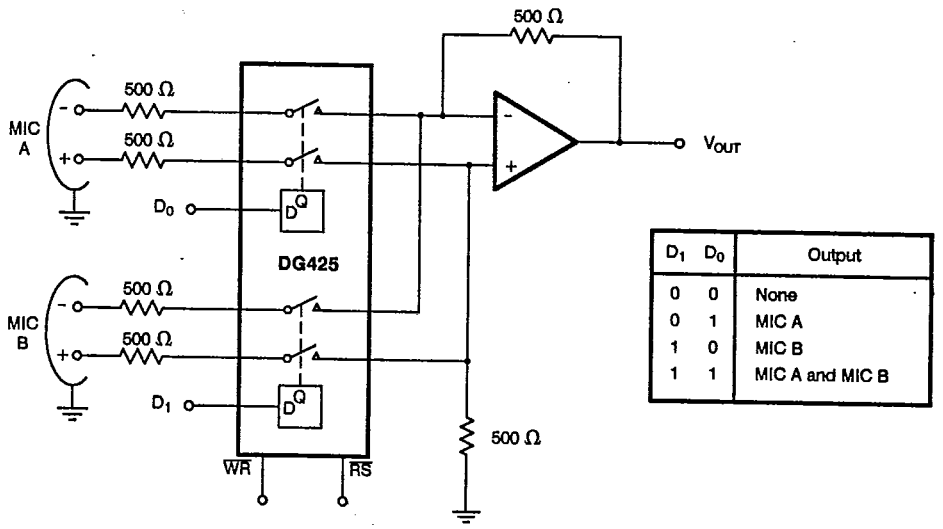
Figure 11 shows a balanced-line microphone input stage that provides selection or summing between two balanced-line microphones and also performs differential-to-single-ended conversion. Either MIC A or MIC B can be selected, and neither and/or both may be summed at the output. This configuration uses "virtual ground" switching, a method which minimizes distortion resulting from the analog switch on-resistance modulation. The actual voltage swings experienced by the analog switch barely exceed 1 V for a 15-V full-scale range input.



D_1	D_0	Output
0	0	None
0	1	MIC A
1	0	MIC B
1	1	MIC A and MIC B

Figure 11. Bus-Controlled Selector for Balanced-Line Microphones