

High Accuracy EPROM Programmable PLL Die for Crystal Oscillators

Features

- Erasable programmable read only memory (EPROM) - programmable die for in-package programming of crystal oscillators
- High resolution Phase locked loop (PLL) with 12-bit multiplier and 10-bit divider
- EPROM programmable capacitor tuning array with optional shadow register
- Twice programmable die
- Simple 2-wire programming interface
- On-chip oscillator runs from 10 MHz to 30 MHz fundamental tuned crystal
- EPROM-selectable Transistor transistor logic (TTL) or Complementary metal oxide semiconductor (CMOS) duty cycle levels
- Operating frequency:
 - 1 MHz to 133 MHz at 5 V
 - 1 MHz to 100 MHz at 3.3 V
 - 1 MHz to 66.6 MHz at 2.7 V
- Eight selectable post divide options, using PLL or reference oscillator output
- Programmable asynchronous or synchronous OE and power-down (PD#) modes(CY2037 and CY2037-2)
- Frequency select (CY2037-3)
- Low jitter outputs typically:
 - $< \pm 100$ ps (pk-pk) at 5 V and $f > 33$ MHz
 - $< \pm 125$ ps (pk-pk) at 3.3 V and $f > 33$ MHz
- 3.3 V or 5 V operation
- Small die
- Controlled rise and fall times and output slew rate

Table 1. Device Functionality: Output Frequencies

Parameter	Description	Condition	Min	Max	Unit
Fo	Output frequency	V _{DD} = 4.5 V to 5.5 V	1	133	MHz
		V _{DD} = 3.0 V to 3.6 V	1	100	MHz
		V _{DD} = 2.7 V to 3.0 V	1	66	MHz

Functional Description

CY2037 is an EPROM-programmable, high accuracy, PLL-based die designed for the crystal oscillator market. The die attaches directly to a low cost 10 to 30 MHz crystal and can be packaged into a 4-pin through-hole or surface mount packages. The oscillator devices may be stocked as blank parts and custom frequencies programmed in-package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

CY2037 contains an on-chip oscillator and a unique oscillator tuning circuit for fine-tuning of the output frequency. The crystal C_{load} may be selectively adjusted by programming a set of seven EPROM bits. This feature is used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

CY2037 uses EPROM programming with a simple 2-wire, 4-pin interface that includes V_{SS} and V_{DD}. Clock outputs may be generated up to 133 MHz at 5 V or up to 100 MHz at 3.3 V. The entire configuration can be reprogrammed once, which allows the programmed inventory to be altered or reused.

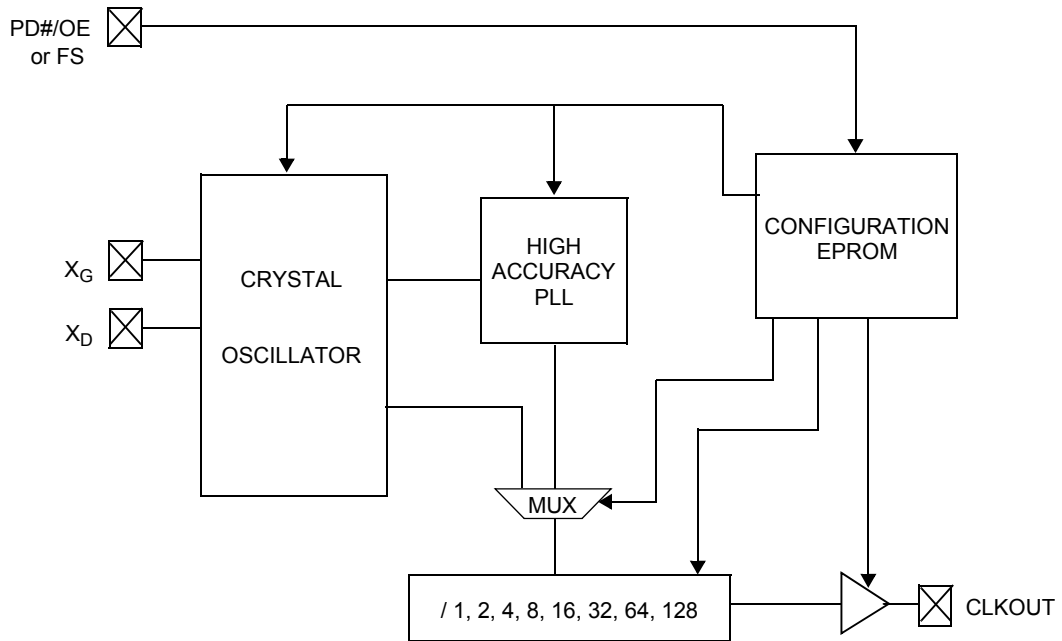
CY2037 PLL die is designed for very high resolution. It has a 12-bit feedback counter multiplier and a 10-bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM error. The clock is further modified by eight output divider options of 1, 2, 4, 8, 16, 32, 64, and 128. The divider input can be selected as the PLL or crystal oscillator output, providing a total of 16 separate output options. For further flexibility, the output is selectable between TTL and CMOS duty cycle levels.

CY2037 also contain flexible power management controls. These parts include both power down (PD#) and output enable (OE) features with integrated pull-up resistors. The PD# and OE modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal. When PD# or OE modes are enabled, CLKOUT is tri-stated and pulled low by a weak pull-down. In PD# mode, all active circuitry on chip get shutdown, where in OE mode PLL and oscillator remain operating.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable CY2037 to have low jitter and accurate outputs, making it suitable for most PC, networking, and consumer applications.

On the other hand, CY2037-3 contains a frequency select function in place of the power-down and output enable modes. For example, consumer products often require frequency compatibility with different electrical standards around the world. With this frequency select feature, a product that incorporates CY2037-3 could be compatible with both NTSC for North American, and PAL for Europe by simply changing the FS line. The twice programmable feature is absent in CY2037-3, because the second EPROM row is now being used for the alternate frequency.

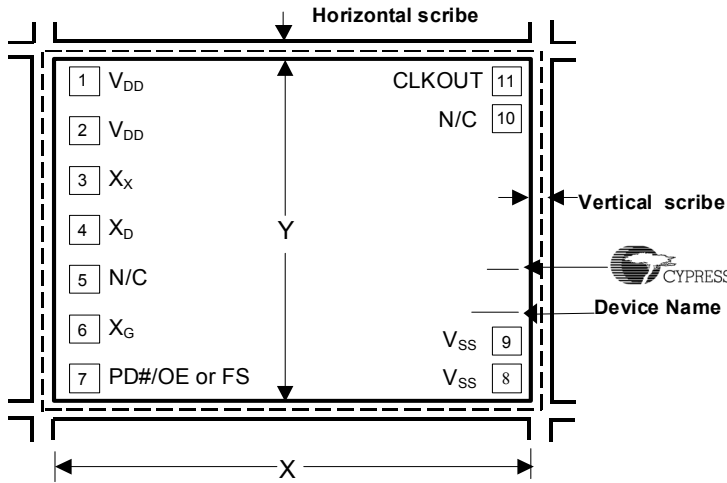
Logic Block Diagram



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Die Pad Description



Note:

Active die size:
 X = 55.9 mils / 1420.1 μ m
 Y = 40.9 mils / 1039.4 μ m
 Scribe:
 X (horizontal) = 3.1mils / 80 μ m
 Y (vertical) = 3.1 mils / 80 μ m
 Bond pad opening: 85 μ m x 85 μ m
 Pad pitch: 125 μ m x 125 μ m
 (pad center to pad center)
 Bottom side of Die can be connected to Vss or can be isolated. Do not connect to VDD.

Ordering Code	Device Name
CY2037EBWAF-IL	7C80383A
CY2037-2WAF-IL	7C80381A
CY2037-311WAF-IL	7C80340A

Die Pad Summary

Name	Die Pad	X Coordinate (μ m)	Y Coordinate (μ m)	Description
V _{DD}	1, 2	124.7	855.6, 731	Voltage supply
V _{SS}	8, 9	1291.35	99.6, 225.2	Ground
X _D	4	124.7	481.8	Crystal connection
X _X	3	124.7	606.4	No connect ^[1]
X _G	6	124.7	232.6	Crystal connection
PD#/OE or FS	7	124.7	108	CY2037 and CY2037-2: EPROM-programmable power-down or output enable pad CY2037-3: Frequency select. Serves as V _{PP} in programming mode for all devices
CLKOUT	11	1282.45	901.8	Clock output. Also serves as three-state input during programming.
N/C	5, 10	124.7, 1282.45	357.2, 769.4	No connect (so do not bond to these pads)

Note

1. For customers not bonding the X_D or X_G pad to external pins, an alternative bonding option would be shorting the X_x pad to the X_D pad.

EPROM Configuration Block

Table 2 summarizes the features that are configurable by EPROM. Refer “7C8038x/7C8034X Proprietary Specification” for further details. This specification can be obtained from your Cypress factory representative.

Table 2. EPROM Adjustable Features

Adjustable Features	
Adjust frequency	Feedback counter value (P)
	Reference counter value (Q)
	Output divider selection
Oscillator tuning (load capacitance values)	
Duty cycle levels (TTL or CMOS)	
Power management mode (OE or PD#)	
Power management timing (synchronous or asynchronous)	

PLL Output Frequency

CY2037 contains a high resolution PLL with 12-bit multiplier and 10-bit divider. The output frequency of the PLL is determined by the following formula:

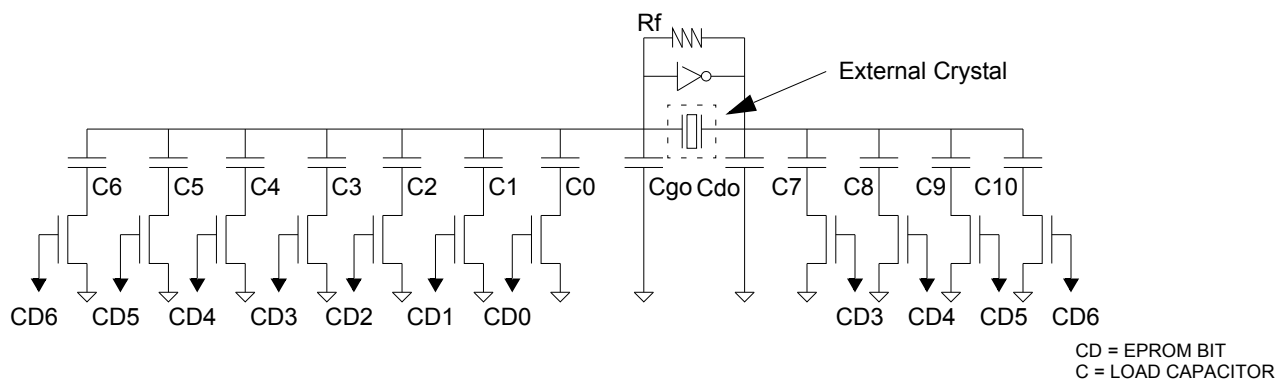
$$F_{PLL} = \frac{2 \cdot (P + 5)}{(Q + 2)} \cdot F_{REF}$$

In this formula, P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

Crystal Oscillator Tuning Circuit

CY2037 contains a unique tuning circuit to fine-tune the output frequency of the device. The tuning circuit consists of an array of eleven load capacitors on both sides of the oscillator drive inverter. The capacitor load values are EPROM-programmable and may be increased in small increments. As the capacitor load is increased the circuit is fine-tuned to a lower frequency. The capacitor load values vary from 0.17 pF to 8 pF for a 100:1 total control ratio. The tuning increments are shown in Table 3 on page 6. Refer to “7C8038x/7C8034x Proprietary Specification” for further details.

Figure 1. Crystal Oscillator Tuning Circuit



Power Management Features

CY2037 contains EPROM-programmable PD# and OE functions. If power-down (PD#) is selected, all active circuitry on the chip is shut down, output is tri-stated and pulled low by a weak pull-down when the control pin goes LOW. The weak pull-down is easily overdriven by another active CLKOUT for applications that require multiple CLKOUTs on a single signal path. The oscillator and PLL circuits must relock when the part leaves the power-down mode. If output enable (OE) mode is selected, the output is tri-stated and weakly pulled low when the control pin goes low. In this mode the oscillator and PLL circuits continue to operate, allowing a rapid return to normal operation when the control input is deasserted.

In addition, the PD# and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the power-down or output disable occurs immediately (allowing for logic delays), regardless of the position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before the power-down or output enable signal is initiated, thus preventing output glitches. In asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of the output.

Table 3. Crystal Oscillator Parameter

Parameter	Description	Min	Typ	Max	Unit
R _f	Feedback resistor, V _{DD} = 4.5 V to 5.5 V	0.5	2	3.5	MΩ
	Feedback resistor, V _{DD} = 2.7 V to 3.6 V	1.0	4	9.0	MΩ
Capacitors have ± 20% tolerance					
C _g	Gate capacitor	–	13	–	pF
C _d	Drain capacitor	–	9	–	pF
C ₀	Series capacitor	–	0.27	–	pF
C ₁	Series capacitor	–	0.52	–	pF
C ₂	Series capacitor	–	1.00	–	pF
C ₃	Series capacitor	–	0.7	–	pF
C ₄	Series capacitor	–	1.4	–	pF
C ₅	Series capacitor	–	2.6	–	pF
C ₆	Series capacitor	–	5.0	–	pF
C ₇	Series capacitor	–	0.45	–	pF
C ₈	Series capacitor	–	0.85	–	pF
C ₉	Series capacitor	–	1.7	–	pF
C ₁₀	Series capacitor	–	3.3	–	pF

CY2037 Vs CY2037-2

CY2037 contains a shadow register in addition to the EPROM register. The shadow register is an exact copy of the EPROM register and is the default register when the valid bit is not set. It is useful when the prototype or production environment calls for measuring and adjusting the CLKOUT frequency several times. Multiple adjustments can be performed with the shadow register. After the required frequency is achieved the EPROM register is permanently programmed.

Some production flows do not require the use of the shadow register. If this is the case, then CY2037-2 is the chosen device and CY2037-2 has a disabled shadow register. CY2037-3 contains the shadow register.

Frequency Select Feature of CY2037-3

CY2037-3 contains a frequency select function in place of the power-down and the output enable functions. With the frequency select feature, customers can switch two different frequencies that are configured in the two EPROM rows. Table 4 lists the definition of the frequency select pin (FS).

Table 4. Frequency Select Pin Decoding for CY2037-3

FS Pin	Output Frequency
0	From EPROM row 0 configuration
1	From EPROM row 1 configuration

Inkless Die Pick Map (DPM) Format

Cypress ships inkless wafers to customers with an accompanying die pick map, which is used to determine the good die for assembly and programming. Customers can also access individual DPM files at their convenience through ftp.cypress.com with a valid user account login and password. Contact your local Cypress Field Application Engineer (FAE) or sales representative for a customer FTP account. The DPM files are named with the fab lot number and wafer number scribed on the wafer. The DPM files are transferred to the customer's FTP account when the factory ships out the wafers against their purchase order (PO).

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.^[2]

Supply voltage -0.5 V to +7.0 V

Input voltage -0.5 V to $V_{DD} + 0.5$ V
 Storage temperature (non-condensing) 55 °C to +150 °C
 Junction temperature -40 °C to +100 °C
 Static discharge voltage 2000 V
 (per MIL-STD-883, method 3015)

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage (3.3 V)	2.7	3.6	V
	Supply voltage (5.0 V)	4.5	5.5	V
T_{AJ} ^[3]	Operating temperature, Junction	-10	+100	°C
C_{TTL}	Max. capacitive load on outputs for TTL levels $V_{DD} = 4.5$ V to 5.5 V, output frequency = 1 MHz to 40 MHz	-	50	pF
	$V_{DD} = 4.5$ V to 5.5 V, output frequency = 40 MHz to 133 MHz	-	25	pF
C_{CMOS}	Max. capacitive load on outputs for CMOS levels $V_{DD} = 4.5$ V to 5.5 V, output frequency = 1 MHz to 66.6 MHz	-	50	pF
	$V_{DD} = 4.5$ V to 5.5 V, output frequency = 66.6 MHz to 133 MHz	-	25	pF
	$V_{DD} = 3.0$ V to 3.6 V, output frequency = 1 MHz to 40 MHz	-	30	pF
	$V_{DD} = 3.0$ V to 3.6 V, output frequency = 40 MHz to 100 MHz	-	15	pF
	$V_{DD} = 2.7$ V to 3.0 V, output frequency = 1 MHz to 66 MHz	-	15	pF
X_{REF}	Reference frequency, input crystal. Fundamental tuned crystals only	10	30	MHz
t_{PU}	Power up time for all V_{DD} 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

Over the Operating Range^[4]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	$V_{DD} = 4.5$ V to 5.5 V	-	-	0.8	V
		$V_{DD} = 2.7$ V to 3.6 V	-	-	$0.2V_{DD}$	V
V_{IH}	High-level input voltage	$V_{DD} = 4.5$ V to 5.5 V	2.0	-	-	V
		$V_{DD} = 2.7$ V to 3.6 V	$0.7V_{DD}$	-	-	V
V_{OL}	Low-level output voltage	$V_{DD} = 4.5$ V to 5.5 V, $I_{OL} = 16$ mA	-	-	0.4	V
		$V_{DD} = 2.7$ V to 3.6 V, $I_{OL} = 8$ mA	-	-	0.4	V
V_{OHCMOS}	High-level output voltage, CMOS levels	$V_{DD} = 4.5$ V to 5.5 V, $I_{OH} = -16$ mA	$V_{DD} - 0.4$	-	-	V
		$V_{DD} = 2.7$ V to 3.6 V, $I_{OH} = -8$ mA	$V_{DD} - 0.4$	-	-	V
V_{OHTTL}	High-level output voltage, TTL levels	$V_{DD} = 4.5$ V to 5.5 V, $I_{OH} = -8$ mA	2.4	-	-	V
I_{IL}	Input low-current	$V_{IN} = 0$ V	-	-	10	μA
I_{IH}	Input high-current	$V_{IN} = V_{DD}$	-	-	5	μA
I_{DD}	Power supply current, Unloaded	$V_{DD} = 4.5$ V to 5.5 V, output frequency ≤ 133 MHz	-	-	45	mA
		$V_{DD} = 2.7$ V to 3.6 V, output frequency ≤ 100 MHz	-	-	25	mA
I_{DDS} ^[5]	Standby current	$V_{DD} = 2.7$ V to 3.6 V	-	10	50	μA
R_{UP}	Input pull-up resistor	$V_{DD} = 4.5$ V to 5.5 V, $V_{IN} = 0$ V	1.1	3.0	8.0	MΩ
		$V_{DD} = 4.5$ V to 5.5 V, $V_{IN} = 0.7 V_{DD}$	50	100	200	kΩ
I_{PD_CLKOUT}	CLKOUT pull-down current(OE or PD# mode)	$V_{DD} = 5.0$ V	-	20	-	μA

Notes

- Stresses greater than listed can impair the life of the device.
- This product is sold in die form so operating conditions are specified for the die, or junction temperature.
- This part was characterized in a 20-pin SOIC package with external crystal. Electrical Characteristics can change with other package types.
- If external reference is used, it is required to stop the reference (set reference to LOW) during power-down.

Output Clock Switching Characteristics

Over the Operating Range^[6]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t _{1w}	Output duty cycle at 1.4 V, V _{DD} = 4.5 V to 5.5 V t _{1w} = t _{1A} ÷ t _{1B} Figure 2 on page 9.	1 MHz to 40 MHz, C _L ≤ 50 pF 40 MHz to 66 MHz, C _L ≤ 15 pF 66 MHz to 125 MHz, C _L ≤ 25 pF 125 MHz to 133 MHz, C _L ≤ 15 pF	45 45 40 40	–	55 55 60 60	% % % %
t _{1x}	Output duty cycle at V _{DD} /2, V _{DD} = 4.5 V to 5.5 V t _{1x} = t _{1A} ÷ t _{1B} Figure 2 on page 9.	1 MHz to 66.6 MHz, C _L ≤ 25 pF 66.6 MHz to 125 MHz, C _L ≤ 25 pF 125 MHz to 133 MHz, C _L ≤ 15 pF	45 40 40	–	55 60 60	% % %
t _{1y}	Output duty cycle at V _{DD} /2, V _{DD} = 3.0 V to 3.6 V t _{1y} = t _{1A} ÷ t _{1B} Figure 2 on page 9.	1 MHz to 40 MHz, C _L ≤ 30 pF 40 MHz to 100 MHz, C _L ≤ 15 pF	45 40	–	55 60	% %
t _{1z}	Output duty cycle at V _{DD} /2, V _{DD} = 2.7 V to 3.0 V t _{1z} = t _{1A} ÷ t _{1B} Figure 2 on page 9.	1 MHz to 40 MHz, C _L ≤ 15 pF 40 MHz to 66.6 MHz, C _L ≤ 10 pF	40 40	–	60 60	% %
t ₂	Output clock rise time Figure 3 on page 9.	Between 0.8 V to 2.0 V, V _{DD} = 4.5 V to 5.5 V, C _L = 50 pF Between 0.8 V to 2.0 V, V _{DD} = 4.5 V to 5.5 V, C _L = 25 pF Between 0.8 V to 2.0 V, V _{DD} = 4.5 V to 5.5 V, C _L = 15 pF Between 0.2 V _{DD} to 0.8 V _{DD} , V _{DD} = 4.5 V to 5.5 V, C _L = 50 pF Between 0.2 V _{DD} to 0.8 V _{DD} , V _{DD} = 3.0 V to 3.6 V, C _L = 30 pF Between 0.2 V _{DD} to 0.8 V _{DD} , V _{DD} = 2.7 V to 3.6 V, C _L = 15 pF	–	–	1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t ₃	Output clock fall time Figure 3 on page 9.	Between 0.8 V to 2.0 V, V _{DD} = 4.5 V to 5.5 V, C _L = 50 pF Between 0.8 V to 2.0 V, V _{DD} = 4.5 V to 5.5 V, C _L = 25 pF Between 0.8 V to 2.0 V, V _{DD} = 4.5 V to 5.5 V, C _L = 15 pF Between 0.2 V _{DD} to 0.8 V _{DD} , V _{DD} = 4.5 V to 5.5 V, C _L = 50 pF Between 0.2 V _{DD} to 0.8 V _{DD} , V _{DD} = 3.0 V to 3.6 V, C _L = 30 pF Between 0.2 V _{DD} to 0.8 V _{DD} , V _{DD} = 2.7 V to 3.6 V, C _L = 15 pF	–	–	1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t ₄	Startup time out of power-down Figure 4 on page 9.	PD# pin LOW to HIGH ^[7]	–	1	2	ms
t _{5a}	Power-down delay time (synchronous setting) Figure 4 on page 9.	PD# pin LOW to output LOW (T = period of output clk)	–	T/2	T+10	ns
t _{5b}	Power-down delay time (asynchronous setting) Figure 4 on page 9.	PD# pin LOW to output LOW	–	10	15	ns
t ₆	Power-up time Figure 5 on page 10.	From power-on ^[7]	–	1	2	ms
t _{7a}	Output disable time (synchronous setting) Figure 6 on page 10.	OE pin LOW to output high Z (T = period of output clk)	–	T/2	T+10	ns

Notes

- 6. Not all parameters measured in production testing.
- 7. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70 ohms.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_{7b}	Output disable time (asynchronous setting) Figure 6 on page 10.	OE pin LOW to output high Z	–	10	15	ns
t_8	Output enable time (always synchronous enable) Figure 6 on page 10.	OE pin LOW to HIGH (T = period of output clk)	–	T	$1.5T + 25$	ns
t_9	Peak-to-peak period jitter Figure 7 on page 10.	$V_{DD} = 4.5\text{ V to }5.5\text{ V}, F_O > 33\text{ MHz}, VCO > 100\text{ MHz}$ $V_{DD} = 2.7\text{ V to }3.6\text{ V}, F_O > 33\text{ MHz}, VCO > 100\text{ MHz}$ $V_{DD} = 2.7\text{ V to }5.5\text{ V}, F_O < 33\text{ MHz}$	–	± 100 ± 125 ± 250	± 125 ± 200 1% of F_O	ps ps ps

Switching Waveforms

Figure 2. Duty Cycle Timing ($t_{1w}, t_{1x}, t_{1y}, t_{1z}$)

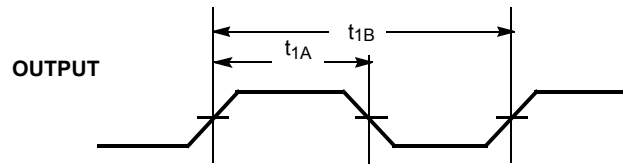


Figure 3. Output Rise/Fall Time

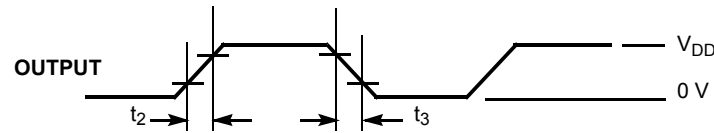
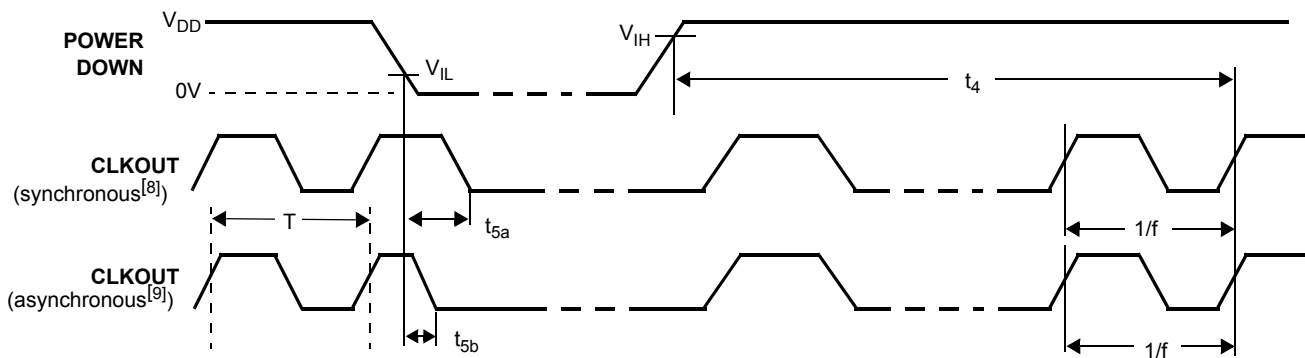


Figure 4. Power Down Timing (Synchronous and Asynchronous Modes)



Notes

- 8. In synchronous mode the power down or output tri-state is not initiated until the next falling edge of the output clock.
- 9. In asynchronous mode the power down or output tri-state occurs within 25 ns regardless of position in the output clock cycle.

Figure 5. Power-Up Timing

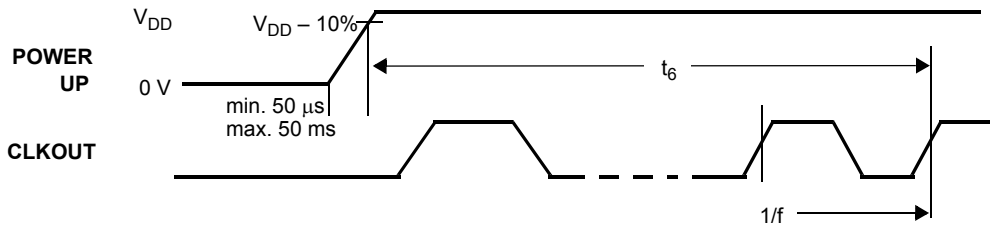


Figure 6. Output Enable Timing (Synchronous and Asynchronous Modes)

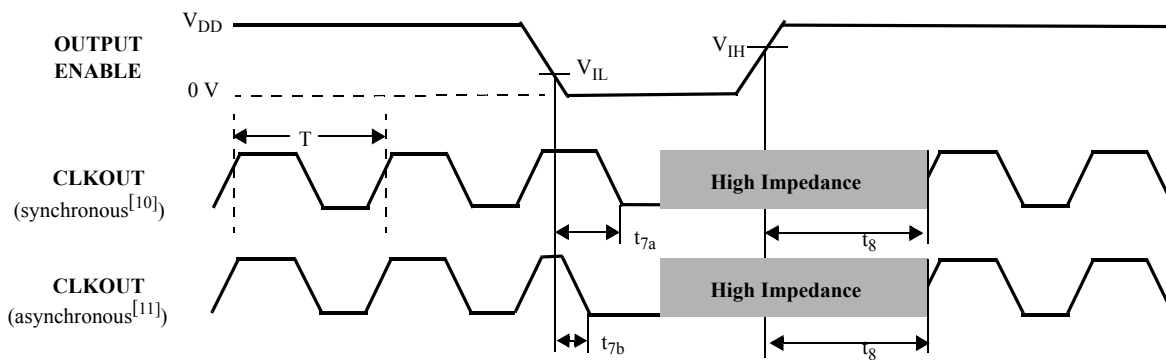
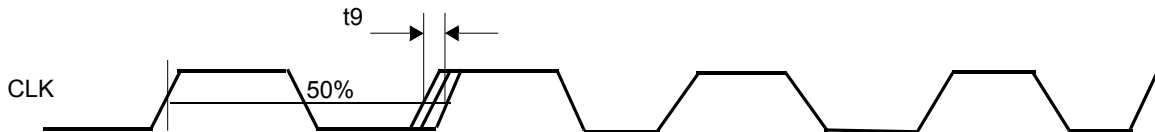


Figure 7. Period Jitter



Notes

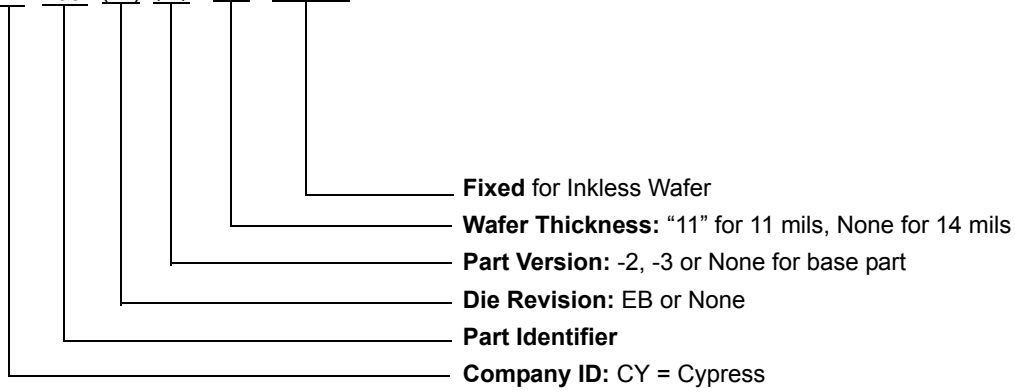
- 10. In synchronous mode the power down or output tri-state is not initiated until the next falling edge of the output clock.
- 11. In asynchronous mode the power down or output tri-state occurs within 25 ns regardless of position in the output clock cycle.

Ordering Information

Ordering Code	Type	Wafer Thickness	Operating Range
CY2037EBWAF-IL	Inkless wafer	14 ± 0.5 mils	-10 °C to 100 °C
CY2037-2WAF-IL	Inkless wafer	14 ± 0.5 mils	-10 °C to 100 °C
CY2037-311WAF-IL	Inkless wafer	11 ± 0.5 mils	-10 °C to 100 °C

Ordering Code Definitions

CY 2037 (xx) (-x) (xx) WAF-IL



Acronyms

Acronym	Description
CLKOUT	Clock output
CMOS	Complementary metal oxide semiconductor
DPM	Die pick map
EPROM	Erasable programmable read only memory
NTSC	National television system committee
OE	Output enable
PAL	Phase alternate line
PD	Power down
PLL	Phase locked loop
PPM	Parts per million
TTL	Transistor transistor logic

Reference Documents

Reference documents are available through your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

Document Number	Document Title	Description
71-00005	7C8038x/7C8034X proprietary specification	Appendix C contains programming specification for customer use

Document Conventions

Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	μW	micro Watts
dB	decibels	mA	milli Amperes
dBc/Hz	decibels relative to the carrier per Hertz	mm	milli meters
fC	femto Coulomb	ms	milli seconds
fF	femto Farads	mV	milli Volts
Hz	Hertz	nA	nano Amperes
KB	1024 bytes	ns	nano seconds
Kbit	1024 bits	nV	nano Volts
kHz	kilo Hertz	Ω	ohms
kΩ	kilo ohms	pA	pico Amperes
MHz	mega Hertz	pF	pico Farads
MΩ	mega Ohms	pp	peak-to-peak
μA	micro Amperes	ppm	parts per million
μF	micro Farads	ps	pico seconds
μH	micro Henrys	sps	samples per second
μs	micro seconds	σ	sigma: one standard deviation
μV	micro Volts		
μVrms	micro Volts root-mean-square		

Document History Page

Document Title: CY2037 High Accuracy EPROM Programmable PLL Die for Crystal Oscillators				
Document Number: 38-07354				
Revision	ECN	Orig. of Change	Submission date	Description of Change
**	112248	DSG	03/01/02	Change from Spec number: 38-00679 to 38-07354
*A	121857	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*B	291092	RGL	See ECN	Updated Min. Operating Temperature, Junction
*C	522769	RGL	See ECN	Added CY2037B information. Updated absolute maximum Junction temperature specification. Updated Ordering information table. Added Die Pad description and coordinates
*D	804376	RGL	See ECN	Minor Change: To post on web
*E	2192266	DPF/PYRS	See ECN	Added Inkless Die information.
*F	2748211	TSAL	08/10/09	Posting to external web.
*G	2761988	KVM	09/14/09	Add CY2037EBWAF-IL to Ordering Information table Remove obsolete part numbers: CY2037AWAF, CY2037-2WAF, CY2037-3WAF, CY2037-3WAF-IL. Removed Status column in Ordering Information table; replaced with footnotes
*H	2906472	CXQ	04/07/2010	Removed inactive part from Ordering Information table.
*I	3022612	BASH	09/03/2010	Post divider number corrected in "Feature" section from 16 to 8 on page 1. Removed all references of obsolete parts(CY2037A) and Benefits section from page 1.(CTI die scribe: X(horizontal)= 2.6 mils/65.6 um, Y(vertical)=3.0 mils/76.9 um) Die diagram on page 3 updated with Pad numbers, Scribe dimensions for TSMC part, Device name table, note for bottom side of die connection. "T" for Transistor removed from Figure 1 on page 4 as it is not mentioned in figure anywhere. Changed parameter name to I _{PD_CLOCKOUT} and clarified its description in Electrical Characterisitcs table on page 7. Added Figure 6 and 7 for OE and Period Jitter on page 9. Part numbers CY2037EB and CY2037-311 added in ordering infomation on page 9. Added Ordering code definitions, Acronyms, Reference documents and Document conventions.
*J	3069175	BASH	10/25/2010	Removing CY2037B from die pad description on page 4, ordering information and ordering code definitions.

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