Frequency Generator for Integrated Core Logic

Features

- Two copies of CPU clock
- Six copies of PCI Clock (Synchronous w/CPU clock)
- One Buffered copy of 14.318MHz input reference signal
- Supports 100MHz or 66MHz CPU operation
- Power management control input pins
- Low Frequency Test Mode
- Available in 28-pin SSOP (209 mil)

Key Specifications

Supply Voltages:

	VDDQ3 = 3.3V±5% VDDQ2 = 2.5V±5%
CPU0:1 Clock Skew:	175ps
CPU0:1 Clock Jitter:	200ps
PCI_F, PCI1:5 Clock Skew:	500ps
PCI_F, PCI1:5 Clock Jitter:	250ps
CPU to PCI Clock Skew:	1.5 - 4.0 ns (CPU Leads)
Output Duty Cycle:	45/55%
PCI_F, PCI Edge Rate:	≥1V/ns

CPU_STOP#, SEL, PCI_STOP#,PWR_DWN#: 250K ohm pull-up resistor

Figure 1 Block Diagram

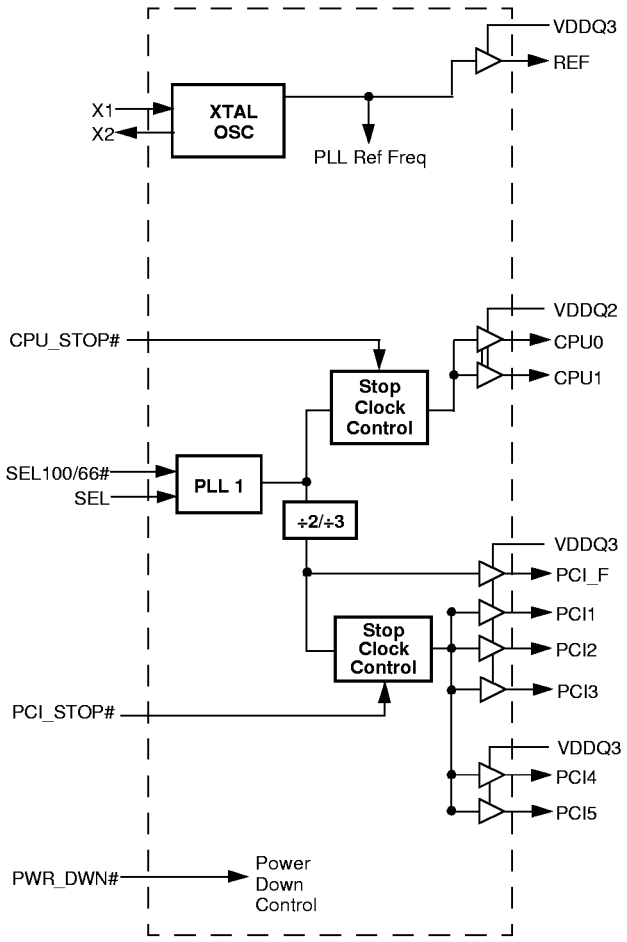


Table 1 Pin Selectable Frequency (Note)

SEL100/66#	SEL	CPU	PCI
0	0	HI-Z	HI-Z
0	1	66.6MHz	33.3
1	0	X1/2	X1/6
1	1	100MHz	33.3

Figure 2 Pin Diagram

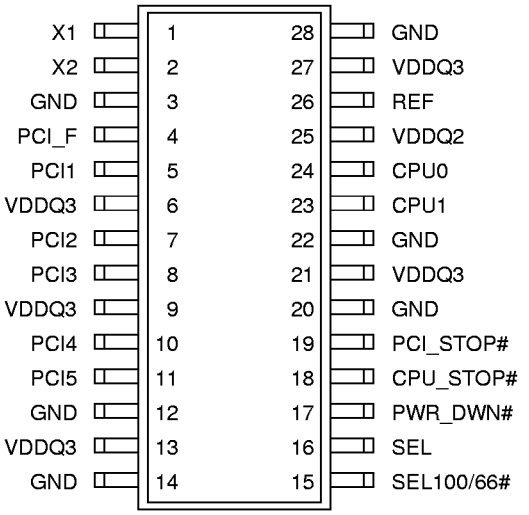


Table 2 Order Information

Part Number	Freq. Mask Code	Package
W48C111	-11	H = SSOP (209 mils)

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:1	24, 23	O	***CPU Clock Outputs 0 and 1:*** These two CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI1:5	5, 7, 8, 10, 11	O	***PCI Bus Clock Outputs 1 through 5:*** These five PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	4	O	***Fixed PCI Clock Output:*** Unlike PCICLK1:5 outputs, this output is not controlled by the PCI_STOP# control pin; it cannot be forced low by PCI_STOP#. Output voltage swing is controlled by voltage applied to VDDQ3.
CPU_STOP#	18	I	***CPU_STOP# input:*** When brought low, clock outputs CPU0:1 are stopped low after completing a full clock cycle (2-3 CPU clock latency). When brought high, clock outputs CPU0:1 start with a full clock cycle (2-3 CPU clock latency).
PCI_STOP#	19	I	***PCI_STOP# input:*** The PCI_STOP# input enables the PCICLK1:5 outputs when high and causes them to remain at logic 0 when low. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effect takes place on the next PCI_F clock cycle.
REF	26	O	***Fixed 14.318MHz Output:*** Used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3.
SEL100/66#	15, 16	I	***Frequency Selection Inputs:*** Select power-up default CPU clock frequency as shown in Table 1 on page 1.
X1	1	I	***Crystal Connection or External Reference Frequency Input:*** This pin can either be used as a connection to a crystal or to a reference signal.
X2	2	I	***Crystal Connection:*** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
PWR_DWN#	17	I	***Power Down Control:*** When this input is low, device goes into a low power standby condition. All outputs are held low. CPU and PCI clock outputs are stopped low after completing a full clock cycle (2-3 CPU clock cycle latency). When brought high, CPU and PCI outputs start with a full clock cycle at full operating frequency (3ms maximum latency).
VDDQ3	6, 9,13,21,27	P	***Power Connection:*** Connected to 3.3V.
VDDQ2	25	P	***Power Connection:*** Power supply for CPU0:1 output buffer. Connected to 2.5V.
GND	3, 12, 14, 20, 22, 28	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

DC Electrical Characteristics:

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
Supply Current							
I_{DD}	Combined 3.3V Supply Current				80	mA	CPU0:1 = 100MHz Outputs Loaded (Note 1)
I_{DD2}	2.5V Supply Current				40		
Logic Inputs							
V_{IL}	Input Low Voltage		GND -.3		0.8	V	
V_{IH}	Input High Voltage		2.0		VDD +.3	V	
I_{IL}	Input Low Current (Note 2)				-25	µA	
I_{IH}	Input High Current (Note 2)				10	µA	
I_{IL}	Input Low Current (SEL100/66#)				-5	µA	
I_{IH}	Input High Current (SEL100/66#)				+5	µA	
Clock Outputs							
V_{OH}	Output High Voltage	CPU0:1	2.2			V	I_{OH} = –1mA
V_{OL}	Output Low Voltage				50	mV	I_{OL} = 1mA
V_{OH}	Output High Voltage		3.1			V	I_{OH} = –1mA
I_{OL}	Output Low Current:	CPU0:1	55	115	190	mA	V_{OL} = 1.25V
		PCI_F, PCI1:5	20.5	53	139	mA	V_{OL} = 1.5V
		REF	25	37	76	mA	V_{OL} = 1.5V
I_{OH}	Output High Current	CPU0:1	50	110	195	mA	V_{OH} = 1.25V
		PCI_F, PCI1:5	31	55	189	mA	V_{OH} = 1.5V
		REF	27	44	94	mA	V_{OH} = 1.5V
Crystal Oscillator							
V_{TH}	X1 Input threshold Voltage (Note 3)			1.65		V	VDDQ# = 3.3V

DC Electrical Characteristics: (cont.)

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
C_{LOAD}	Load Capacitance, As seen by External Crystal (Note 4)		14		pF	
$C_{IN,X1}$	X1 Input Capacitance (Note 5)		28		pF	Pin X2 unconnected
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance			5	pF	Except X1 and X2
C_{OUT}	Output Pin Capacitance			6	pF	
L_{IN}	Input Pin Inductance			7	nH	

Notes:
1. All clock outputs loaded with 6 " 60 ohm transmission lines with 20 pF capacitors.
2. CPU_STOP#, PCI_STOP#, PWR_DWN#, and SEL logic inputs have internal pull-up resistors except SEL100/66# (not CMOS level).
3. X1 input threshold voltage (typical) is VDDQ3/2.
4. The W48C111-11 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics:

T_A = 0°C to +70°C; VDDQ21 = 3.3V±5%; VDDQ2 = 2.5V±5%f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.6MHz			CPU = 100MHz			Unit	Test Condition/Comments
		Min	Typ	Max	Min	Typ	Max		
t_P	Period	15		15.5	10		10.5	ns	Measured on rising edge at 1.25.
t_H	High Time	5.2			3.0			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5.0			2.8			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			200			200	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			175			175	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		13.5			13.5		ohm	Average value during switching transition. Used for determining series termination value

PCI Clock Outputs, PCI1:5 and PCI_F (Lump Capacitance Test Load = 30pF)

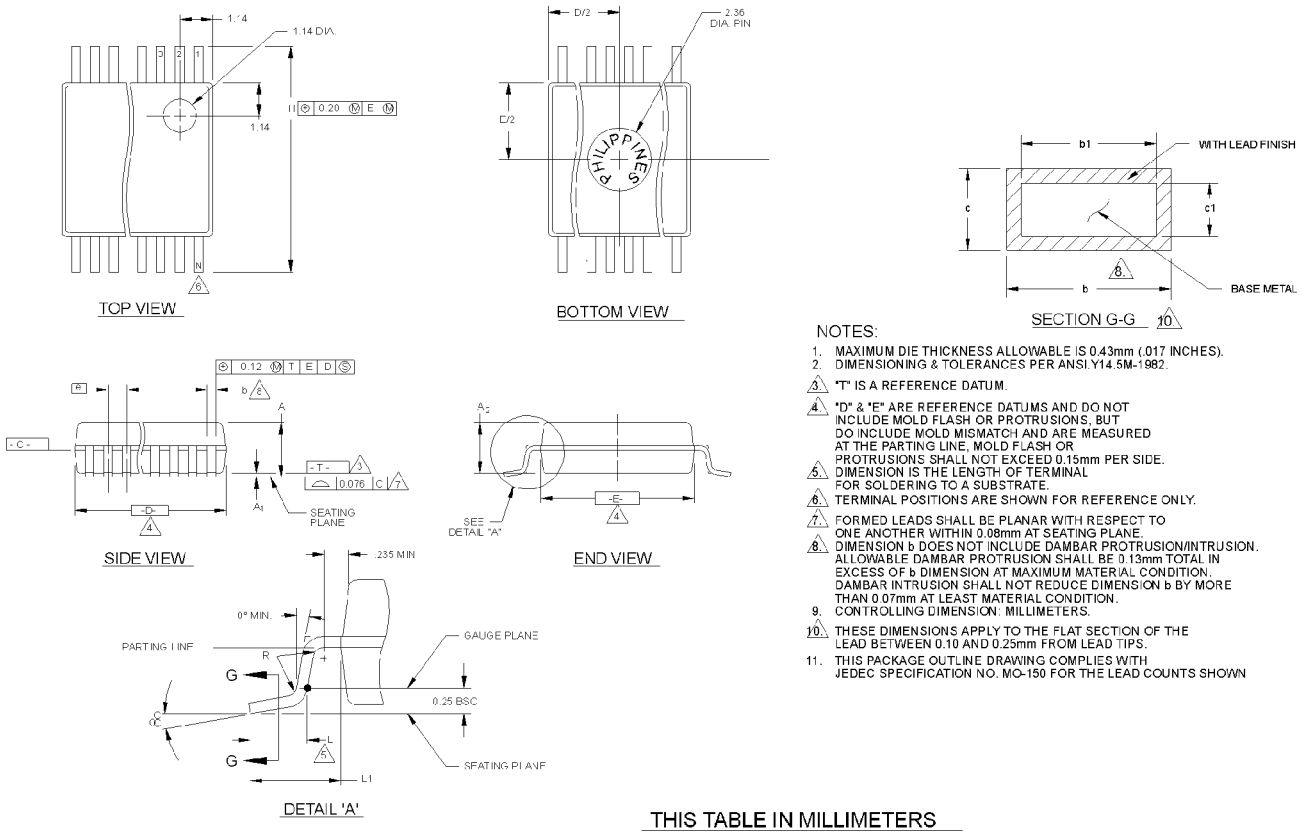
Symbol	Parameter	CPU = 66.6/100MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
t_P	Period	30			ns	Measured on rising edge at 1.5V.
t_H	High Time	12.0			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			500	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1.5		4.0	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

REF Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition/Comments
f	Frequency, Actual		14.318		MHz	Determined by crystal oscillator frequency
t_R	Output Rise Edge Rate	1.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		30		ohm	Average value during switching transition. Used for determining series termination value.

Mechanical Package Outline

Figure 3 28-Pin Small Shrink Outline Package (SSOP, 209 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A_1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A_2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
α	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.068	.073	.078		AA	.239	.244	.249	14
A_1	.002	.005	.008		AB	.239	.244	.249	16
A_2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
α	0°	4°	8°						
R	.004	.006							