DATA SHEET

74ALVT16260

12-bit to 24-bit multiplexed D-type latches (3-State)

Product specification
IC23 Data Handbook

1998 Jan 30

Philips
Semiconductors

PHILIPS

2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

74ALVT16260

FEATURES

- ESD protection exceeds 2000V per Mil-Std-883C, Method 3015; exceeds 200V using machine model
- Latch-up protection exceeds 500mA per JEDEC Standard JESD-17.
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise.
- Output capability (–32mA I_{OH}, 64mA I_{OL}).
- Bus hold inputs eliminate the need for external pull-up resistors.
- 5V I/O compatible
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ALVT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is alto useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is high, the latch is transparent. When the latch enable input goes low, the data present at the inputs is latched and remains latched until the latch enable input is returned high.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The 74ALVT16260 is available in a 56-pin Shrink Small Outline Package (SSOP) and 56-pin Thin Shrink Small Outline Package (TSSOP).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH}	Propagation delay	C_L = 50 pF	3.5	2.8	ns
t_{PHL}	nAx to nBx nBx to nAx		3.3	2.6	
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	4	pF
C_{OUT}	Output capacitance	$V_{I/O}$ = 0 V or 5.0 V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	100	80	µA

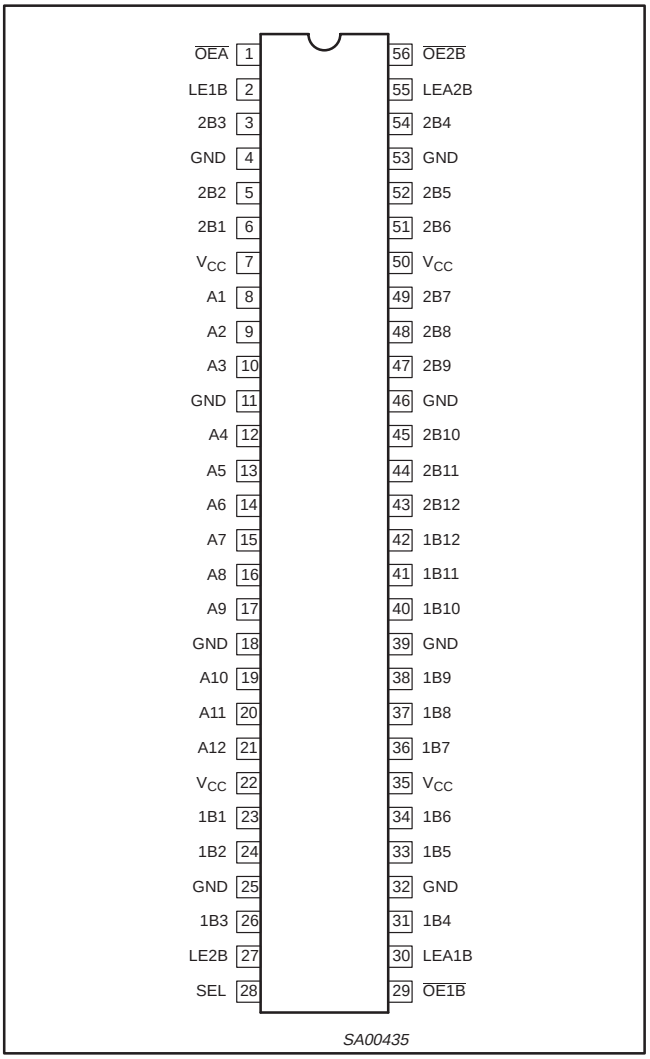
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16260 DL	AV16260 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16260 DGG	AV16260 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21	An	Data inputs/outputs (A)
23, 24, 26, 31, 33, 34, 36, 37, 38, 40, 41, 42	1Bn	Data inputs/outputs (B1)
6, 5, 3, 54, 52, 51, 49, 48, 47, 45, 44, 43	2Bn	Data inputs/outputs (B2)
1, 29, 56	$\overline{OEA}$, $\overline{OE1B}$, $\overline{OE2B}$	Output enable input (active low)
2, 27, 30, 55	LE1B, LE2B, LEA1B, LEA2B	Latch enable inputs
28	SEL	B1/B2 input select input
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION



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FUNCTION TABLES

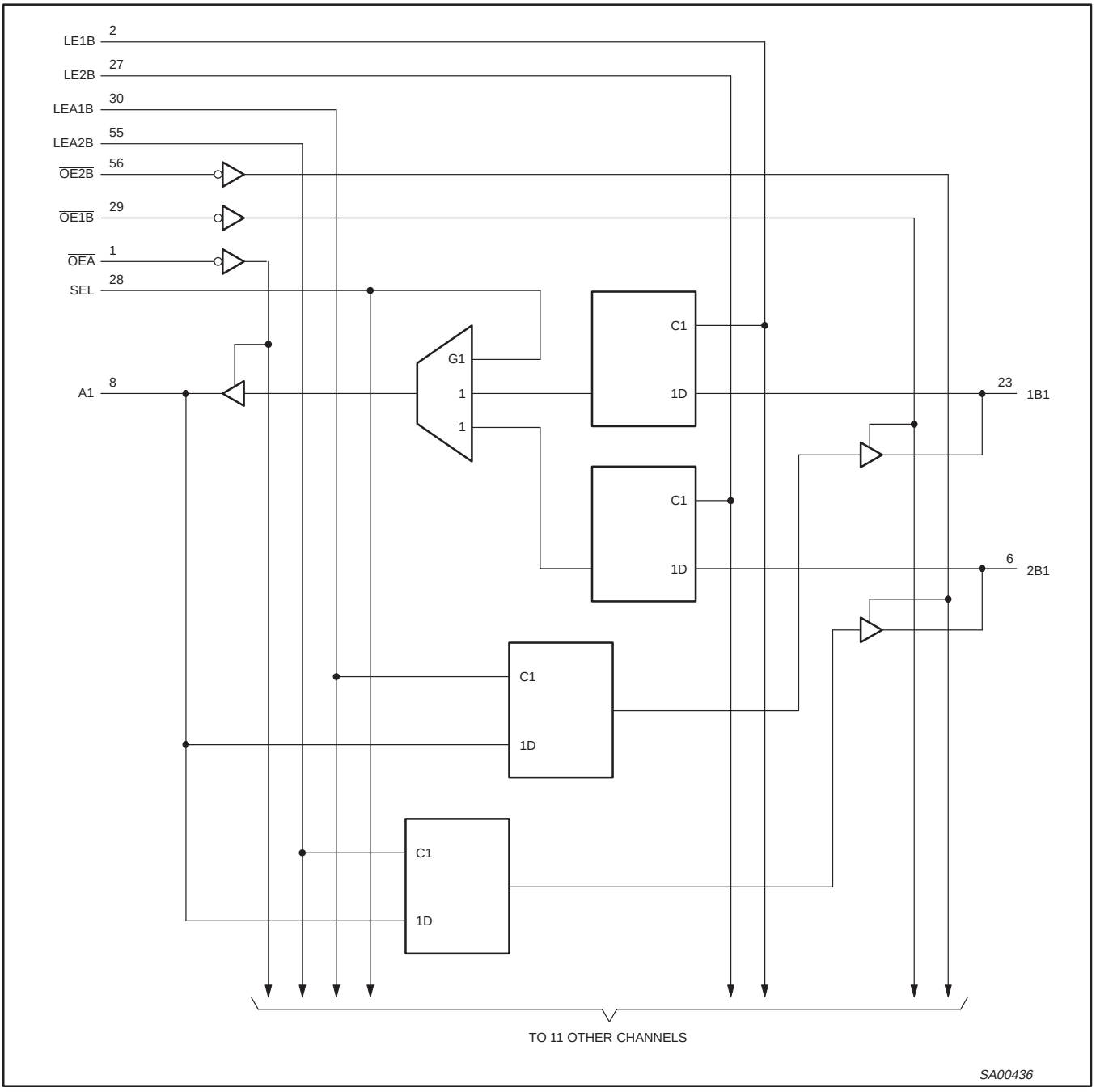
B to A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A0
X	X	X	X	X	H	Z

A to B ($\overline{OEA}$ = H)

INPUTS					OUTPUT	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B0
L	H	L	L	L	L	2B0
H	L	H	L	L	1B0	H
L	L	H	L	L	1B0	L
X	L	L	L	L	1B0	2B0
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.7	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER		T_{amb} = –40°C to +85°C V_{CC} = +3.3V ± 0.3V			UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	
t_{PLH}	A or B	B or A	1	2.8	4.8	ns
t_{PHL}			1	2.6	4.6	ns
t_{PLH}	$\overline{LE}$	A or B	1.1	2.9	4.6	ns
t_{PHL}			1.1	3.1	4.7	ns
t_{PLH}	SEL (B1)	A	1.3	2.3	3.4	ns
	SEL (B2)	A	1.1	2.4	3.8	ns
t_{PHL}	SEL (B1)	A	1.5	2.4	3.6	ns
	SEL (B2)	A	1.6	2.4	3.6	ns
t_{PZH}	$\overline{OE}$	A or B	1	2.3	4.2	ns
t_{PZL}			1.6	2.3	4.0	ns
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.4	6.0	ns
t_{PLZ}			1.3	3.1	5.0	ns

AC SETUP CHARACTERISTICS (3.3V ± 0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	T_{amb} = –40°C to +85°C V_{CC} = +3.3V ± 0.3V		UNIT
		MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.7	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER		T_{amb} = –40°C to +85°C V_{CC} = +2.5V ± 0.2V			UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	
t_{PLH}	A or B	B or A	1	3.5	5.3	ns
t_{PHL}			1	3.3	5.4	ns
t_{PLH}	$\overline{LE}$	A or B	1.1	3.9	6.0	ns
t_{PHL}			1.1	4.2	6.2	ns
t_{PLH}	SEL (B1)	A	1.3	2.9	4.5	ns
	SEL (B2)	A	1.1	3.3	4.8	ns
t_{PHL}	SEL (B1)	A	1.5	3.0	4.5	ns
	SEL (B2)	A	1.6	3.2	4.6	ns
t_{PZH}	$\overline{OE}$	A or B	1	3.1	5.0	ns
t_{PZL}			1.6	2.0	3.0	ns
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.0	6.6	ns
t_{PLZ}			1.3	2.0	3.4	ns

AC SETUP CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	T_{amb} = –40°C to +85°C V_{CC} = +2.5V ± 0.2V		UNIT
		MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		ns

AC WAVEFORMS

V_M = 1.5V for all waveforms

The outputs are measured one at a time with one transition per measurement.

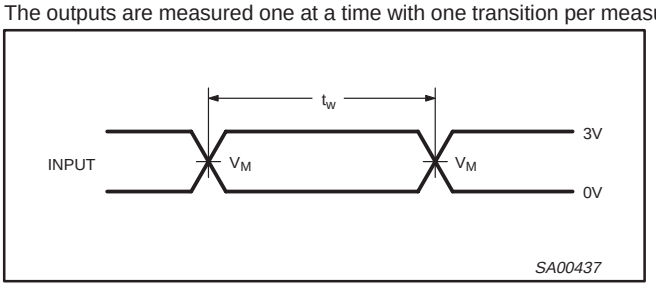


Figure 1. Pulse duration

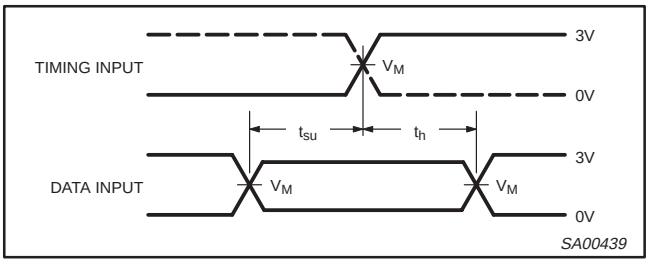
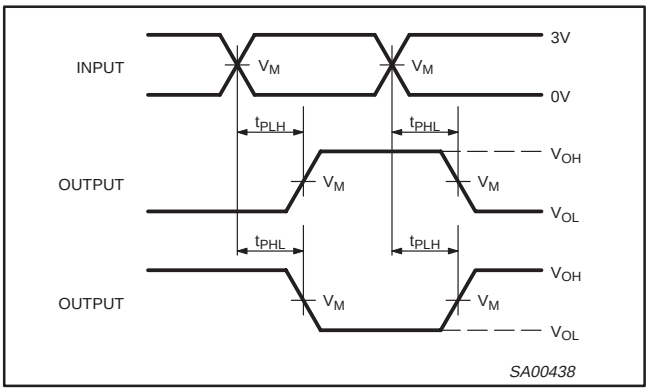
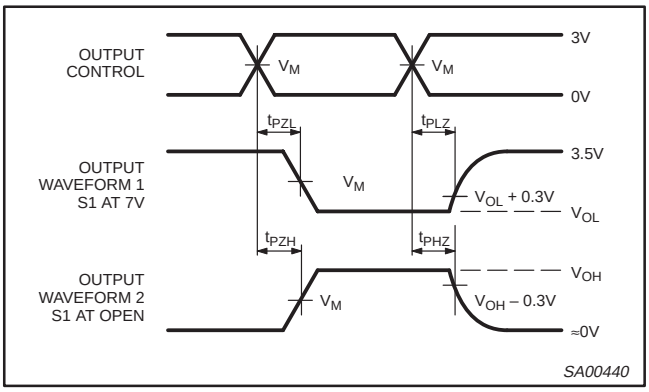


Figure 3. Setup and hold times



All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r ≤ 2.5ns, t_f ≤ 2.5ns.

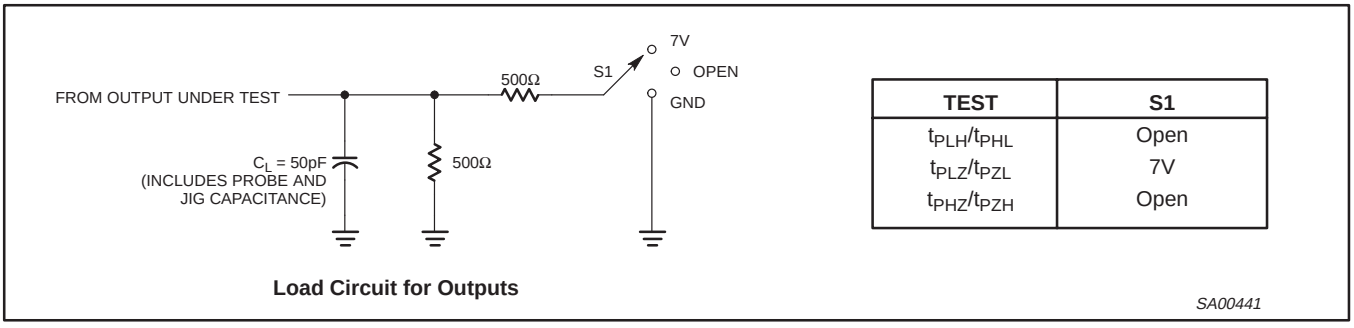
Figure 2. Propagation delay times; inverting and non-inverting outputs



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 4. Enable and disable times; low- and high-level enabling

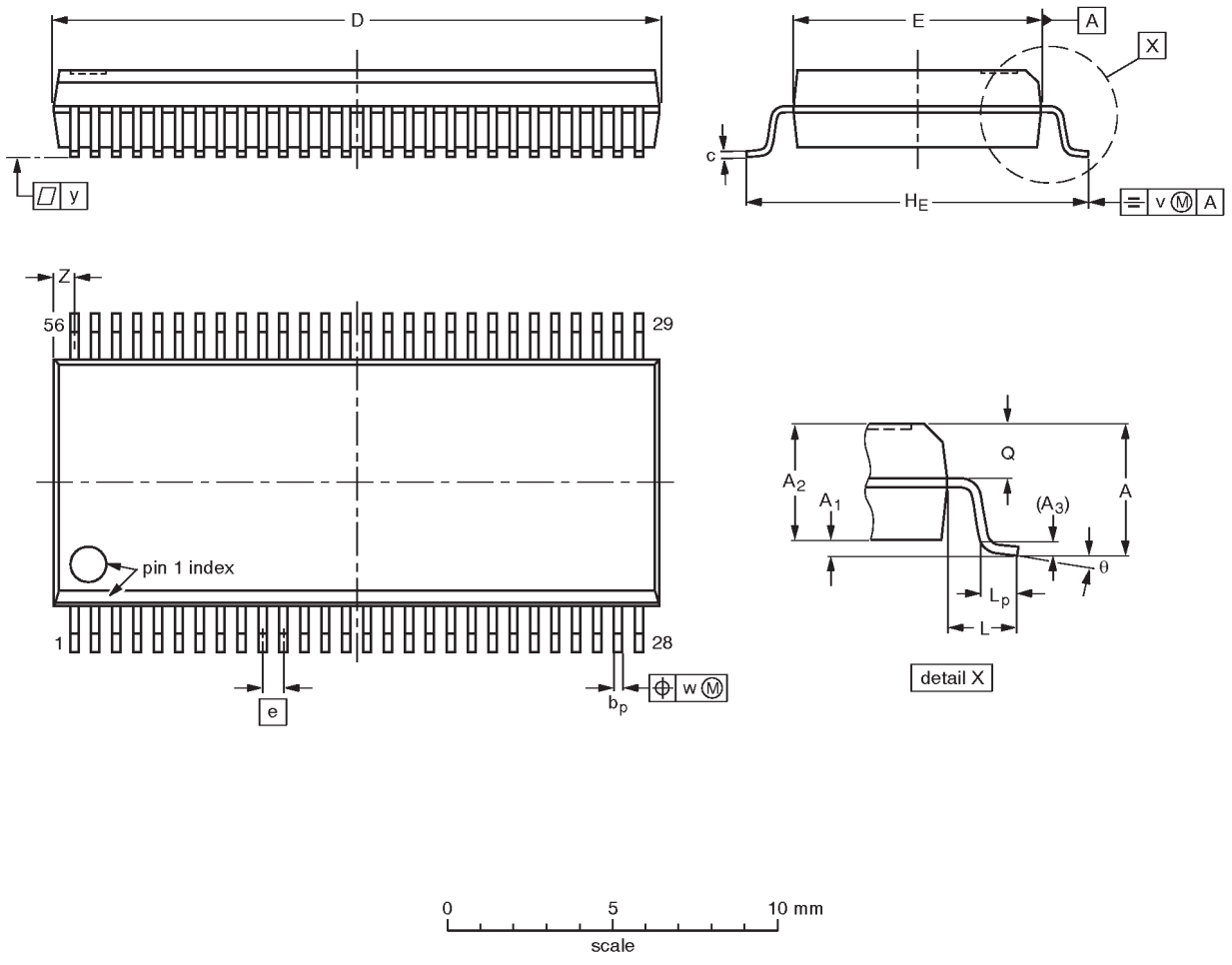
TEST LOAD CIRCUIT



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7V
t_{PHZ}/t_{PZH}	Open

Figure 5. Test load circuit

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

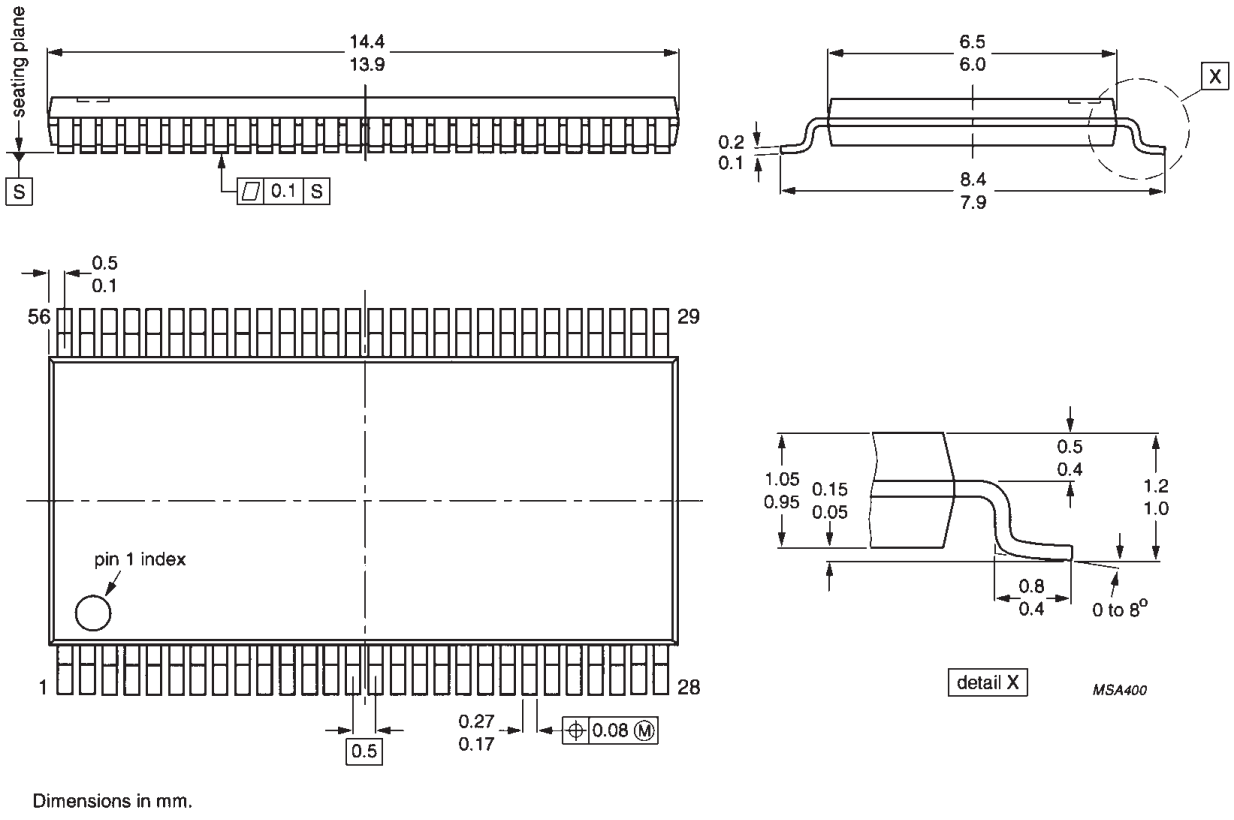
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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74ALVT16260; 12-bit to 24-bit multiplexed D-type latches (3-State)

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- Products
- MultiMarket Semiconductors
- Product Selector
- Catalog by Function
- Catalog by System
- Cross-reference
- Packages
- End of Life information
- Distributors Go Here!
- Models
- SoC solutions

General description | Features | Applications | Datasheet
Block diagram | Buy online | Support & tools | Email/translate
Products & packages | Parametrics | Similar products

General description

The 74ALVT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is alto useful in memory-interleaving applications.

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. The OE1B and OE2B control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is high, the latch is transparent. When the latch enable input goes low, the data present at the inputs is latched and remains latched until the latch enable input is returned high.

To ensure the high-impedance state during power-up or power-down, OE should be tied to V_{cc} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The 74ALVT16260 is available in a 56-pin Shrink Small Outline Package (SSOP) and 56-pin Thin Shrink Small Outline Package (TSSOP).

Features

- ESD protection exceeds 2000V per Mil-Std-883C, Method 3015; exceeds 200V using machine model
- Latch-up protection exceeds 500mA per JEDEC Standard JESD-17.
- Distributed V_{cc} and GND pin configuration minimizes high-speed switching noise.
- Output capability (-32mA I_{OH} , 64mA I_{OL}).
- Bus hold inputs eliminate the need for external pull-up resistors.
- 5V I/O compatible
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset

Applications

AN203_2: Test Fixtures for High Speed Logic (date 02-Apr-98)
AN214_2: 74F extended octal-plus family applications (date 01-Jun-88)
AN215_2: 74FXXXX Light Load input products (date 01-Apr-88)
AN220_1: Synchronizing and clock driving solutions - using the 74F50XXX family (date 01-Sep-89)
AN2301: Simulation Support for Philips' Advanced BiCMOS Products
AN240: Interfacing 3 Volt and 5 Volt Applications
AN243: LVT (Low Voltage Technology) and ALVT (Advanced LVT) (date 01-Jan-98)
AN246: Transmission Lines and Terminations with Philips Advanced Logic Families

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74ALVT16260	12-bit to 24-bit multiplexed D-type latches (3-State)	1/30/1998	Product specification	14	101	Download

Blockdiagram(s)

Block diagram of 74ALVT16260DGG

Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74ALVT16260DGG	SOT364-1 (TSSOP56)	2.5/3.3V 12-Bit to 24-Bit Multiplexed D-Type Latch with Bus Hold (3-State)	4~6	Low	56	None	TTL	High
74ALVT16260DL	SOT371-1 (SSOP56)	2.5/3.3V 12-Bit to 24-Bit Multiplexed D-Type Latch with Bus Hold (3-State)	4~6	Low	56	None	TTL	High

Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing IC packing info	Package	Device status	Buy online
74ALVT16260DGG	74ALVT16260DG	9352 603 44112	Standard Marking * Tube	SOT364-1 (TSSOP56)	Full production	order this -
	74ALVT16260DG-T	9352 603 44118	Standard Marking * Reel Pack, SMD, 13"	SOT364-1 (TSSOP56)	Full production	order this -
74ALVT16260DL	74ALVT16260DL	9352 603 45112	Standard Marking * Tube	SOT371-1 (SSOP56)	Full production	order this -
	74ALVT16260DL-T	9352 603 45118	Standard Marking * Reel Pack, SMD, 13"	SOT371-1 (SSOP56)	Full production	order this -

Similar products

74ALVT16260 links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

- Innovative Low Voltage Logic Solutions(date 01-Aug-00)
- Introduction to Advanced BiCMOS Logic Products(date 01-Mar-98)
- Family specifications ALVT16, family characteristics(date 01-Mar-98)
- Introduction to Advanced Low-Voltage Technology(date 01-Mar-98)
- Advanced BiCMOS features(date 01-Jan-98)

Email/translate this product information

- Email this product information.
- Translate this product information page from English to:

French Translate

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