# 256K x 36, 512K x 18
# 2.5V Synchronous ZBT™ SRAMs
# 2.5V I/O, Burst Counter
# Flow-Through Outputs

***Preliminary***
***IDT71T657***
***IDT71T659***

## Features

- **256K x 36, 512K x 18 memory configurations**
- **Supports high performance system speed - 100 MHz (7.5 ns Clock-to-Data Access)**
- **ZBT™ Feature - No dead cycles between write and read cycles**
- **Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$**
- **Single R/$\overline{W}$ (READ/WRITE) control pin**
- **4-word burst capability (Interleaved or linear)**
- **Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)**
- **Three chip enables for simple depth expansion**
- **2.5V power supply (±5%)**
- **2.5V (±5%) I/O Supply ($V_{DDQ}$)**
- **Packaged in a JEDEC standard 100-lead plastic thin quad flatpack (TQFP) and 119-lead ball grid array (BGA).**

## Description

The IDT71T657/59 are 2.5V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMs organized as 256K x 36 / 512K x 18. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and on the next clock cycle the associated data cycle occurs, be it read or write.

The IDT71T657/59 contain address, data-in and control signal registers. The outputs are flow-through (no output data register). Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71T657/59 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$) is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, $CE_2$, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three are not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state one cycle after chip is deselected or a write is initiated.

The IDT71T657/59 have an on-chip burst counter. In the burst mode, the IDT71T657/59 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71T657/59 SRAMs utilize IDT's high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-lead plastic thin quad flatpack (TQFP) as well as a 119-lead ball grid array (BGA).

## Pin Description Summary

| | | | |
|---|---|---|---|
| $A_0$-$A_{18}$ | Address Inputs | Input | Synchronous |
| $\overline{CE}_1$, $CE_2$, $\overline{CE}_2$ | Chip Enables | Input | Synchronous |
| $\overline{OE}$ | Output Enable | Input | Asynchronous |
| R/$\overline{W}$ | Read/Write Signal | Input | Synchronous |
| $\overline{CEN}$ | Clock Enable | Input | Synchronous |
| $\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$ | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| ADV/$\overline{LD}$ | Advance burst address / Load new address | Input | Synchronous |
| $\overline{LBO}$ | Linear / Interleaved Burst Order | Input | Static |
| $I/O_0$-$I/O_{31}$, $I/O_{P1}$-$I/O_{P4}$ | Data Input / Output | I/O | Synchronous |
| $V_{DD}$, $V_{DDQ}$ | Core Power, I/O Power | Supply | Static |
| $V_{SS}$ | Ground | Supply | Static |

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**AUGUST 1999**

# Pin Definitions(1)

| Symbol | Pin Function | I/O | Active | Description |
|---|---|---|---|---|
| $A_0$-$A_{18}$ | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables. |
| ADV/$\overline{LD}$ | Advance / Load | I | N/A | ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high. |
| R/$\overline{W}$ | Read / Write | I | N/A | R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place one clock cycle later. |
| $\overline{CEN}$ | Clock Enable | I | LOW | Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock. |
| $\overline{BW_1}$-$\overline{BW_4}$ | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW_1}$-$\overline{BW_4}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device one cycle later. $\overline{BW_1}$-$\overline{BW_4}$ can all be tied low if always doing write to the entire 36-bit word. |
| $\overline{CE_1}$, $\overline{CE_2}$ | Chip Enables | I | LOW | Synchronous active low chip enable. $\overline{CE_1}$ and $\overline{CE_2}$ are used with $CE_2$ to enable the IDT71T657/59 ($\overline{CE_1}$ or $\overline{CE_2}$ sampled high or $CE_2$ sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a one cycle deselect, i.e., the data bus will tri-state one clock cycle after deselect is initiated. |
| $CE_2$ | Chip Enable | I | HIGH | Synchronous active high chip enable. $CE_2$ is used with $\overline{CE_1}$ and $\overline{CE_2}$ to enable the chip. $CE_2$ has inverted polarity but otherwise identical to $\overline{CE_1}$ and $\overline{CE_2}$. |
| CLK | Clock | I | N/A | This is the clock input to the IDT71T657/59. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK. |
| $I/O_0$-$I/O_{31}$ $I/O_{P1}$-$I/O_{P4}$ | Data Input/Output | I/O | N/A | Data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register). |
| $\overline{LBO}$ | Linear Burst Order | I | LOW | Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input, and it must not change during device operation. |
| $\overline{OE}$ | Output Enable | I | LOW | Asynchronous output enable. $\overline{OE}$ must be low to read data from the IDT71T657/59. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low. |
| $V_{DD}$ | Power Supply | N/A | N/A | 2.5V core power supply. |
| $V_{DDQ}$ | Power Supply | N/A | N/A | 2.5V I/O Supply. |
| $V_{SS}$ | Ground | N/A | N/A | Ground. |

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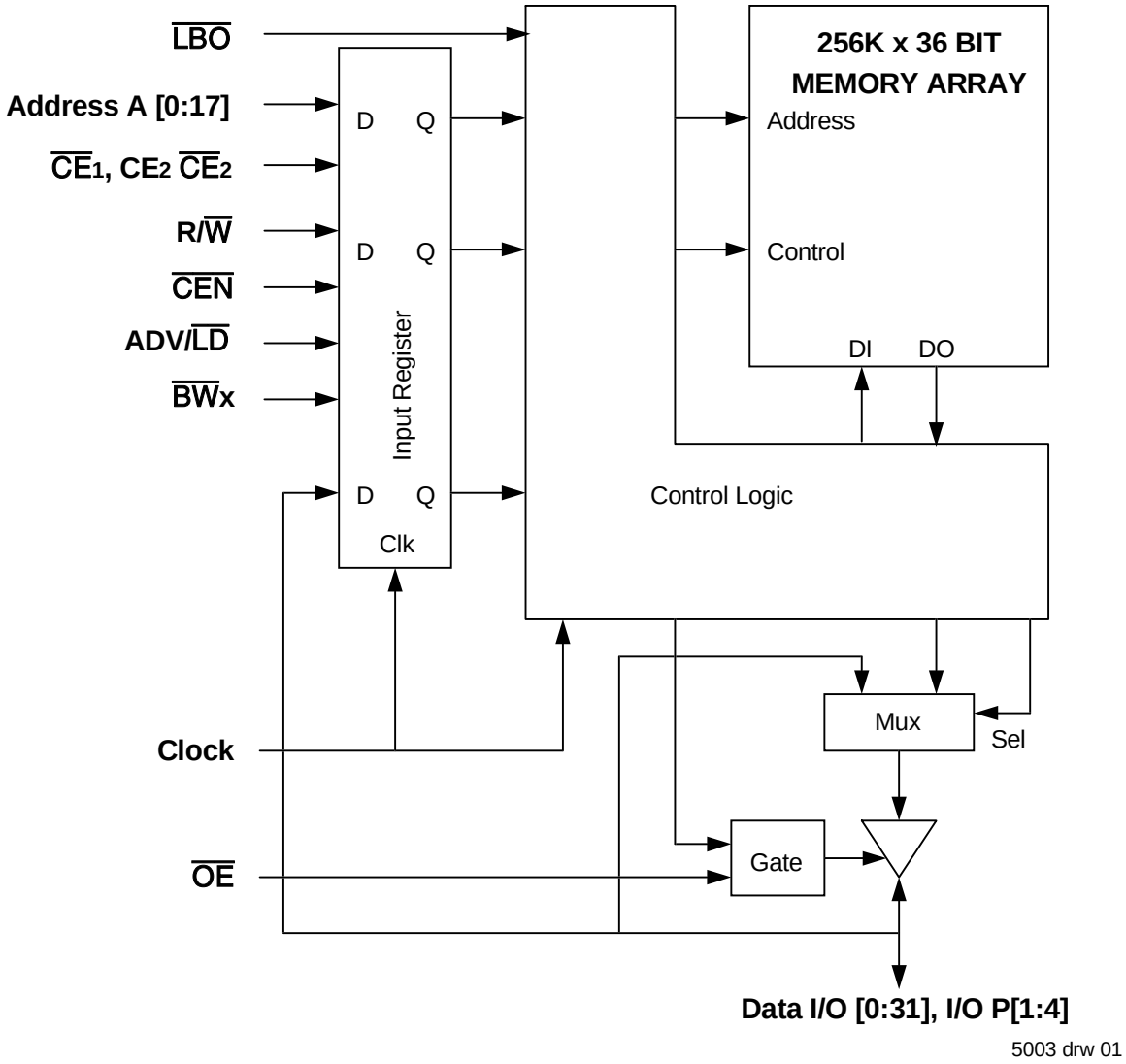
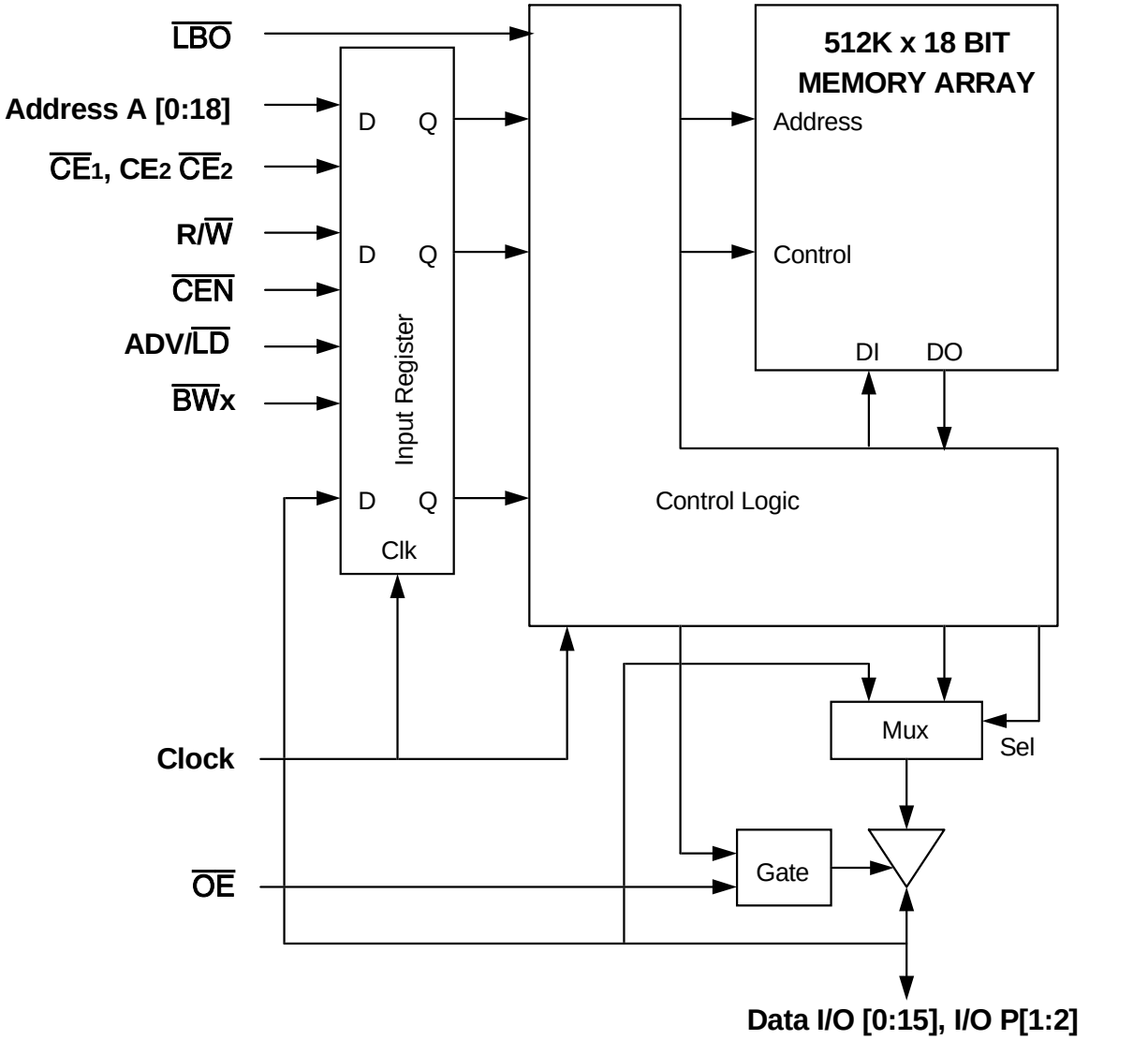
**NOTE:**
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

# Functional Block Diagram for 256K x 36 Configuration




5003 drw 01

## Functional Block Diagram for 512K x 18 Configuration

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## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| $V_{DDQ}$ | I/O Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage — Inputs | 1.7 | — | $V_{DD}$ +0.3 | V |
| $V_{IH}$ | Input High Voltage — I/O | 1.7 | — | $V_{DDQ}$ +0.3[2] | V |
| $V_{IL}$ | Input Low Voltage | -0.3[1] | — | 0.7 | V |

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**NOTE:**
1. $V_{IL}$ (min.) = –0.8V for pulse width less than $t_{CYC}/2$, once per cycle.

## Recommended Operating Temperature Supply Voltage

| Grade | Temperature | VSS | VDD | VDDQ |
|---|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 2.5V±5% | 2.5V±5% |

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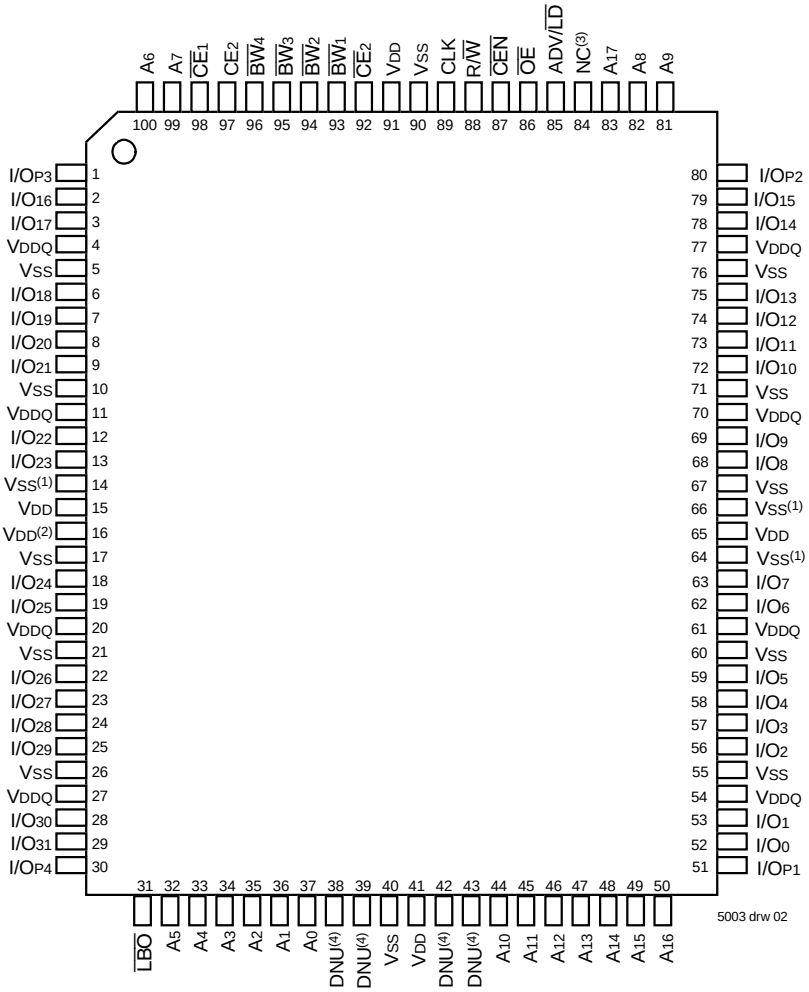
## Pin Configuration - 256K x 36

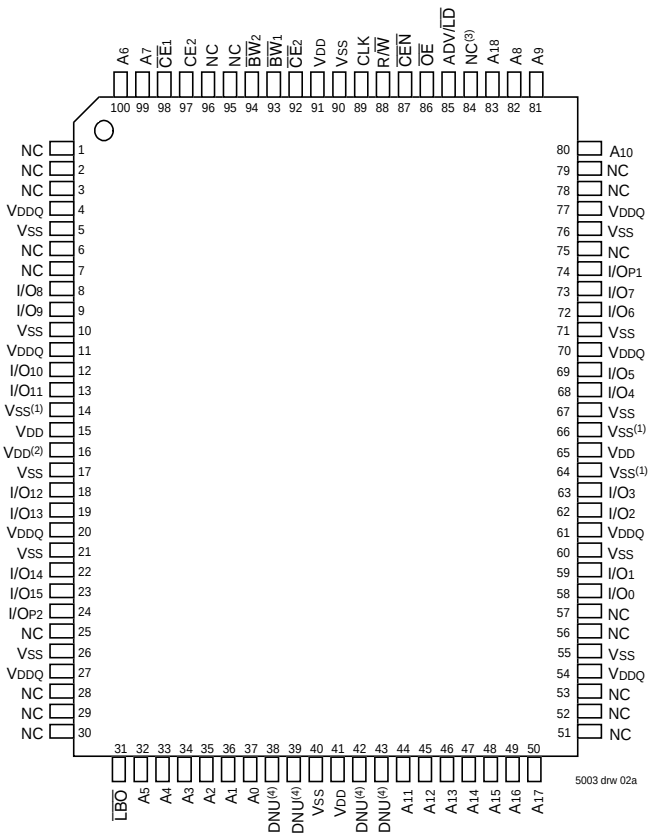



## Top View TQFP

**NOTES:**

1. Pins 14, 64, and 66 do not have to be connected directly to VSS as long as the input voltage is ≤ VIL.
2. Pin 16 does not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
3. Pin 84 is reserved for a future 16M.
4. DNU = Do not use

## Pin Configuration - 512K x 18




**Top View**
**TQFP**

**NOTES:**
1. Pins 14, 64, and 66 do not have to be connected directly to $V_{SS}$ as long as the input voltage is $\leq V_{IL}$.
2. Pin 16 does not have to be connected directly to $V_{DD}$ as long as the input voltage is $\geq V_{IH}$.
3. Pin 84 is reserved for a future 16M.
4. DNU = Do not use.

## Absolute Maximum Ratings(1)

| Symbol | Rating | Commercial | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to +3.6 | V |
| $V_{TERM}$(3,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DD}$ | V |
| $V_{TERM}$(4,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DD}$ +0.5 | V |
| $V_{TERM}$(5,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DDQ}$ +0.5 | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | °C |
| $P_T$ | Power Dissipation | 2.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{DD}$ terminals only.
3. $V_{DDQ}$ terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed $V_{DDQ}$ during power supply ramp up.

## Capacitance

### ($T_A$ = +25°C, f = 1.0MHz, TQFP Package)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 5 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

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**NOTE:**
1. This parameter is guaranteed by device characterization, but not production tested.

## Pin Configuration - 256K x 36 BGA(1,2,3,4)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | A6 | A4 | NC(3) | A8 | A16 | $V_{DDQ}$ |
| B | NC | $\overline{CE}_2$ | A3 | ADV/$\overline{LD}$ | A9 | $\overline{CE}_2$ | NC |
| C | NC | A7 | A2 | $V_{DD}$ | A12 | A15 | NC |
| D | $I/O_{16}$ | $I/O_{P3}$ | $V_{SS}$ | NC | $V_{SS}$ | $I/O_{P2}$ | $I/O_{15}$ |
| E | $I/O_{17}$ | $I/O_{18}$ | $V_{SS}$ | $\overline{CE}_1$ | $V_{SS}$ | $I/O_{13}$ | $I/O_{14}$ |
| F | $V_{DDQ}$ | $I/O_{19}$ | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $I/O_{12}$ | $V_{DDQ}$ |
| G | $I/O_{20}$ | $I/O_{21}$ | $\overline{BW}_3$ | A17 | $\overline{BW}_2$ | $I/O_{11}$ | $I/O_{10}$ |
| H | $I/O_{22}$ | $I/O_{23}$ | $V_{SS}$ | R/$\overline{W}$ | $V_{SS}$ | $I/O_9$ | $I/O_8$ |
| J | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$(2) | $V_{DD}$ | $V_{SS}$(1) | $V_{DD}$ | $V_{DDQ}$ |
| K | $I/O_{24}$ | $I/O_{26}$ | $V_{SS}$ | CLK | $V_{SS}$ | $I/O_6$ | $I/O_7$ |
| L | $I/O_{25}$ | $I/O_{27}$ | $\overline{BW}_4$ | NC | $\overline{BW}_1$ | $I/O_4$ | $I/O_5$ |
| M | $V_{DDQ}$ | $I/O_{28}$ | $V_{SS}$ | $\overline{CEN}$ | $V_{SS}$ | $I/O_3$ | $V_{DDQ}$ |
| N | $I/O_{29}$ | $I/O_{30}$ | $V_{SS}$ | $A_1$ | $V_{SS}$ | $I/O_2$ | $I/O_1$ |
| P | $I/O_{31}$ | $I/O_{P4}$ | $V_{SS}$ | $A_0$ | $V_{SS}$ | $I/O_0$ | $I/O_{P1}$ |
| R | NC | $A_5$ | $\overline{LBO}$ | $V_{DD}$ | $V_{SS}$(1) | $A_{13}$ | DNU(4) |
| T | NC | NC | $A_{10}$ | $A_{11}$ | $A_{14}$ | NC | NC |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | DNU(4) | $V_{DDQ}$ |

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**Top View**

## Pin Configurations - 512K x 18 BGA(1,2,3,4)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | A6 | A4 | NC(3) | A8 | A16 | $V_{DDQ}$ |
| B | NC | CE2 | A3 | ADV/$\overline{LD}$ | A9 | $\overline{CE}_2$ | NC |
| C | NC | A7 | A2 | $V_{DD}$ | A13 | A17 | NC |
| D | $I/O_8$ | NC | $V_{SS}$ | NC | $V_{SS}$ | $I/O_7$ | NC |
| E | NC | $I/O_9$ | $V_{SS}$ | $\overline{CE}_1$ | $V_{SS}$ | NC | $I/O_6$ |
| F | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $I/O_5$ | $V_{DDQ}$ |
| G | NC | $I/O_{10}$ | $\overline{BW}_2$ | $A_{18}$ | $V_{SS}$ | NC | $I/O_4$ |
| H | $I/O_{11}$ | NC | $V_{SS}$ | R/$\overline{W}$ | $V_{SS}$ | $I/O_3$ | NC |
| J | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$(2) | $V_{DD}$ | $V_{SS}$(1) | $V_{DD}$ | $V_{DDQ}$ |
| K | NC | $I/O_{12}$ | $V_{SS}$ | CLK | $V_{SS}$ | NC | $I/O_2$ |
| L | $I/O_{13}$ | NC | $V_{SS}$ | NC | $\overline{BW}_1$ | $I/O_1$ | NC |
| M | $V_{DDQ}$ | $I/O_{14}$ | $V_{SS}$ | $\overline{CEN}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| N | $I/O_{15}$ | NC | $V_{SS}$ | $A_1$ | $V_{SS}$ | $I/O_0$ | NC |
| P | NC | $I/O_{P2}$ | $V_{SS}$ | $A_0$ | $V_{SS}$ | NC | $I/O_{P1}$ |
| R | NC | $A_5$ | $\overline{LBO}$ | $V_{DD}$ | $V_{SS}$(1) | $A_{12}$ | DNU(4) |
| T | NC | $A_{10}$ | $A_{15}$ | NC | $A_{14}$ | $A_{11}$ | NC |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | DNU(4) | $V_{DDQ}$ |

5003 drw 13B

**Top View**

**NOTES:**
1. R5 and J5 do not have to be directly connected to $V_{SS}$ as long as the input voltage is ≤ $V_{IL}$.
2. J3 does not have to be directly connected directly to $V_{DD}$ as long as the input voltage is ≥ $V_{IH}$.
3. A4 is reserved for future 16M.
4. DNU = Do not use.

## Synchronous Truth Table(1)

| $\overline{CEN}$ | R/$\overline{W}$ | $\overline{CE_1}$, $\overline{CE_2}$(5) | ADV/$\overline{LD}$ | $\overline{BW}$x | ADDRESS USED | PREVIOUS CYCLE | CURRENT CYCLE | I/O (One cycle later) |
|---|---|---|---|---|---|---|---|---|
| L | L | L | L | Valid | External | X | LOAD WRITE | D(7) |
| L | H | L | L | X | External | X | LOAD READ | Q(7) |
| L | X | X | H | Valid | Internal | LOAD WRITE / BURST WRITE | BURST WRITE (Advance burst counter)(2) | D(7) |
| L | X | X | H | X | Internal | LOAD READ / BURST READ | BURST READ (Advance burst counter)(2) | Q(7) |
| L | X | H | L | X | X | X | DESELECT or STOP(3) | HIZ |
| L | X | X | H | X | X | DESELECT / NOOP | NOOP | HIZ |
| H | X | X | X | X | X | X | SUSPEND(4) | Previous Value |

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**NOTES:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE_1}$, or $\overline{CE_2}$ is sampled high or $CE_2$ is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state one cycle after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propogating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE_1}$ = L, $\overline{CE_2}$ = L and $CE_2$ = H on these chip enable pins. The chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z during device power-up.
7. Q - data read from the device, D - data written to the device.

## Partial Truth Table for Writes(1)

| OPERATION | R/$\overline{W}$ | $\overline{BW_1}$ | $\overline{BW_2}$ | $\overline{BW_3}$(3) | $\overline{BW_4}$(3) |
|---|---|---|---|---|---|
| READ | H | X | X | X | X |
| WRITE ALL BYTES | L | L | L | L | L |
| WRITE BYTE 1 (I/O[0:7], $I/O_{P1}$)(2) | L | L | H | H | H |
| WRITE BYTE 2 (I/O[8:15], $I/O_{P2}$)(2) | L | H | L | H | H |
| WRITE BYTE 3 (I/O[16:23], $I/O_{P3}$)(2,3) | L | H | H | L | H |
| WRITE BYTE 4 (I/O[24:31], $I/O_{P4}$)(2,3) | L | H | H | H | L |
| NO WRITE | L | H | H | H | H |

5003 tbl 09

**NOTES:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for x18 configuration.

## Interleaved Burst Sequence Table ($\overline{LBO}$=$V_{DD}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address(1) | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

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**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

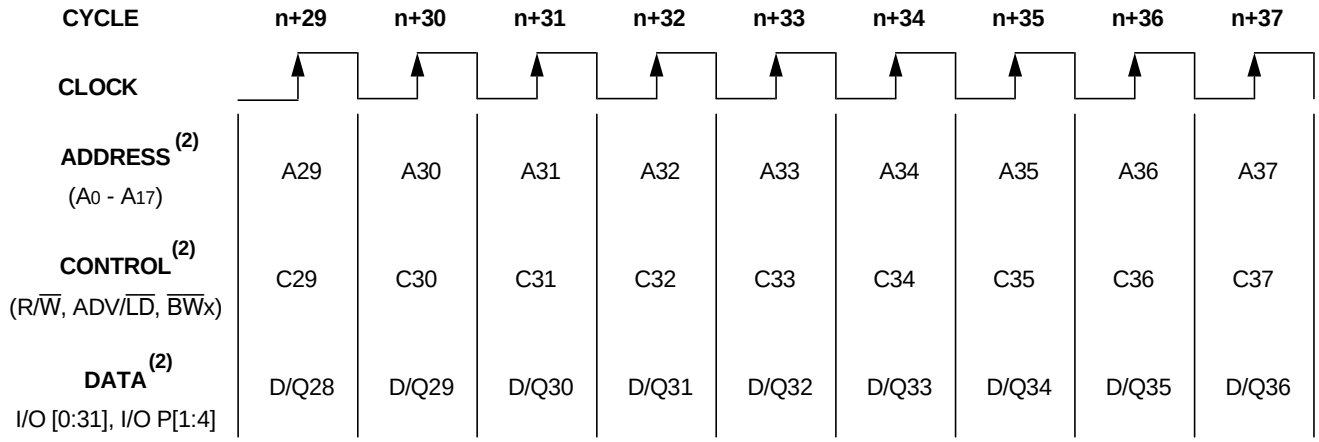
## Linear Burst Sequence Table ($\overline{LBO}$=Vss)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address(1) | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

5003 tbl 11

**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

## Functional Timing Diagram(1)




5003 drw 03

**NOTES:**
1. This assumes $\overline{CEN}$, $\overline{CE}_1$, $CE_2$ and $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

# Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles(2)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(1) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | $D_1$ | Load read |
| n+1 | X | X | H | X | L | X | L | $Q_0$ | Burst read |
| n+2 | $A_1$ | H | L | L | L | X | L | $Q_{0+1}$ | Load read |
| n+3 | X | X | L | H | L | X | L | $Q_1$ | Deselect or STOP |
| n+4 | X | X | H | X | L | X | X | Z | NOOP |
| n+5 | $A_2$ | H | L | L | L | X | X | Z | Load read |
| n+6 | X | X | H | X | L | X | L | $Q_2$ | Burst read |
| n+7 | X | X | L | H | L | X | L | $Q_{2+1}$ | Deselect or STOP |
| n+8 | $A_3$ | L | L | L | L | L | X | Z | Load write |
| n+9 | X | X | H | X | L | L | X | $D_3$ | Burst write |
| n+10 | $A_4$ | L | L | L | L | L | X | $D_{3+1}$ | Load write |
| n+11 | X | X | L | H | L | X | X | $D_4$ | Deselect or STOP |
| n+12 | X | X | H | X | L | X | X | Z | NOOP |
| n+13 | $A_5$ | L | L | L | L | L | X | Z | Load write |
| n+14 | $A_6$ | H | L | L | L | X | X | $D_5$ | Load read |
| n+15 | $A_7$ | L | L | L | L | L | L | $Q_6$ | Load write |
| n+16 | X | X | H | X | L | L | X | $D_7$ | Burst write |
| n+17 | $A_8$ | H | L | L | L | X | X | $D_{7+1}$ | Load read |
| n+18 | X | X | H | X | L | X | L | $Q_8$ | Burst read |
| n+19 | $A_9$ | L | L | L | L | L | L | $Q_{8+1}$ | Load write |

5003 tbl 12

**NOTES:**
1. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.
2. H = High; L = Low; X = Don't Care; Z = High Impedence.

## Read Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | X | X | L | $Q_0$ | Contents of Address $A_0$ Read Out |

5003 tbl 13

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

## Burst Read Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | H | X | L | X | L | $Q_0$ | Address $A_0$ Read Out, Inc. Count |
| n+2 | X | X | H | X | L | X | L | $Q_{0+1}$ | Address $A_{0+1}$ Read Out, Inc. Count |
| n+3 | X | X | H | X | L | X | L | $Q_{0+2}$ | Address $A_{0+2}$ Read Out, Inc. Count |
| n+4 | X | X | H | X | L | X | L | $Q_{0+3}$ | Address $A_{0+3}$ Read Out, Load $A_1$ |
| n+5 | $A_1$ | H | L | L | L | X | L | $Q_0$ | Address $A_0$ Read Out, Inc. Count |
| n+6 | X | X | H | X | L | X | L | $Q_1$ | Address $A_1$ Read Out, Inc. Count |
| n+7 | $A_2$ | H | L | L | L | X | L | $Q_{1+1}$ | Address $A_{1+1}$ Read Out, Load $A_2$ |

5003 tbl 14

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

## Write Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | L | L | L | L | L | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | L | X | X | $D_0$ | Write to Address $A_0$ |

5003 tbl 15

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

## Burst Write Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | L | L | L | L | L | X | X | Address and Control meet setup |
| n+1 | X | X | H | X | L | L | X | $D_0$ | Address $A_0$ Write, Inc. Count |
| n+2 | X | X | H | X | L | L | X | $D_{0+1}$ | Address $A_{0+1}$ Write, Inc. Count |
| n+3 | X | X | H | X | L | L | X | $D_{0+2}$ | Address $A_{0+2}$ Write, Inc. Count |
| n+4 | X | X | H | X | L | L | X | $D_{0+3}$ | Address $A_{0+3}$ Write, Load $A_1$ |
| n+5 | $A_1$ | L | L | L | L | L | X | $D_0$ | Address $A_0$ Write, Inc. Count |
| n+6 | X | X | H | X | L | L | X | $D_1$ | Address $A_1$ Write, Inc. Count |
| n+7 | $A_2$ | L | L | L | L | L | X | $D_{1+1}$ | Address $A_{1+1}$ Write, Load $A_2$ |

5003 tbl 16

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

## Read Operation with Clock Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | X | Address $A_0$ and Control meet setup |
| n+1 | X | X | X | X | H | X | X | X | Clock n+1 Ignored |
| n+2 | $A_1$ | H | L | L | L | X | L | $Q_0$ | Address $A_0$ Read out, Load $A_1$ |
| n+3 | X | X | X | X | H | X | L | $Q_0$ | Clock Ignored. Data $Q_0$ is on the bus. |
| n+4 | X | X | X | X | H | X | L | $Q_0$ | Clock Ignored. Data $Q_0$ is on the bus. |
| n+5 | $A_2$ | H | L | L | L | X | L | $Q_1$ | Address $A_1$ Read out, Load $A_2$ |
| n+6 | $A_3$ | H | L | L | L | X | L | $Q_2$ | Address $A_2$ Read out, Load $A_3$ |
| n+7 | $A_4$ | H | L | L | L | X | L | $Q_3$ | Address $A_3$ Read out, Load $A_4$ |

5003 tbl 17

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

## Write Operation with Clock Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | L | L | L | L | L | X | X | Address $A_0$ and Control meet setup. |
| n+1 | X | X | X | X | H | X | X | X | Clock n+1 Ignored. |
| n+2 | $A_1$ | L | L | L | L | L | X | $D_0$ | Write data $D_0$, Load $A_1$. |
| n+3 | X | X | X | X | H | X | X | X | Clock Ignored. |
| n+4 | X | X | X | X | H | X | X | X | Clock Ignored. |
| n+5 | $A_2$ | L | L | L | L | L | X | $D_1$ | Write Data $D_1$, Load $A_2$ |
| n+6 | $A_3$ | L | L | L | L | L | X | $D_2$ | Write Data $D_2$, Load $A_3$ |
| n+7 | $A_4$ | L | L | L | L | L | X | $D_3$ | Write Data $D_3$, Load $A_4$ |

5003 tbl 18

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

## Read Operation with Chip Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}_1$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O(3) | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | X | X | L | H | L | X | X | ? | Deselected. |
| n+1 | X | X | L | H | L | X | X | Z | Deselected. |
| n+2 | $A_0$ | H | L | L | L | X | X | Z | Address $A_0$ and Control meet setup. |
| n+3 | X | X | L | H | L | X | L | $Q_0$ | Address $A_0$ read out, Deselected. |
| n+4 | $A_1$ | H | L | L | L | X | X | Z | Address $A_1$ and Control meet setup. |
| n+5 | X | X | L | H | L | X | L | $Q_1$ | Address $A_1$ read out, Deselected. |
| n+6 | X | X | L | H | L | X | X | Z | Deselected. |
| n+7 | $A_2$ | H | L | L | L | X | X | Z | Address $A_2$ and Control meet setup. |
| n+8 | X | X | L | H | L | X | L | $Q_2$ | Address $A_2$ read out, Deselected. |
| n+9 | X | X | L | H | L | X | X | Z | Deselected. |

5003 tbl 19

**NOTES:**
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. $CE_2$ timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.
3. Device outputs are ensured to be in High-Z during device power-up.

## Write Operation with Chip Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | X | X | L | H | L | X | X | ? | Deselected. |
| n+1 | X | X | L | H | L | X | X | Z | Deselected. |
| n+2 | $A_0$ | L | L | L | L | L | X | Z | Address $A_0$ and Control meet setup |
| n+3 | X | X | L | H | L | X | X | $D_0$ | Data $D_0$ Write In, Deselected. |
| n+4 | $A_1$ | L | L | L | L | L | X | Z | Address $A_1$ and Control meet setup |
| n+5 | X | X | L | H | L | X | X | $D_1$ | Data $D_1$ Write In, Deselected. |
| n+6 | X | X | L | H | L | X | X | Z | Deselected. |
| n+7 | $A_2$ | L | L | L | L | L | X | Z | Address $A_2$ and Control meet setup |
| n+8 | X | X | L | H | L | X | X | $D_2$ | Data $D_2$ Write In, Deselected. |
| n+9 | X | X | L | H | L | X | X | Z | Deselected. |

5003 tbl 20

**NOTES:**
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD}$ = 2.5V±5%)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 5 | µA |
| $\|I_{LI}\|$ | $\overline{LBO}$ Input Leakage Current[1] | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 30 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$ | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = +6mA, $V_{DD}$ = Min. | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -6mA, $V_{DD}$ = Min. | 2.0 | — | V |

5003 tbl 21

**NOTE:**
1. The $\overline{LBO}$ pin will be internally pulled to $V_{DD}$ if it is not actively driven in the application.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] ($V_{DD}$ = 2.5V±5%)

| Symbol | Parameter | Test Conditions | 7.5ns | 8ns | 8.5ns | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Operating Power Supply Current | Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, $V_{DD}$ = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = $f_{MAX}$[2] | 275 | 250 | 225 | mA |
| $I_{SB1}$ | CMOS Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3] | 40 | 40 | 40 | mA |
| $I_{SB2}$ | Clock Running Power Supply Current | Device Deselected, Outputs Open, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = $f_{MAX}$[2,3] | 105 | 100 | 95 | mA |
| $I_{SB3}$ | Idle Power Supply Current | Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = $f_{MAX}$[2,3] | 40 | 40 | 40 | mA |

5003 tbl 22

**NOTES:**
1. All values are maximum guaranteed values.
2. At f = $f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of 1/$t_{CYC}$; f=0 means no input lines are changing.
3. For I/Os $V_{HD}$ = $V_{DDQ}$ – 0.2V, $V_{LD}$ = 0.2V. For other inputs $V_{HD}$ = $V_{DD}$ – 0.2V, $V_{LD}$ = 0.2V.

## AC Test Load

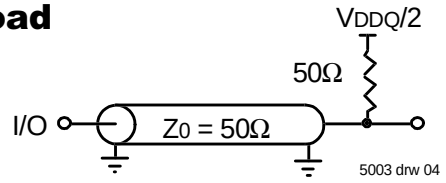



**Figure 1. AC Test Load**

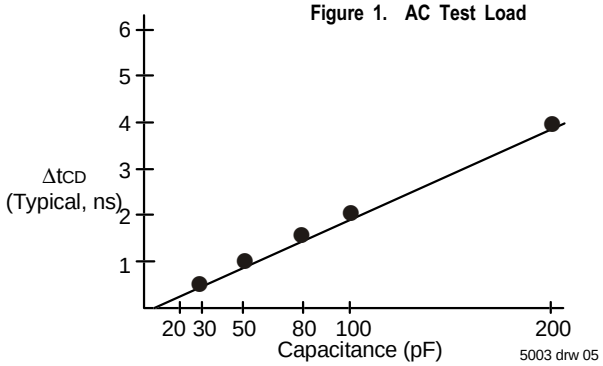



**Figure 2. Lumped Capacitive Load, Typical Derating**

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 0 to 2.5V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | ($V_{DDQ/2}$) |
| Output Reference Levels | ($V_{DDQ/2}$) |
| Output Load | Figure 1 |

5003 tbl 23

# AC Electrical Characteristics

## ($V_{DD}$ = 2.5V±5%, $T_A$ = 0 to 70°C)

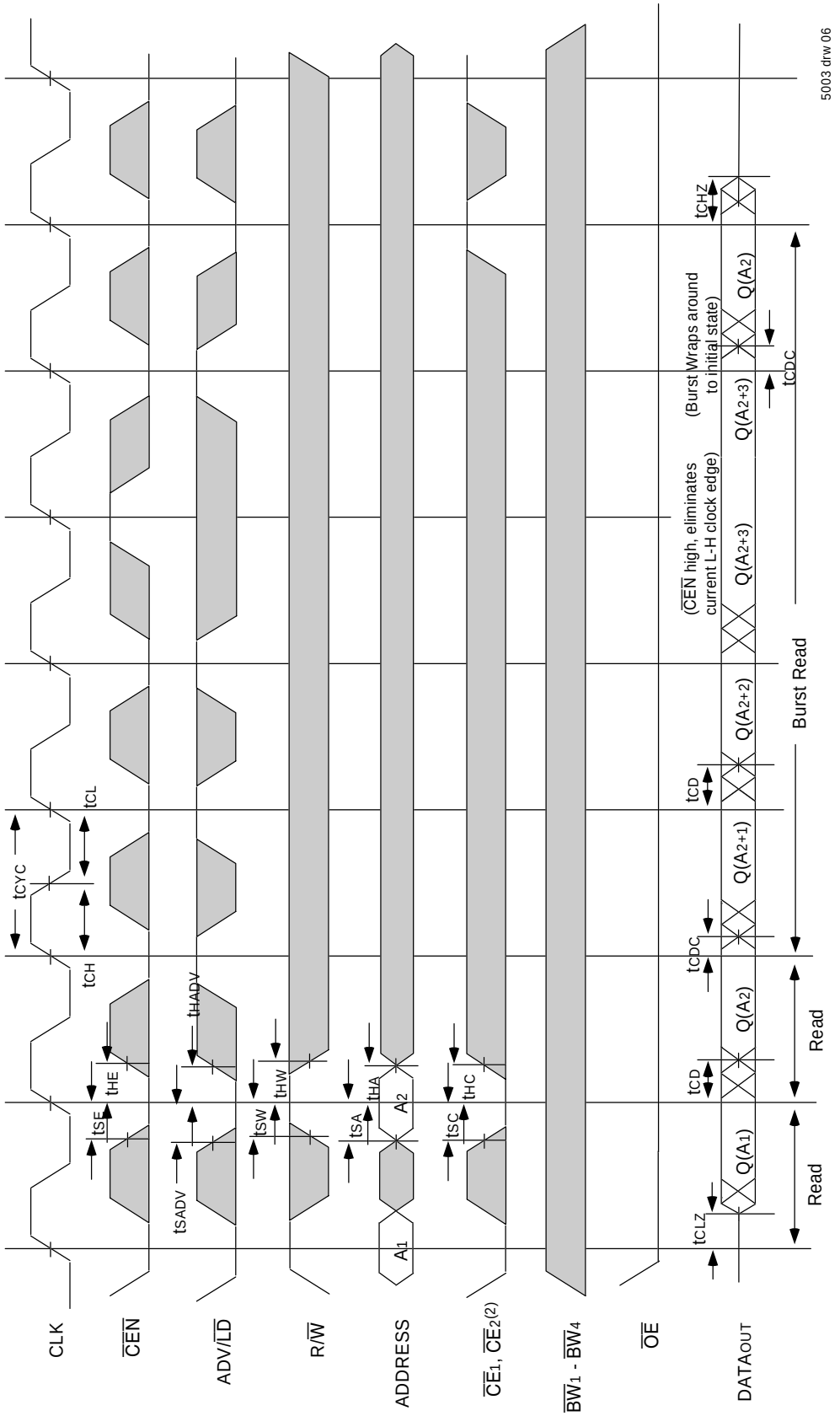
| Symbol | Parameter | 7.5ns | | 8ns | | 8.5ns | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| | | | | | | | | |
| $t_{CYC}$ | Clock Cycle Time | 10 | — | 10.5 | — | 11 | — | ns |
| $t_{CH}$(1) | Clock High Pulse Width | 2.5 | — | 2.7 | — | 3.0 | — | ns |
| $t_{CL}$(1) | Clock Low Pulse Width | 2.5 | — | 2.7 | — | 3.0 | — | ns |
| **Output Parameters** | | | | | | | | |
| $t_{CD}$ | Clock High to Valid Data | — | 7.5 | — | 8 | — | 8.5 | ns |
| $t_{CDC}$ | Clock High to Data Change | 2 | — | 2 | — | 2 | — | ns |
| $t_{CLZ}$(2,3,4) | Clock High to Output Active | 3 | — | 3 | — | 3 | — | ns |
| $t_{CHZ}$(2,3,4) | Clock High to Data High-Z | — | 5 | — | 5 | — | 5 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 5 | — | 5 | — | 5 | ns |
| $t_{OLZ}$(2,3) | Output Enable Low to Data Active | 0 | — | 0 | — | 0 | — | ns |
| $t_{OHZ}$(2,3) | Output Enable High to Data High-Z | — | 5 | — | 5 | — | 5 | ns |
| **Set Up Times** | | | | | | | | |
| $t_{SE}$ | Clock Enable Setup Time | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_{SA}$ | Address Setup Time | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_{SD}$ | Data In Setup Time | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_{SW}$ | Read/Write (R/$\overline{W}$) Setup Time | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_{SADV}$ | Advance/Load (ADV/$\overline{LD}$) Setup Time | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_{SC}$ | Chip Enable/Select Setup Time | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_{SB}$ | Byte Write Enable ($\overline{BW}$x) Setup Time | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| **Hold Times** | | | | | | | | |
| $t_{HE}$ | Clock Enable Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HA}$ | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HD}$ | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HW}$ | Read/Write (R/$\overline{W}$) Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HADV}$ | Advance/Load (ADV/$\overline{LD}$) Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HC}$ | Chip Enable/Select Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HB}$ | Byte Write Enable ($\overline{BW}$x) Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |

5003 tbl 24

**NOTES:**

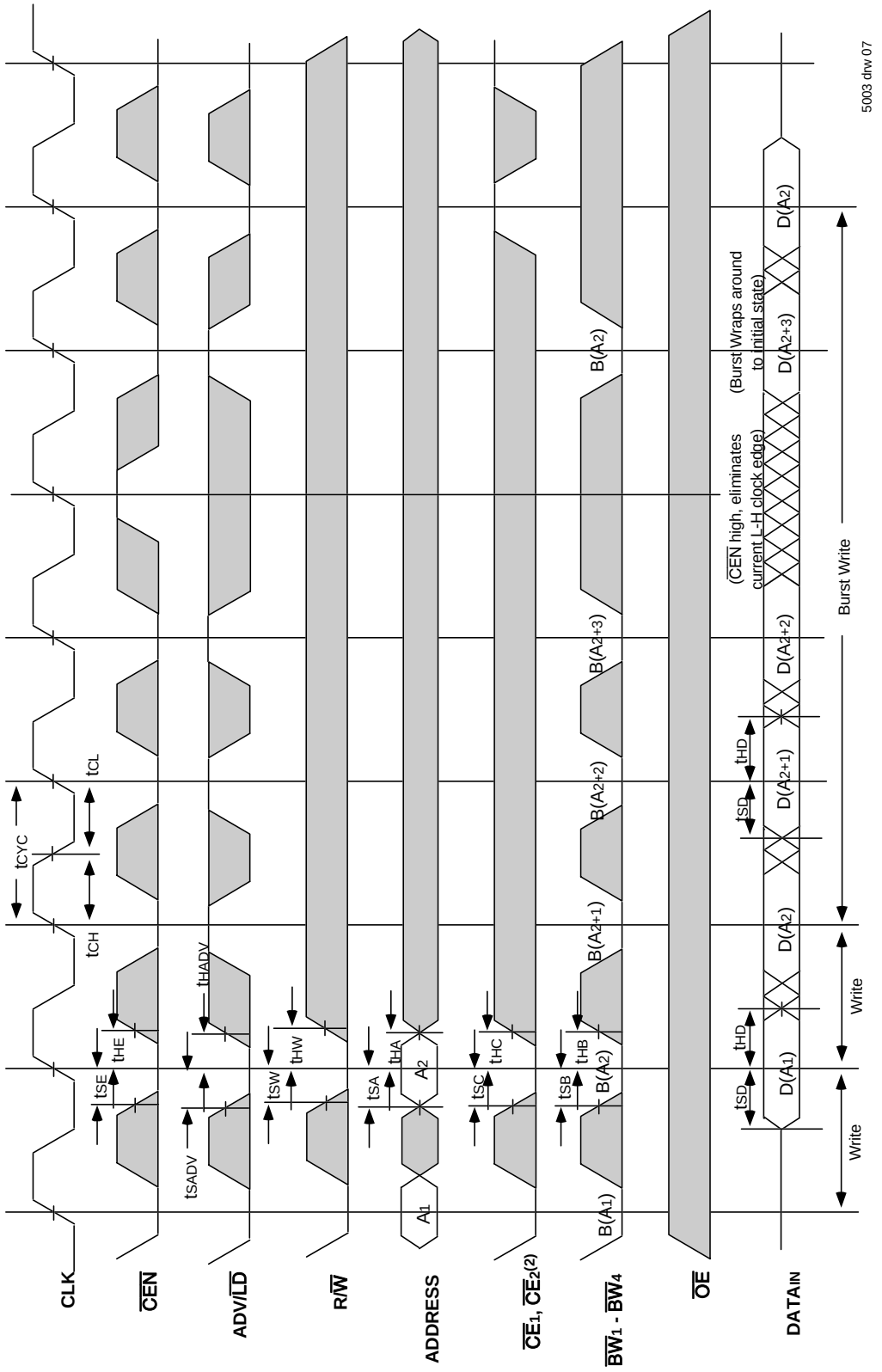
1. Measured as HIGH above 0.6$V_{DDQ}$ and LOW below 0.4$V_{DDQ}$.
2. Transition is measured ±200mV from steady-state.
3. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
4. To avoid bus contention, the output buffers are designed such that $t_{CHZ}$ (device turn-off) is about 1ns faster than $t_{CLZ}$ (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because $t_{CLZ}$ is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 2.625V) than $t_{CHZ}$, which is a Max. parameter (worse case at 70 deg. C, 2.375V).

# Timing Waveform of Read Cycle(1,2,3,4)




**NOTES:**
1. Q (A1) represents the first output from the external address A1. Q (A2) represents the first output from the external address A2; Q (A2+1) represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.

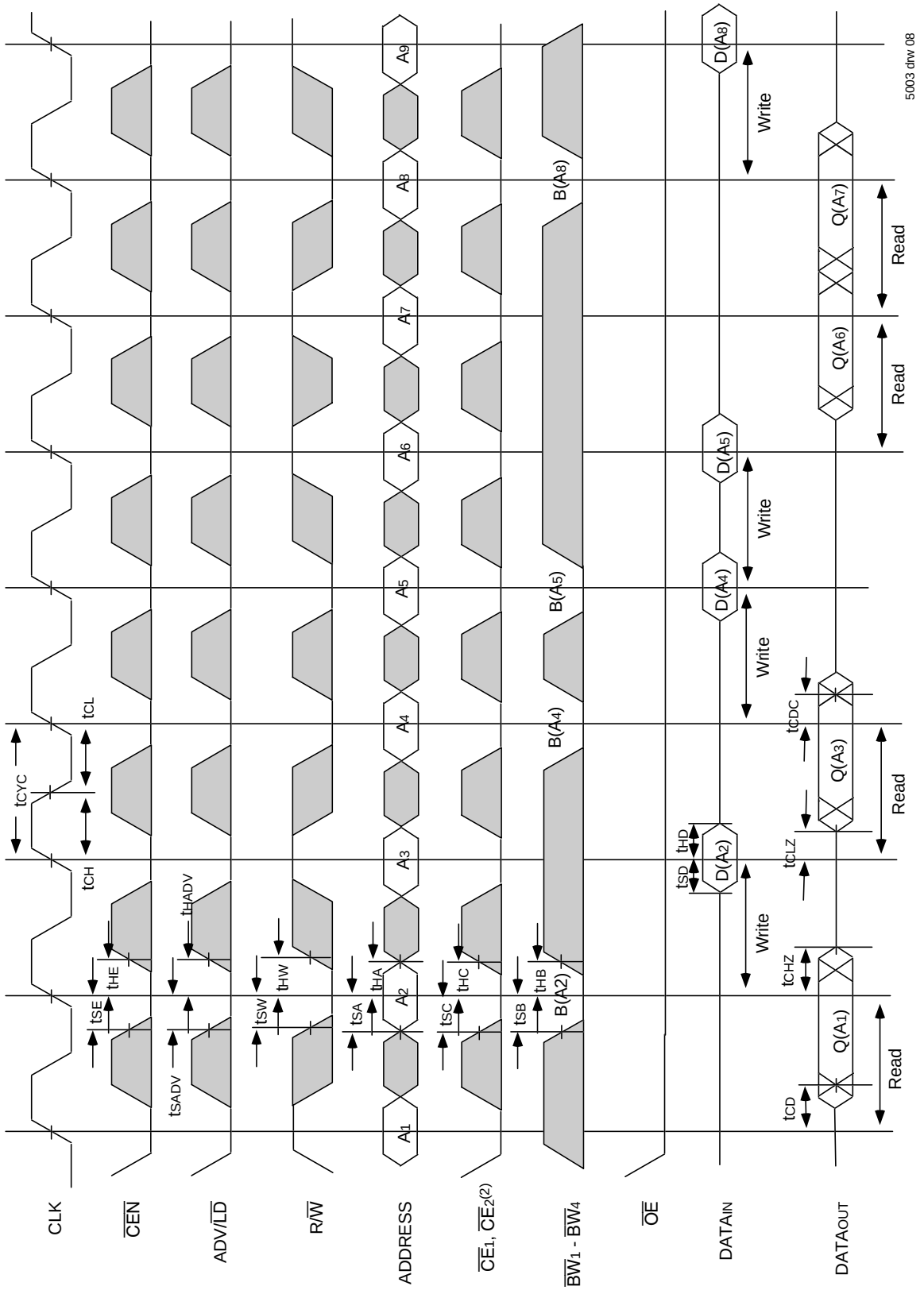
# Timing Waveform of Write Cycles(1,2,3,4,5)




**NOTES:**

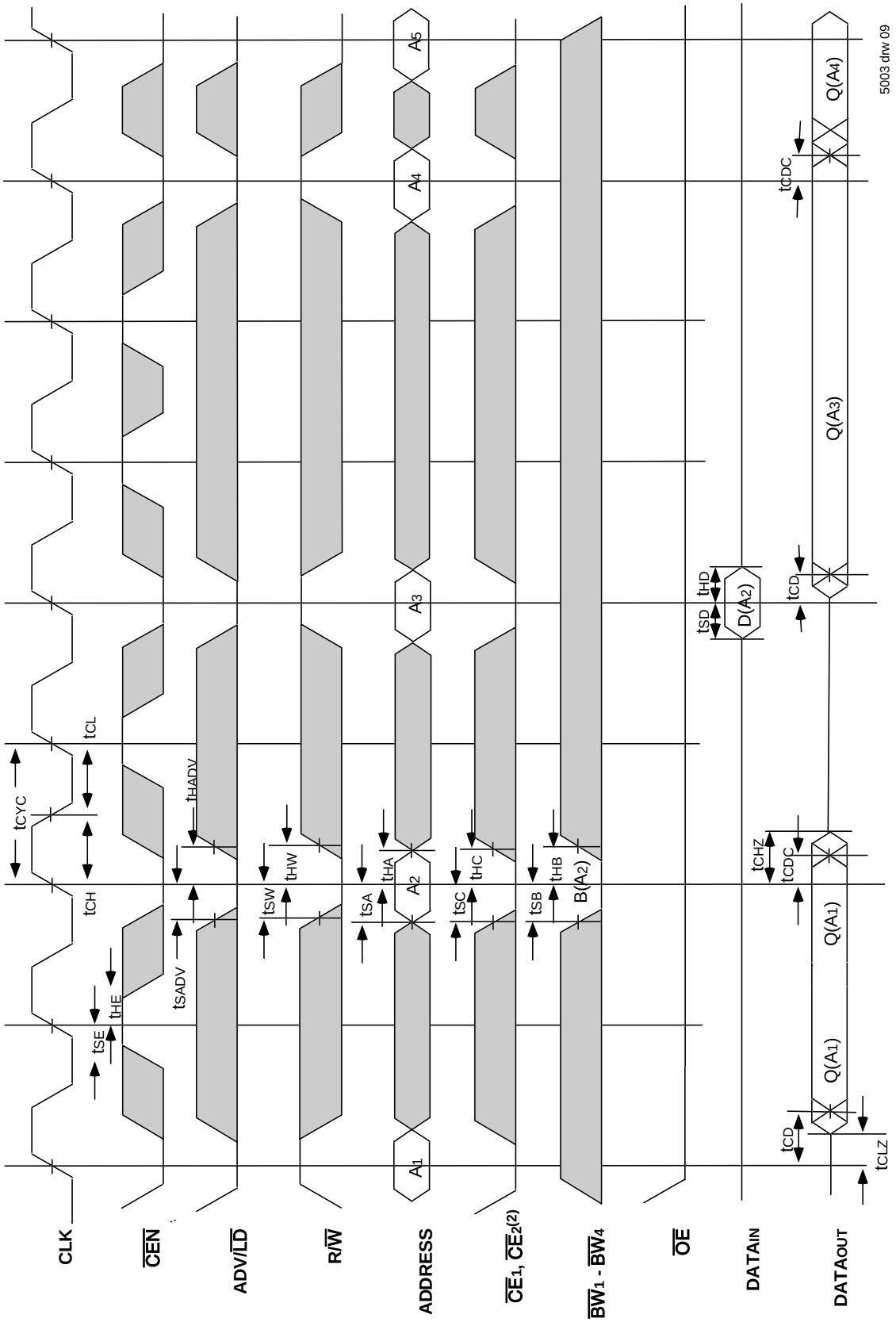
1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

# Timing Waveform of Combined Read and Write Cycles(1,2,3)



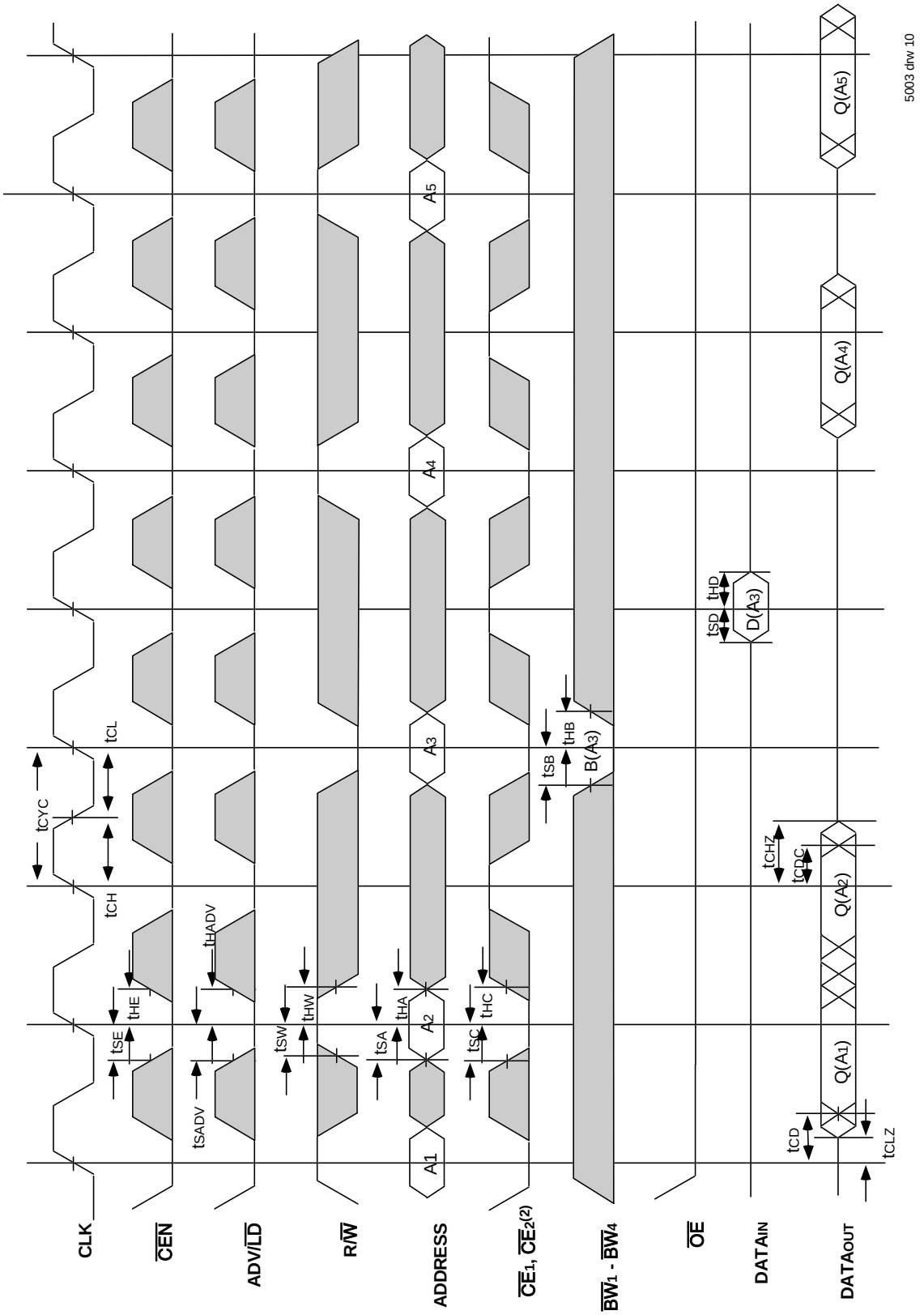

**NOTES:**
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

# Timing Waveform of $\overline{CEN}$ Operation(1,2,3,4)




**NOTES:**
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. $CE_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, $CE_2$ is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propogating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

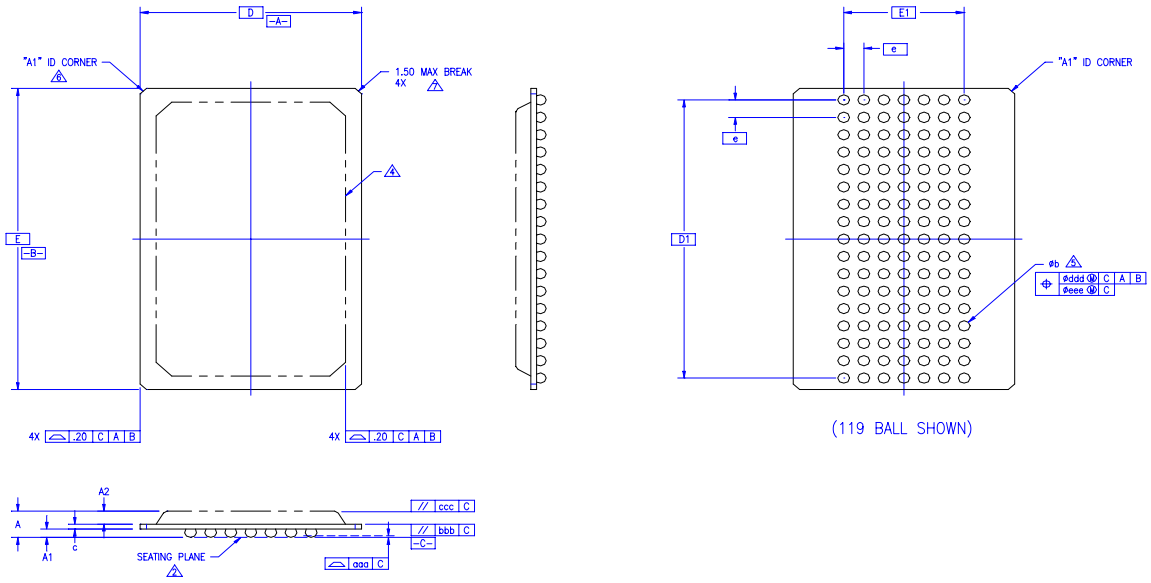
# Timing Waveform of $\overline{CS}$ Operation(1,2,3,4)




**NOTES:**
1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3 etc.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. When either one of the Chip enables ($\overline{CE}_1$, CE2, $\overline{CE}_2$) is sampled inactive at the rising clock edge, a deselect cycle is initiated. The data-bus tri-states one cycle after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

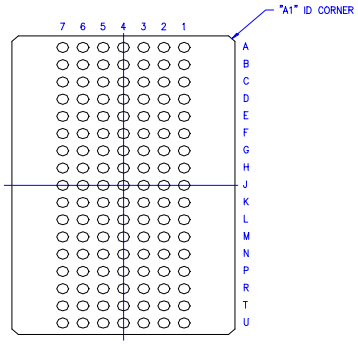
# 119-Lead Ball Grid Array (BGA) Package Diagram Outline

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 60626 | 00 | INITIAL RELEASE | 10/15/97 | |




| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
|---|---|---|---|
| DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | | |
| APPROVALS | DATE | TITLE | BG PACKAGE OUTLINE<br>14.0 X 22.0 mm BODY<br>PBGA |
| DRAWN JTV | 10/15/97 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4063 REV 00 |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 60626 | 00 | INITIAL RELEASE | 10/15/97 | |




| SYMBOL | JEDEC VARIATION AA | | | NOTE |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| A | – | 2.15 | 3.50 | |
| A1 | .50 | .60 | .70 | |
| A2 | – | – | 2.50 | |
| D | | 22.00 BSC | | |
| D1 | | 20.32 BSC | | |
| E | | 14.00 BSC | | |
| E1 | | 7.62 BSC | | |
| MD | | 17 | | 3 |
| ME | | 7 | | 3 |
| N | | 119 | | 3 |
| e | | 1.27 BSC | | |
| b | .60 | .75 | .90 | 5 |
| c | .10 | – | 2.50 | |
| aaa | – | – | .20 | |
| bbb | – | – | .25 | |
| ccc | – | – | .35 | |
| ddd | – | – | .30 | |
| eee | – | – | .15 | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
3. "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION
   "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION
   "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS
4. PACKAGE MAY EXTEND TO EDGE PERIPHERY AND MAY CONSIST OF MOLDING COMPOUND, EPOXY, METAL, CERAMIC OR OTHER MATERIAL
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE
7. ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL
8. ALL DIMENSIONS ARE IN MILLIMETERS
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–028, VARIATION AA

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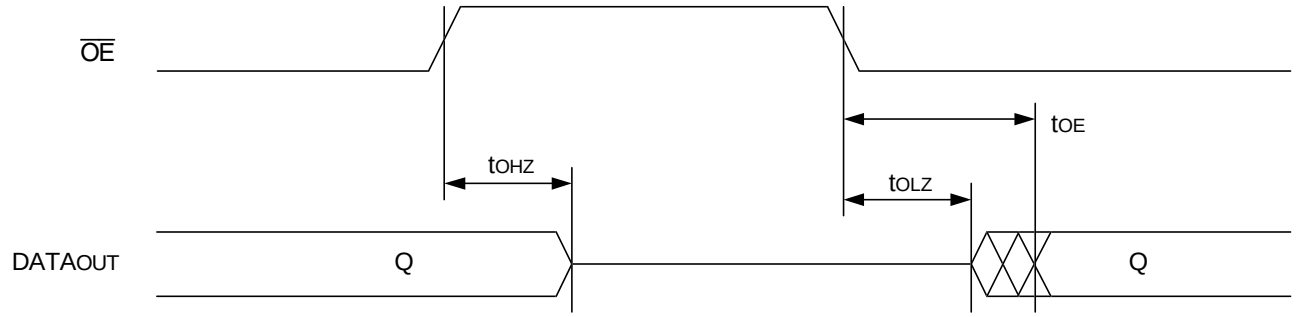
|---|---|---|---|
| DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | | |
| APPROVALS | DATE | TITLE | BG PACKAGE OUTLINE<br>14.0 X 22.0 mm BODY<br>PBGA |
| DRAWN JTV | 10/15/97 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4063 REV 00 |
| | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

## Timing Waveform of $\overline{OE}$ Operation(1)

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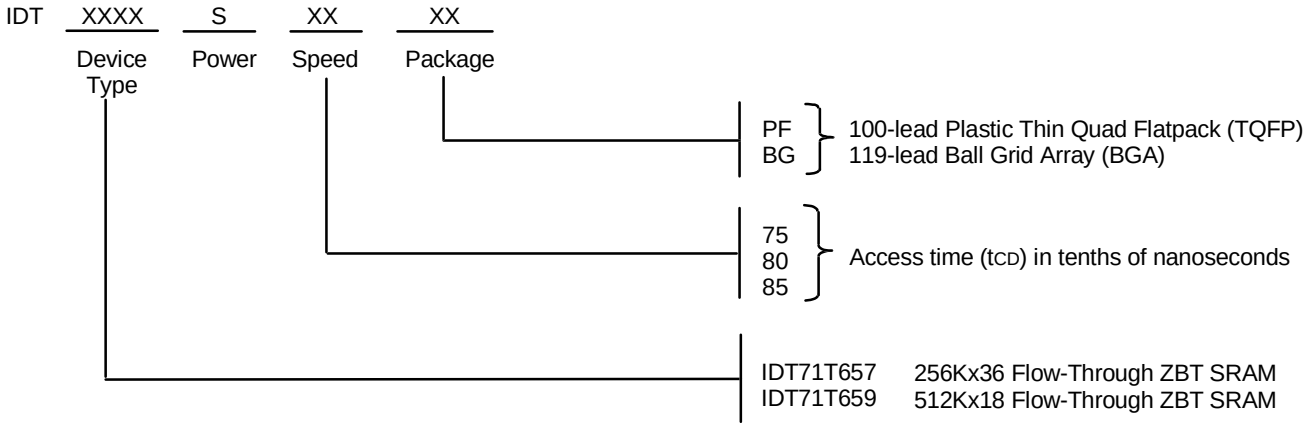
**NOTE:**
1. A read operation is assumed to be in progress.

## Ordering Information

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# Datasheet Document History

| | | |
|---|---|---|
| 7/26/99 | | Updated to new format |
| 8/23/99 | Pp. 5, 6 | Added pin 64 to Note 1 and changed pins 38, 42, and 43 to DNU |
| | Pg. 7 | Changed U6 to DNU |
| | Pg. 15 | Improved $t_{CH}$, $t_{CL}$; revised $t_{CLZ}$ |
| | Pg. 23 | Added Datasheet Document History |

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