

T-46-23-14

MSM8128S/K/V/W/JX 128K x 8 Monolithic CMOS SRAM

Issue 1.0 : August 1989

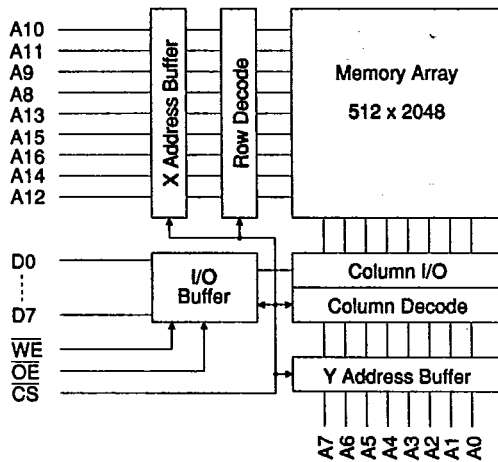
131,072 x 8 CMOS High Speed Static RAM

ADVANCE PRODUCT INFORMATION

Features

- Fast Access Times of 45,55,70 nS
- ASIC (JEDEC) 1Megabit Module Pinout
- Upgradable to 4Megabit Module
- VIL™ High Density Package
- Low Power Standby 50μW (typ.)-L Version
- Low Power Operation 150mW(yp.)-L Version
- 2.0V Data Retention Mode
- Completely Static Operation
- Equal Access and Cycle Times
- Battery Back-up Capability
- Directly TTL Compatible
- Common Data Inputs & Outputs
- May be Processed to MIL-STD-883B (suffix MB)

Block Diagram



Pin Definition

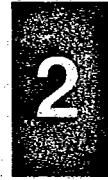
Package Type: 'S', 'K', 'V'

NC	1		32	V _{CC}
A16	2		31	A15
A14	3		30	NC
A12	4		29	WE
A7	5		28	A13
A6	6		27	A8
A5	7		26	A9
A4	8		25	A11
A3	9		24	OE
A2	10		23	A10
A1	11		22	CS
A0	12		21	D7
D0	13		20	D6
D1	14		19	D5
D2	15		18	D4
GND	16		17	D3

Type 'W', 'J' on page 2-96.

Pin Functions

- A0-A16 Address Inputs
- D0-7 Data Input/Output
- CS Chip Select
- OE Output Enable
- WE Write Enable
- NC No Connect
- V_{CC} Power (+5V)
- GND Ground



Package Details

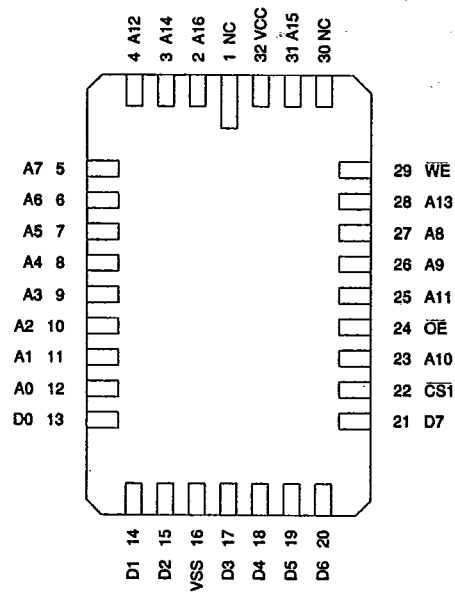
Pin Count	Description	Package Type	Material	Pin Out
32	600 mil Dual-in-Line (DIP)	S	Ceramic	JEDEC
32	400 mil Dual-in-Line (DIP)	K	Ceramic	JEDEC
32	100 mil Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	W	Ceramic	ASIC
32	J-Leaded Chip Carrier (JLCC)	J	Ceramic	ASIC

Package dimensions and outlines are displayed on page 2-97,98.

VIL is a trademark of Mosaic Semiconductor Inc., Patent Pending #287982.

Pin Definition: Package Type 'W','J'

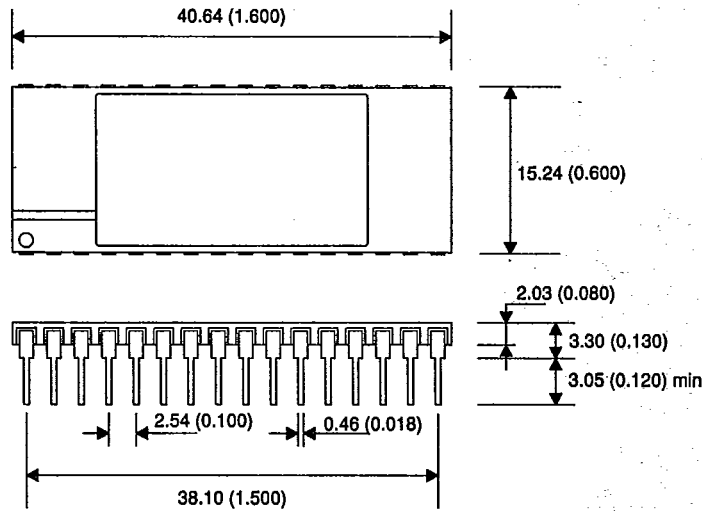
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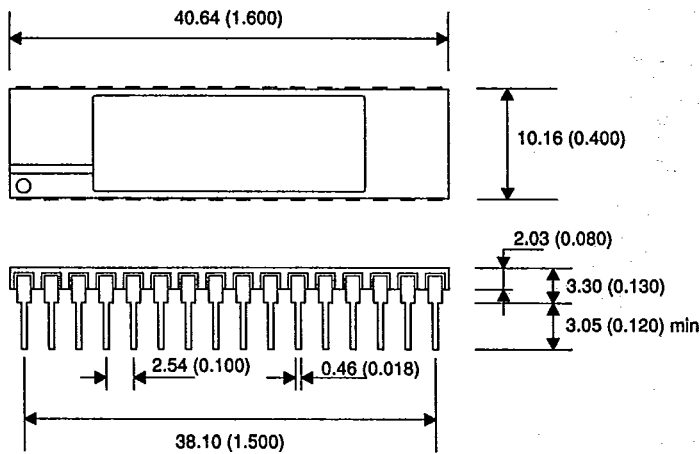
Package Details Dimensions in mm (inches). Tolerance on all dimensions +/-0.254(0.010).

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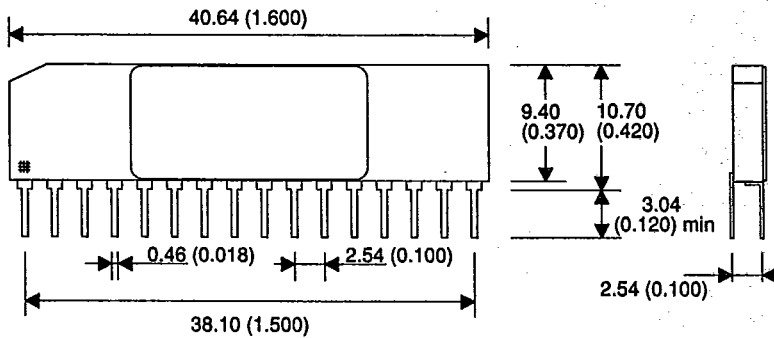
32 pin 600 mil Dual-in-Line (DIP) - 'S' Package



32 pin 400 mil Dual-in-Line (DIP) - 'K' Package

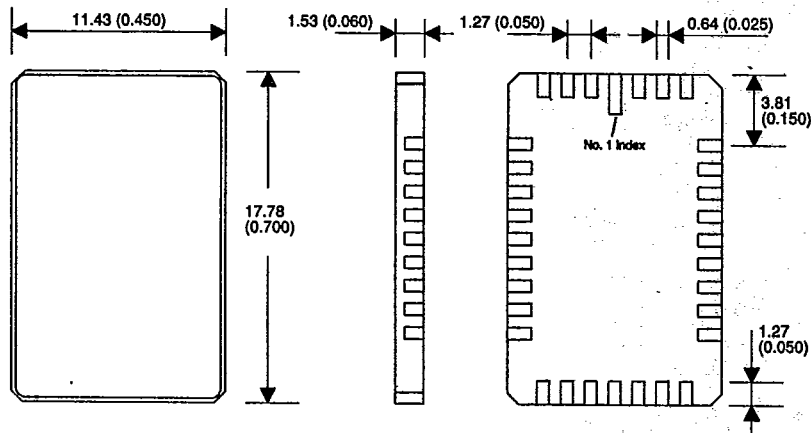


32 pin 100 mil Vertical-in-Line (VIL™) - 'V' Package

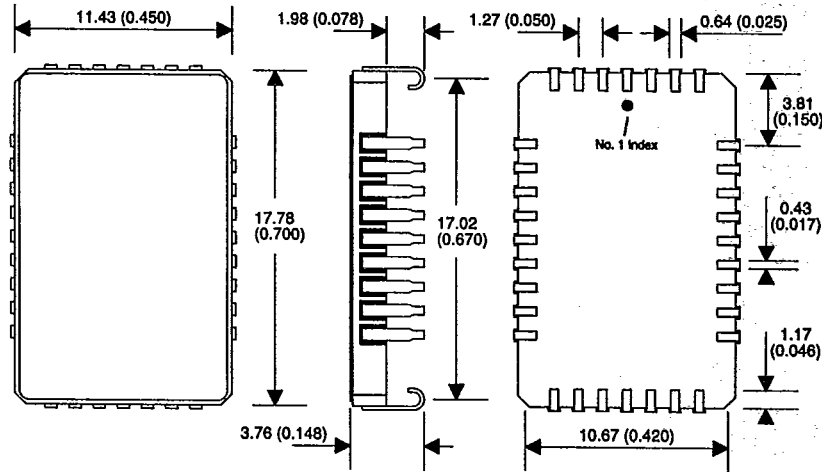


32 pin Extended Leadless Chip Carrier (LCC) - 'W' Package

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32 pin Extended 'J' Leaded Chip Carrier (JLCC) - 'J' Package



Military Screening Procedure

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Monolithic Screening Flow for high reliability product is in accordance with Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW		
<i>SCREEN</i>	<i>TEST METHOD (Per MIL 883C)</i>	<i>LEVEL</i>
Visual and Mechanical Internal visual High-temperature storage Temperature Cycle Constant acceleration Pre-Burn-in electrical Burn-in	2010 Condition B or manufacturers equivalent 1008 Condition C (24hrs @ 150°C) 1010 Condition C (10 Cycles, -65°C to 150°C) 2001 Condition E (Y axis only), (30,000g) Per applicable device specification @ Ta+25°C Method 1015, Condition D, Ta+125°C, 160 hrs min.	100% 100% 100% 100% 100% 100%
Final Electrical Tests Static (dc) Functional Switching (ac)	Per applicable device specification a) @ Ta=25°C and power supply extremes b) @ temperature and power supply extremes a) @ Ta=25°C and power supply extremes b) @ temperature and power supply extremes a) @ Ta=25°C and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100% 100%
Percent Defective Allowable(PDA)	Calculated at post-burn-in @ Ta=25°C	5%
Hermeticity Fine Gross	1014 Condition A Condition C	100% 100%
External Visual	2009 Per vendor or customer specification	100%



Ordering Information

MSM8128SXLMB-45

