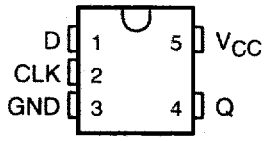
# SN74ALVC1G79
# SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES105B – SEPTEMBER 1997– REVISED JANUARY 1998

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Packaged in Plastic Small-Outline Transistor Package

DCK PACKAGE
(TOP VIEW)




## description

This single positive-edge-triggered D-type flip-flop is designed for 2.3-V to 3.6-V $V_{CC}$ operation.

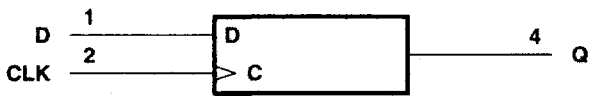
When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN74ALVC1G79 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| CLK | D | Q |
| ↑ | H | H |
| ↑ | L | L |
| L | X | $Q_0$ |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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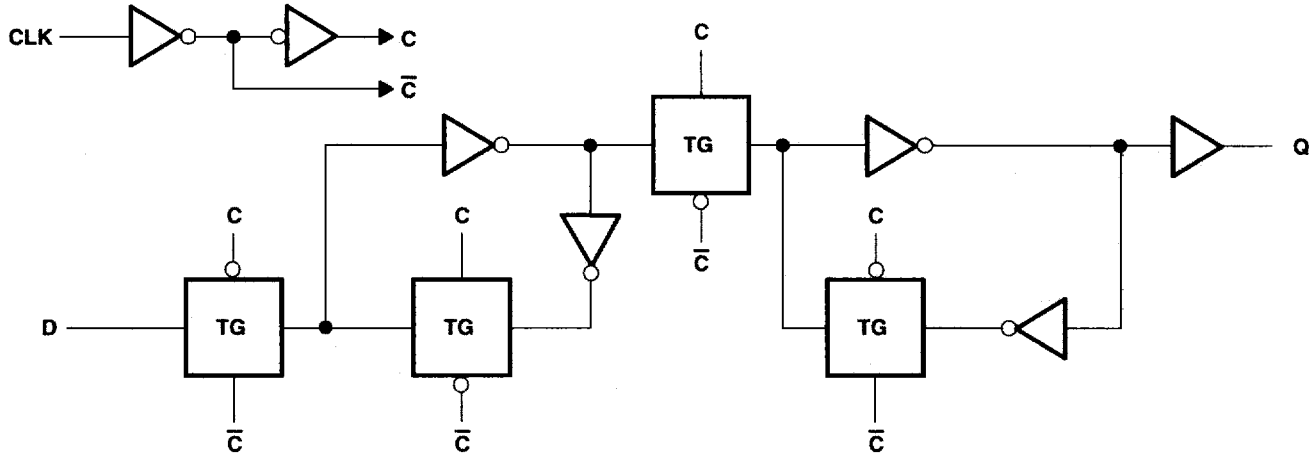
## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2) ..... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) ..... –50 mA
Continuous output current, $I_O$ ..... ±50 mA
Continuous current through $V_{CC}$ or GND ..... ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) ..... 389°C/W
Storage temperature range, $T_{stg}$ ..... –65 C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.3 V | | –12 | mA |
| | | $V_{CC}$ = 2.7 V | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.3 V | | 12 | mA |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH}$ = –100 µA | 2.3 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | $I_{OH}$ = –6 mA | 2.3 V | 2 | | | |
| | $I_{OH}$ = –12 mA | 2.3 V | 1.7 | | | |
| | | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| | $I_{OH}$ = –24 mA | 3 V | 2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | 2.3 V to 3.6 V | | | 0.2 | V |
| | $I_{OL}$ = 6 mA | 2.3 V | | | 0.4 | |
| | $I_{OL}$ = 12 mA | 2.3 V | | | 0.7 | |
| | | 2.7 V | | | 0.4 | |
| | $I_{OL}$ = 24 mA | 3 V | | | 0.55 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 3.6 V | | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 20 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

PRODUCT PREVIEW

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

| | | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | | | | | MHz |
| $t_w$ | Pulse duration, CLK high or low | | | | | | | | ns |
| $t_{su}$ | Setup time before CLK↑ | Data high | | | | | | | ns |
| | | Data low | | | | | | | |
| $t_h$ | Hold time, data after CLK↑ | | | | | | | | ns |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | | | | | | | MHz |
| $t_{pd}$ | CLK | Q | | | | | | | ns |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V | UNIT |
|---|---|---|---|---|---|
| | | | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 0, f = 10 MHz | | | pF |

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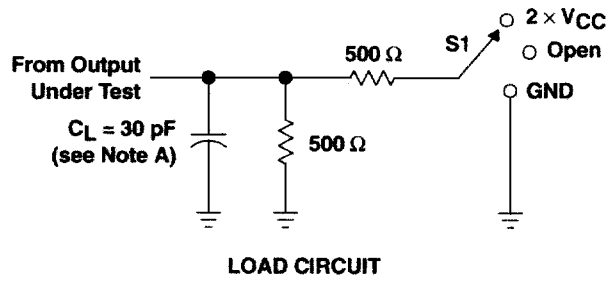
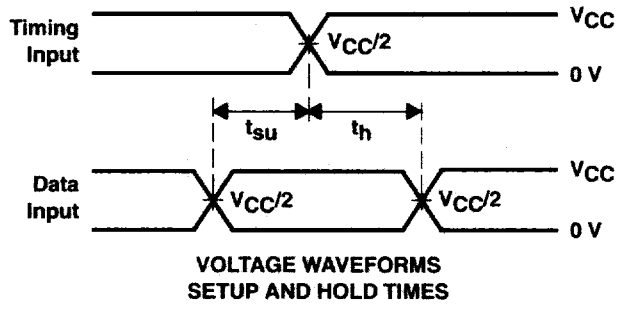
## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

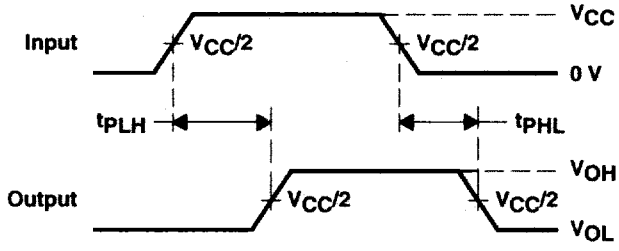



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

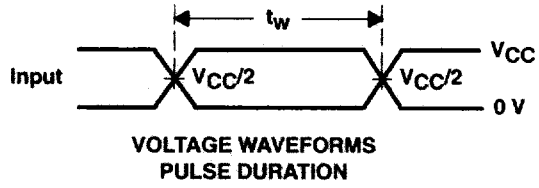
LOAD CIRCUIT



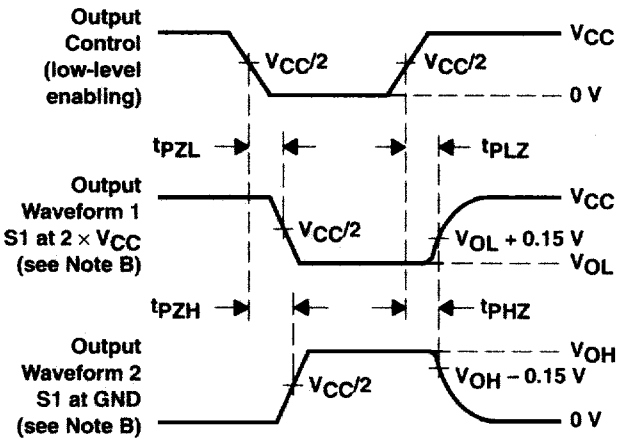

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The output is measured with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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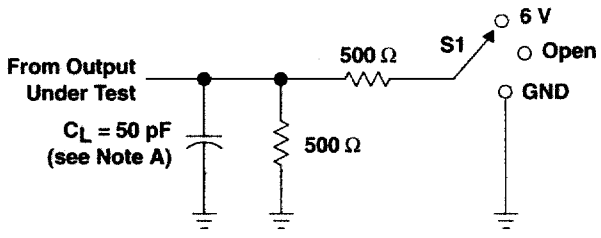
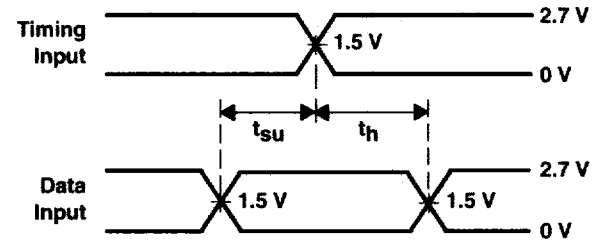
## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

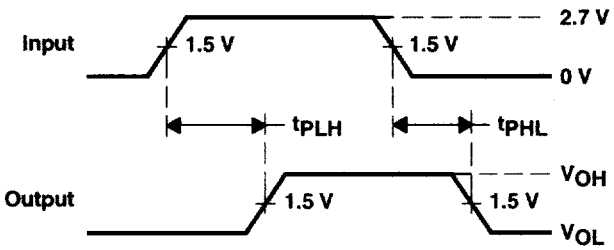



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

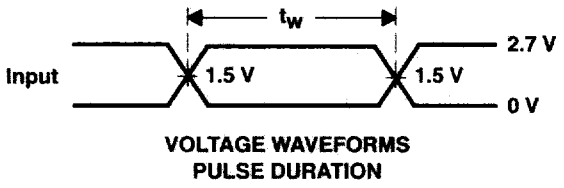
LOAD CIRCUIT



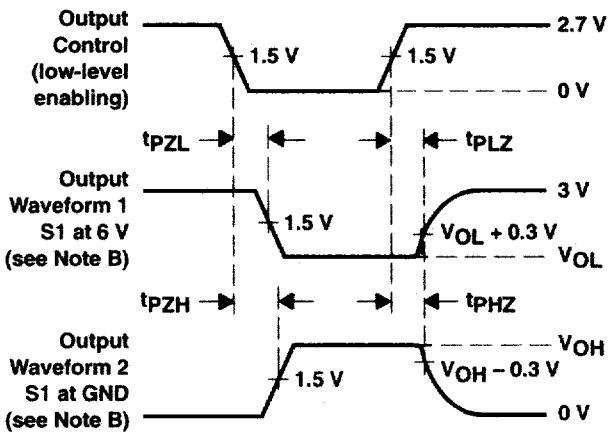

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The output is measured with one input transition per measurement.
E. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
F. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

**Figure 2. Load Circuit and Voltage Waveforms**

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