Winbond Electronics Corp.

512K x 8 CMOS FLASH MEMORY

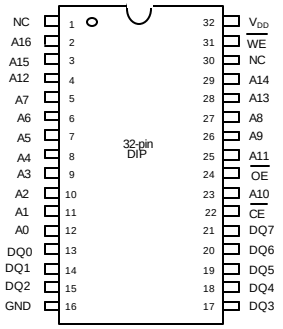
GENERAL DESCRIPTION

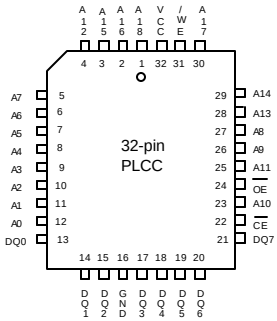
The W29D040C is an 4Mbit, 5-volt only CMOS flash memory organized as 512K × 8 bits. For flexible erase capability, the 4 Mbits of data are divided into 8 uniform sectors of 64 Kbytes. The byte-wide (× 8) data appears on DQ7–DQ0. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29D040C results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased by using standard EPROM programmers.

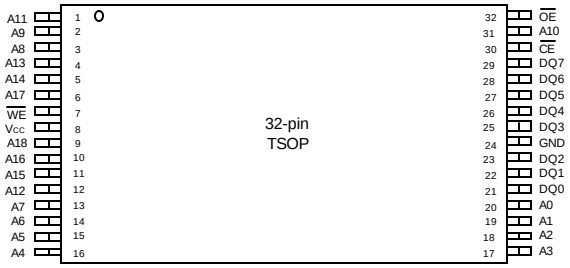
FEATURES

- Single 5-volt write (program and erase) operations
- Fast byte-write operation
  - Chip programming cycle: 20 S (typ.)
  - Chip erase cycle: 1 S (typ.)
- Sector erase architecture
  - 8 uniform sectors of 64K bytes each
  - Any combination of sectors can be erased
  - Supports full chip erase
- Sector protection
  - Sectors can be locked via programmer
- Read access time: 55/70 ns
- Typical program/erase cycles:
  - 10K/100K
- Twenty-year data retention
- Low power consumption
  - Active current: 30 mA (typ.)
  - Standby current: 1 μA (typ.)
- End of program detection
  - Software method: Toggle bit/Data polling
- TTL compatible I/O
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin PLCC, 32-pin TSOP and 32-pin PDIP

PIN CONFIGURATIONS



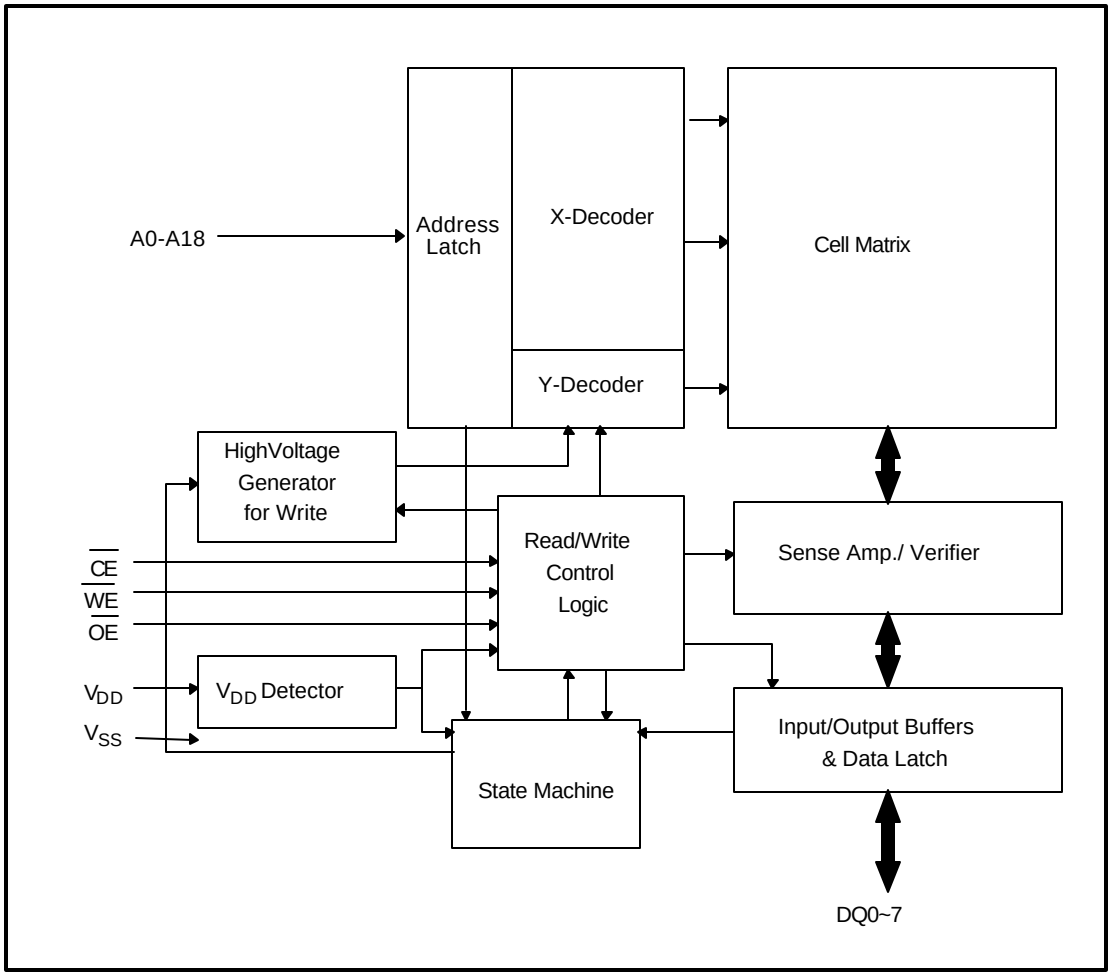




PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A18	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VDD	Power Supply
GND	Ground

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

DEVICE BUS OPERATION

Read Mode

The read operation of the W29D040C is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. Refer to the timing waveforms for further details.

Write Mode

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written to bringing $\overline{WE}$ to logic low state, while $\overline{CE}$ is at logic low state and $\overline{OE}$ is at logic high state. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Standby Mode

There are two ways to implement the standby mode on the W29D040C device, both using the $\overline{CE}$ pin.

A CMOS standby mode is achieved with the $\overline{CE}$ input held at VCC $\pm$ 0.3V. Under this condition the current is typically reduced to less than 5 μA. A TTL standby mode is achieved with the $\overline{CE}$ pin held at VIH. Under this condition the current is typically reduced to 1 mA.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Output Disable Mode

With the $\overline{OE}$ input at a logic high level (VIH), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect Mode

The autoselect mode allows the reading of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force VID (11.5V to 12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from VIL to VIH. All addresses are don′t cares except A0, A1, and A6 (see "Autoselet Codes").

The manufacturer and device codes may also be read via the command register, for instances, when the W29D040C is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in "Autoselet Codes".

Byte 0 (A0 = VIL) represents the manufacturer's code (Winbond = DAH) and byte 1 (A0 = VIH) the device identifier code (W29D040C = 26). All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A1 must be VIL.

The autoselect mode also facilitates the determination of sector protection in the system. By performing a read operation at the address location XX02H with the higher order address bits A16–A18 set to the desired sector address, the device will return 01H for a protected sector and 00H for a non-protected sector.

Full Chip/Sector Protection

The W29D040C features hardware full chip/sector protection. This feature will disable both program and erase operations in full chip or any combination of nineteen sectors of memory. The full chip sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. (See "Device Bus Operations")

It is possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order address bits A16 – A18 is the desired sector address, will produce a logical "1" at DQ0 for a protected sector.

DATA PROTECTION

The W29D040C is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transitions or system noise.

Low VCC Write Inhibit

To avoid initiation of a write cycle during VCC power-up and power-down, the W29D040C locks out write cycles for VCC < VLKO (see DC Characteristics section for voltages). When VCC < VLKO, all internal program/erase circuits are disabled, and the device resets to the read mode. The W29D040C ignores all writes until VCC > VLKO. The user must ensure that the control pins are in the correct logic state when VCC > VLKO to prevent unintentional writes.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 nS (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH, or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE}$ = $\overline{CE}$ = VIL and $\overline{OE}$ = VIH will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. "Command Definitions" defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover, both Reset/Read commands are functionally equivalent, resetting the device to the read mode.

Read Command

The device will automatically power-up in the read state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition.

The device will automatically returns to read state after completing an Embedded Program or Embedded Erase algorithm.

Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Reset Command

Writing the reset command to the device resets the device to the read mode.

Once in the autoselect mode, exiting is accomplished by issuing the reset command sequence, which returns the device to the read mode. Please note that the software reset command is ignored during an internal program or erase operation.

Autoselect Command

Flash memories are intended for use in applications where the local CPU can alter memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desirable system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of DAH. A read cycle from address XX01H returns the device code (W29D040C = 26).

Furthermore, the write protect status of sectors can be read in this mode. Scanning the sector addresses (A18, A17, and A16) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read command sequence into the register.

Byte Program Command

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two "unlock" write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded program algorithm. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$

or $\overline{WE}$ (whichever happens first) begins programming using the Embedded Program Algorithm. Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as Data Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see "Hardware Sequence Flags").Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for Data Polling operations. Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to program 0 back to 1, will produce a "1" at the DQ5 output, the toggle bit will stop toggling. Only erase operations can convert "0"s to "1"s.

Refer to the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase Command

Chip erase is a six-bus-cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically erase and verify the entire memory for an all one data pattern. The erase is performed simultaneously on all sectors at the same time (see "Feature"). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" at which time the device returns to read the mode.

Refer to the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase Command

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (30H) is latched on the rising edge of $\overline{WE}$. After a time-out of 80 µS from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased sequentially by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be sequentially erased. The time between writes must be less than 80µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µS time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open. See DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during

this period will reset the device to the read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete.

Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 8).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80 μS time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7, Data Polling, is "1" at which time the device returns to the read mode. Data Polling must be performed at an address within any of the sectors being erased.

Refer to the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend Command

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads or programs to a sector not being erased. This command is applicable only during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are "don′t-cares" when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during a Sector Erase operation, the chip will suspend the operation and go into erase suspended mode, at which time the user can read or program from a sector that is not being erased. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ2 to toggle. After entering the erase-suspend mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase suspend-program mode. Again, programming in this mode is the same as programming in regular Byte Program mode, except that the data must be programmed to sectors that are not erase suspended. Successively reading from the erase suspended sector while the device is in the erase suspend-program mode will cause DQ2 to toggle. The end of the erase suspend-program operation is detected by the DATA Polling of DQ7, or by the Toggle Bit (DQ6), which is the same as the regular Byte Program operation. Note that DQ7 must be read from the Byte Program address while DQ6 can be read from any address.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

WRITE OPERATION STATUS

DQ7: Data Polling

The W29D040C device features Data Polling as a method to indicate to the host that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. This DQ7 status also applies to programming during erase suspend. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7.

During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm, or if the device enters the Erase Suspend mode, an attempt to read the device will produce a "1" at the DQ7 output.

The flowchart for Data Polling (DQ7) is shown in "Data Polling Algorithm".

For chip erase, the Data Polling is valid after the rising edge of the sixth pulse in the six $\overline{WE}$ write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. Data Polling must be performed at sector addresses within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0 – DQ6 may be still invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see "Command Definitions").

See "$\overline{DATA}$ Polling During Embedded Algorithm Timing Diagrams".

DQ6: Toggle Bit

The W29D040C also features the "Toggle Bit" as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device at any address will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector erase time-out.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ6 to toggle. See "Toggle Bit During Embedded Algorithm Timing Diagrams".

DQ5: Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count).

Under these conditions DQ5 will produce a "1" and DQ6 will stop toggling. This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the

only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in "Device Bus Operations".

The DQ5 failure condition will also appear if a user tries to program a 1 to a location that is previously programmed to 0. In this case the device locks out and never completes the Embedded Program Algorithm. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device.

DQ3: Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin.

DQ3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands (other than Erase Suspend) to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to "Hardware Sequence Flags".

DQ2: Toggle Bit 2

This toggle bit, along with DQ6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase suspend.

Successive reads from the erasing sector will cause DQ2 to toggle during the Embedded Erase Algorithm. If the device is in the erase suspend-read mode, successive reads from the erase-suspend sector will cause DQ2 to toggle. When the device is in the erase suspend-program mode, successive reads from the byte address of the non-erase suspend sector will indicate a logic "1" at the DQ2 bit. Note that a sector which is selected for erase is not available for read in Erase Suspend mode. Other sectors which are not selected for Erase can be read in Erase Suspend.

DQ6 is different from DQ2 in that DQ6 toggles only when the standard program or erase, or erase suspend program operation is in progress.

If the DQ5 failure condition is observed while in Sector Erase mode (i.e., exceeded timing limits), the DQ2 toggle bit can give extra information. In this case, the normal function of DQ2 is modified.

TABLE OF OPERATING MODES

Device Bus Operations

MODE	PIN							
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0- DQ7
Read	V_{IL}	V_{IL}	X	A0	A1	A6	A9	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A0	A1	A6	A9	Din
Standby	V_{IH}	X	X	X	X	X	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High Z
Verify Sector Protect	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Code
Full Chip Protect Set	V_{IL}	V_{ID}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	X
Full Chip Unprotected Set	V_{ID}	V_{ID}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	X
Product ID	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Code
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Code

Autoselect Codes (High Voltage Method)

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A18 TO A16	A15 TO A10	A9	A8 TO A7	A6	A5 TO A2	A1	A0	DQ7 TO DQ0
Manufacturer ID: Winbond	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IL}	DAh
Device ID: W29D040C	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	26
Sector Protection Verification	V_{IL}	V_{IL}	V_{IH}	SA	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IL}	01h
												00h

Note: SA = Sector Address, X = Don't Care. Sector Protection Verification: 01h (protected); 00h (unprotected)

Sector Address Table

SECTOR	A18	A17	A16	SECTOR SIZE (KBYTES)	ADDRESS
SA0	0	0	0	64	00000h–0FFFFh
SA1	0	0	0	64	10000h–1FFFFh
SA2	0	0	1	64	20000h–2FFFFh
SA3	0	0	1	64	30000h–3FFFFh
SA4	0	1	0	64	40000h–4FFFFh
SA5	0	1	0	64	50000h–5FFFFh
SA6	0	1	1	64	60000h–6FFFFh
SA7	0	1	1	64	70000h–7FFFFh

Note: All sectors are 64K bytes in size.

Hardware Sequence Flags

	STATUS		DQ7	DQ6	DQ5	DQ3	DQ2
In Progress	Byte Programming		$\overline{DQ7}$	Toggle	0	0	No Tog
	Program/Erase in Auto-Erase		0	Toggle	0	1	(Note 1)
	Erase suspend mode	Erase sector address	1	No Tog	0	1	Toggle
		Non-erase sector address	Data	Data	Data	Data	Data
	Program in erase suspend		$\overline{DQ7}$ (Note 2)	Toggle	0	1	1 (Note 1)
Exceeded Time Limits	Bye Programming		$\overline{DQ7}$	Toggle	1	0	No Tog
	Programming/Erase in Auto-Erase		0	Toggle	1	1	(Note 3)
	Program in erase suspend		$\overline{DQ7}$	Toggle	1	1	(Note 3)

Note:

1. DQ2 can be toggles when sector address applied is that of an erasing sector. Conversely, DQ2 cannot be toggle when the sector address applied is that of a non-erasing sector. DQ2 is used to determine which are erasing and which are not.

2. These status flags apply when outputs are read from the address of a erase-suspended sector.

3. If DQ5 is high (exceeded timing limits), successive reads from a problem sector will cause DQ2 will stop toggling.

Command Definitions

COMMAND SEQUENCE (NOTE 2)	BUS CYCLES											
	FIRST		SECOND		THIRD		FOURTH		FIFTH		SIXTH	
	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
Read	RA	RD										
Manufacturer ID	2AAA	AA	5555	55	2AAA	90	00	DA				
Device ID	2AAA	AA	5555	55	2AAA	90	01	26				
Sector Protect	2AAA	AA	5555	55	2AAA	90	(SA)	00				
Verify (Note 3)							02	01				
Program	2AAA	AA	5555	55	2AAA	A0	(PA)	(PD)				
Chip Erase	2AAA	AA	5555	55	2AAA	80	2AAA	AA	5555	55	2AAA	10
Sector Erase	2AAA	AA	5555	55	2AAA	80	2AAA	AA	5555	55	(SA)	30
Erase Suspend (Note 4)	×××	B0										
Erase Resume	×××	30										

Legend :

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Address are latched on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse.

PD = Data to be programmed at location PA. Data is latched on the rising edge of the $\overline{WE}$ or $\overline{CE}$ pulse.

SA = Address of the sector to be erased. Address bits A18–A16 uniquely select any sector.

Note :

1. All values are in hexadecimal.
2. See "Device Bus Operations" for description of bus operations.
3. The data is 00H for an unprotected sector group and 01H for a protected sector group. The complete bus address composed of the sector address (A18–A6), A1 = 1, and A0 = 0.
4. Read and program functions in non-erasing sector are allowed in the Erase Suspend mode.
5. Unless otherwise noted, address bits A18-A11 = × = don't care.

DC CHARACTERISTICS

Absolute maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-2.0 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
Voltage on Any Pin to Ground Potential except A9	-2.0 to +7.0	V
Voltage on A9 Pin to Ground Potential	-2.0 to +13.0	V

Note: Exposure to conditions beyond those listed under Absolute maximum Ratings may adversely affect the life and reliability of the device.

TTL/NMOS Compatible

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} (Max.)	-	-	±1.0	µA
A9 Input Load Current	I_{LIT}	V_{CC} = V_{CC} (Max.), A9 = 13.0 V	-	-	50	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} (Max.)	-	-	±1.0	µA
V_{CC} Active Current (Note 1)	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	20	30	mA
V_{CC} Active Current (Note 2, 3)	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	30	40	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = V_{CC} (Max.), $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	0.4	1.0	mA
Input Low Voltage	V_{IL}	-	-0.5	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{CC} +0.5	V
Voltage for Autoselect and Temporary Sector Unprotected	V_{ID}	V_{CC} =5.25V	10.5	-	13.0	V
Output Low Voltage	V_{OL}	I_{OL} = 5.8 mA , V_{CC} = V_{CC} (Min.)	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = V_{CC} (Min.)	2.4	-	-	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	-	3.2	-	4.2	V

Note :

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Program or Erase Algorithm is in progress.
3. Not 100% tested.

CMOS Compatible

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} (Max.)	-	-	±1.0	µA
A9 Input Load Current	I_{LIT}	V_{CC} = V_{CC} (Max.), A9 = 13.0 V	-	-	50	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} (Max.)	-	-	±1.0	µA
V_{CC} Active Current (Note 1)	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	20	30	mA
V_{CC} Active Current (Note 2, 3)	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	30	40	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = V_{CC} (Max.), $\overline{CE}$ = VCC±0.5V	-	1	5	µA
Input Low Voltage	V_{IL}	-	-0.5	-	0.8	V
Input High Voltage	V_{IH}	-	0.7× V_{CC}	-	V_{CC} +0.3	V
Voltage for Autoselect and Temporary Sector Unprotected	V_{ID}	V_{CC} =5.25V	10.5	12	13.0	V
Output Low Voltage	V_{OL}	I_{OL} = 5.8 mA , V_{CC} = V_{CC} (Min.)	-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = V_{CC} (Min.)	0.85× V_{CC}	-	-	V
	V_{OH2}	I_{OH} = -100 µA, V_{CC} = V_{CC} (Min.)	V_{CC} - 0.4	-	-	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	-	3.2	-	4.2	V

Note :

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz).

   The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.

2. I_{CC} active while Embedded Program or Erase Algorithm is in progress.

3. Not 100% tested.

4. I_{CC3} = 20 µ (Max.) at extended temperatures (>+85°C)

TSOP and PLCC Pin Capacitance

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

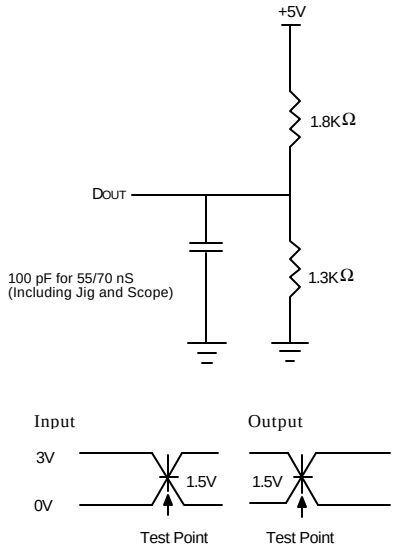
PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	7.5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0V	7.5	9	pF

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF for 55 nS, C_L = 100 pF for 70 nS

AC Test Load and Waveform



Read Cycle Timing Parameters

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.		W29D040C -55	W29D040C -70	UNIT
Read Cycle Time	T_{RC}	Min.	55	70	nS
Chip Enable Access Time	T_{CE}	Max.	55	70	nS
Address Access Time	T_{ACC}	Max.	55	70	nS
Output Enable Access Time	T_{OE}	Max.	30	30	nS
$\overline{CE}$ High to High-Z Output	T_{DF}	Max.	20	20	nS
$\overline{OE}$ High to High-Z Output	T_{DF}	Max.	20	20	nS
Output Hold from Address Change	T_{OH}	Min.	0	0	nS

Write Cycle Timing Parameters

PARAMETER		SYM.		W29D040C -55	W29D040C -70	UNIT
Write Cycle Time		TWC	Min.	55	70	nS
Address Setup Time		TAS	Min.	0	0	nS
Address Hold Time		TAH	Min.	40	45	nS
Data Setup Time		TDS	Min.	25	30	nS
Data Hold Time		TDH	Min.	0	0	nS
Output Enable Hold Time	Read	TOEH	Min.	0	0	nS
	Toggle and Data Polling		Min.	10	10	nS
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		TGHWL	Min.	0	0	nS
$\overline{CE}$ Setup Time		TCS	Min.	0	0	nS
$\overline{CE}$ Hold Time		TCH	Min.	0	0	nS
Write Pulse Width		TWP	Min.	30	35	nS
Write Pulse Width High		TWPH	Min.	20	20	nS
Byte Programming Operation		TWHWH1	Typ.	40	40	µS
Sector Erase Operation		TWHWH2	Typ.	30	30	mS
			Max.	4	4	sec
Chip Erase Operation		TWHWH3	Typ.	300	300	mS
			Max.	32	32	sec
VCC Set Up Time		TVCS	Min.	50	50	µS

Notes:

All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is V_{IH}.

(b) Low level signal's reference level is V_{IL}.

Write Cycle Timing Parameters

Alternate $\overline{CE}$ Controlled Writes

PARAMETER		SYM.		W29D040C -55	W29D040C -70	UNIT
Write Cycle Time		TWC	Min.	55	70	nS
Address Setup Time		TAS	Min.	0	0	nS
Address Hold Time		TAH	Min.	40	45	nS
Data Setup Time		TDS	Min.	25	30	nS
Data Hold Time		TDH	Min.	0	0	nS
Output Enable Setup Time		TOES	Min.	0	0	nS
Output Enable Hold Time	Read	TOEH	Min.	0	0	nS
	Toggle and Data Polling		Min.	10	10	nS
Read Recover Time Before Write		TGHEL	Min.	0	0	nS
$\overline{WE}$ Setup Time		TWS	Min.	0	0	nS
$\overline{WE}$ Hold Time		TWH	Min.	0	0	nS
$\overline{CE}$ Pulse Width		TCP	Min.	30	35	nS
$\overline{CE}$ Pulse Width High		TCPH	Min.	20	20	nS
Byte Programming Operation		TWHWH1	Typ.	40	40	µS
Sector Erase Operation		TWHWH2	Typ.	30	30	mS
			Max.	4	4	sec
Chip Erase Operation		TWHWH3	Typ.	300	300	mS
			Max.	32	32	sec
VCC Set Up Time		TVCS	Min.	50	50	µS

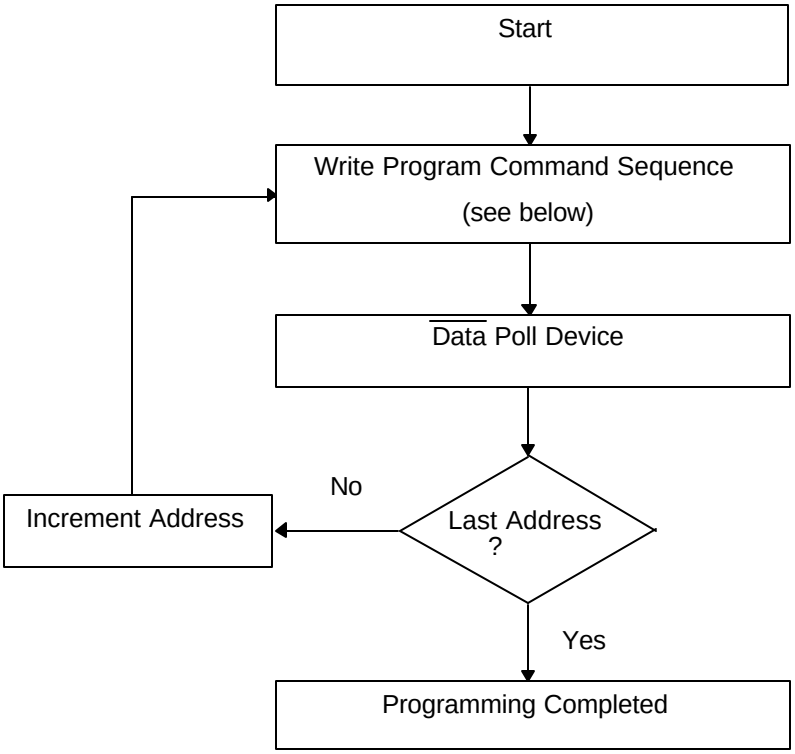
Notes:

All AC timing signals observe the following guidelines for determining setup and hold times:

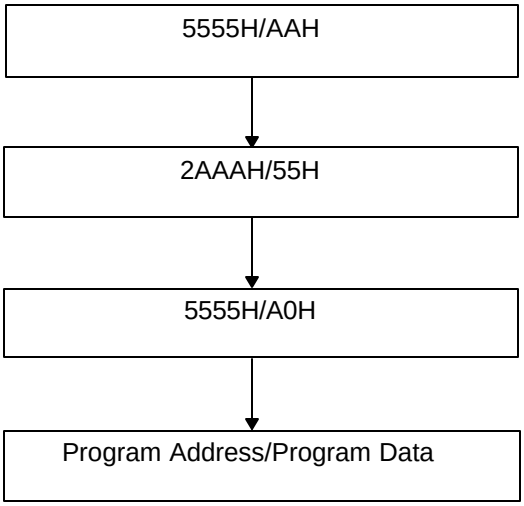
(a) High level signal's reference level is V_{IH}.

(b) Low level signal's reference level is V_{IL}.

EMBEDDED ALGORITHMS

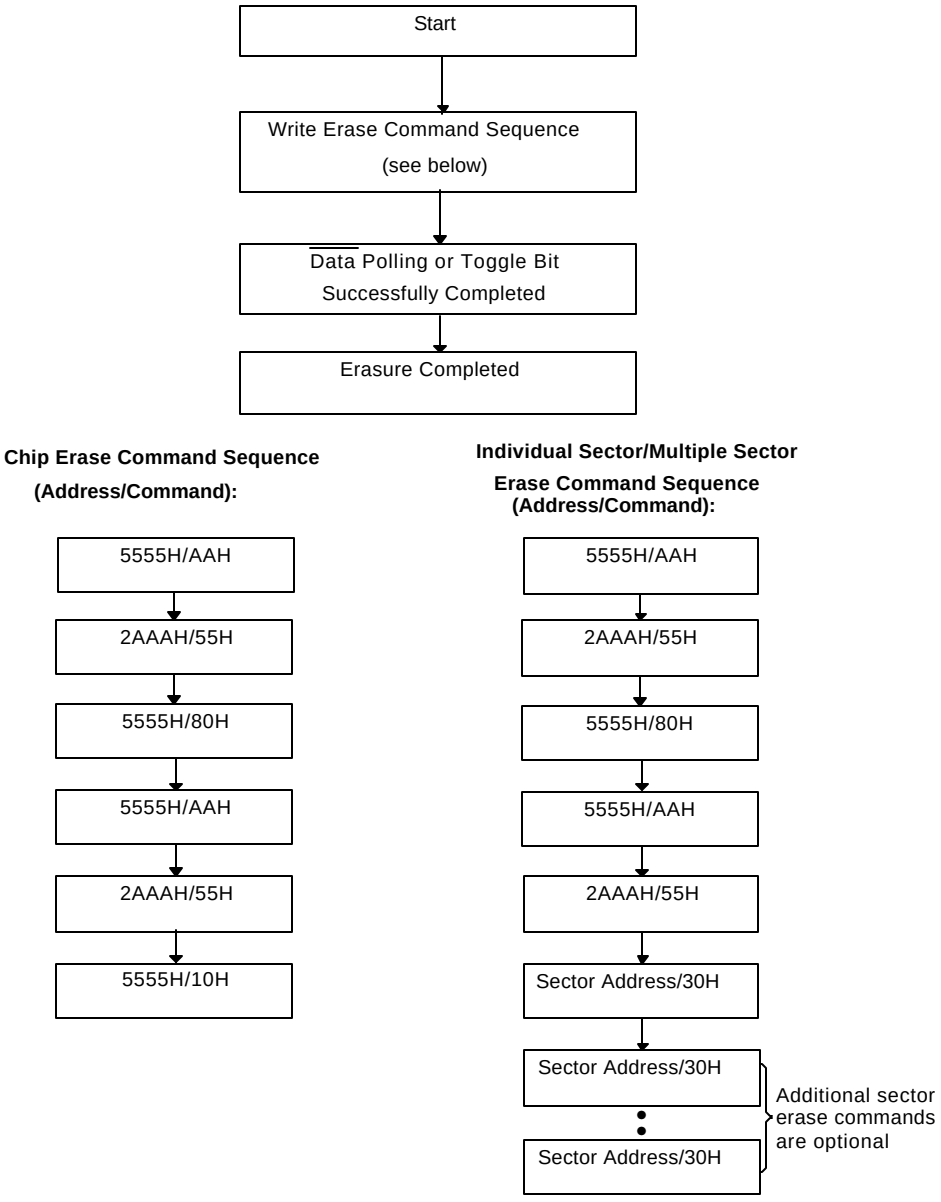


Program Command Sequence (Address/Command):



Embedded Programming Algorithm

EMBEDDED ALGORITHMS

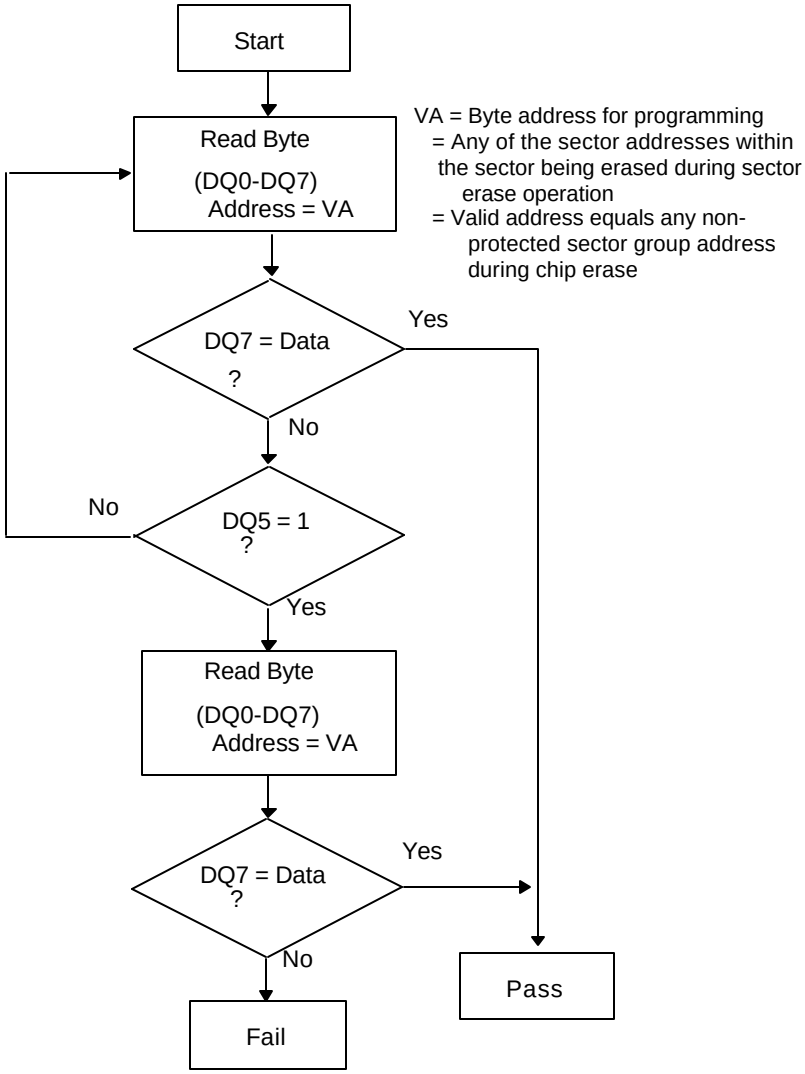


Embedded Erase Algorithm

Note:

To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

EMBEDDED ALGORITHMS

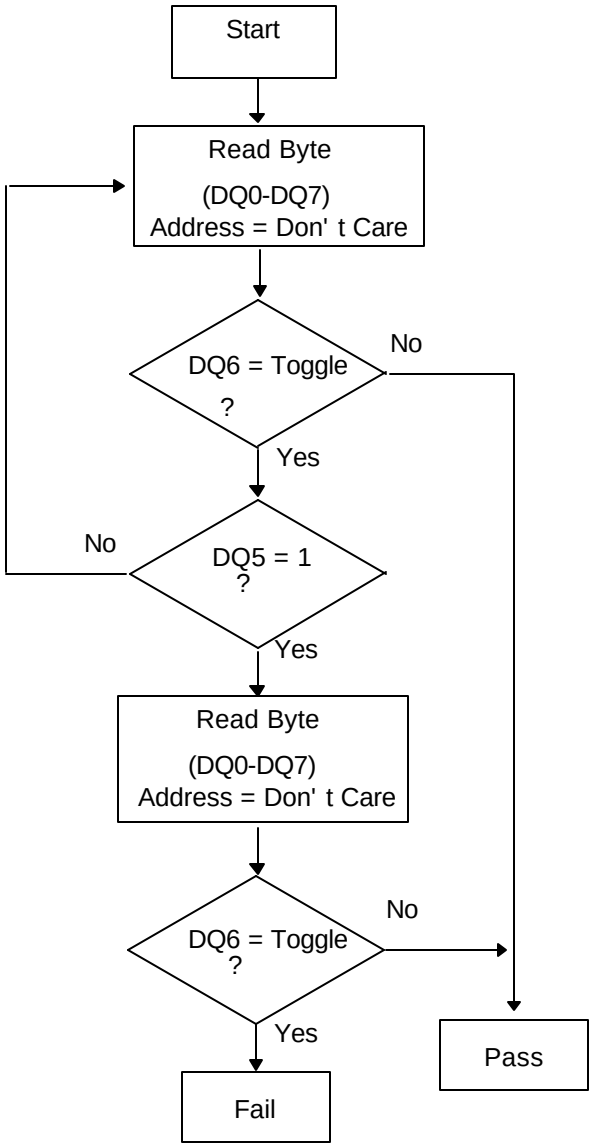


$\overline{\text{Data}}$ Polling Algorithm

Note:

DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

EMBEDDED ALGORITHMS



Toggle Bit Algorithm

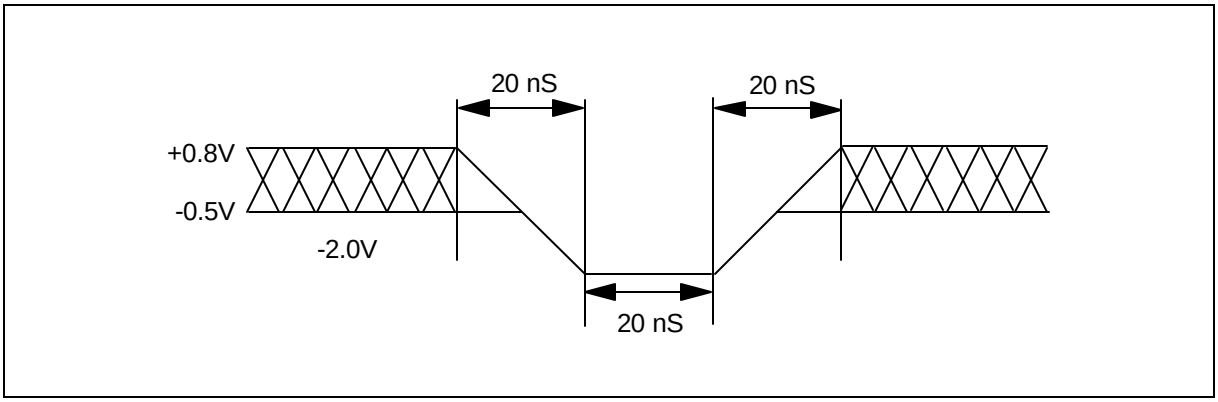
Note:

DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1". 1 .

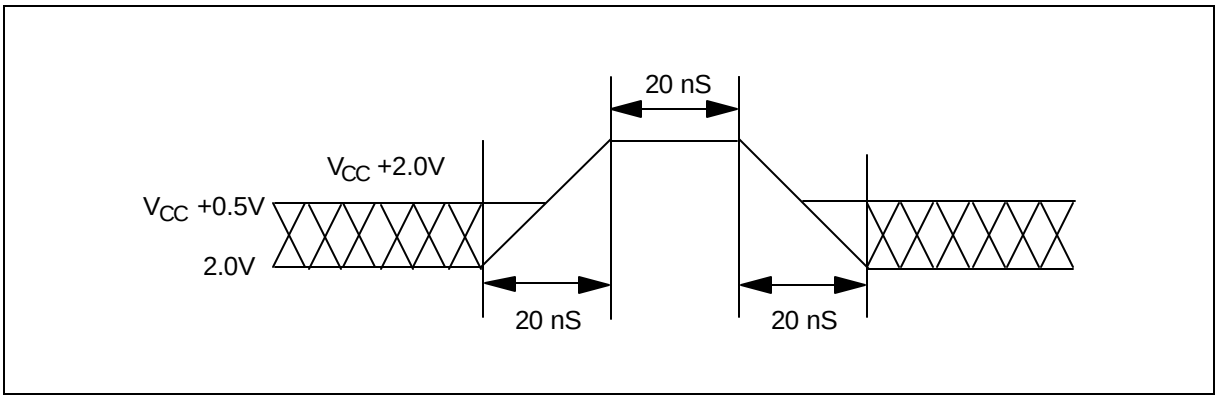
Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off"State

Maximum Negative Overshoot Waveform

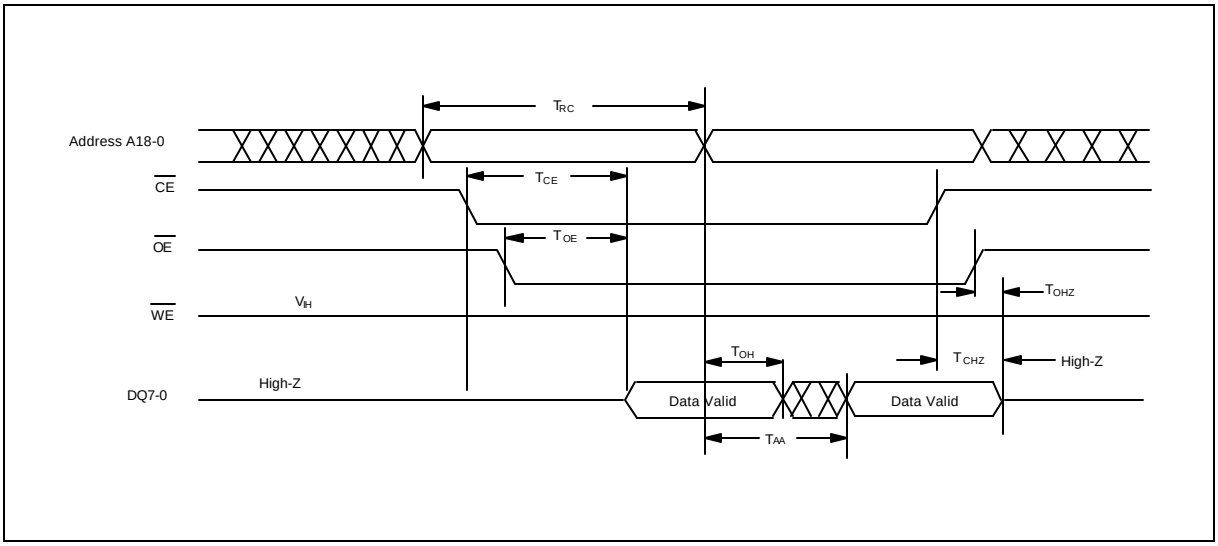


Maximum Positive Overshoot Waveform

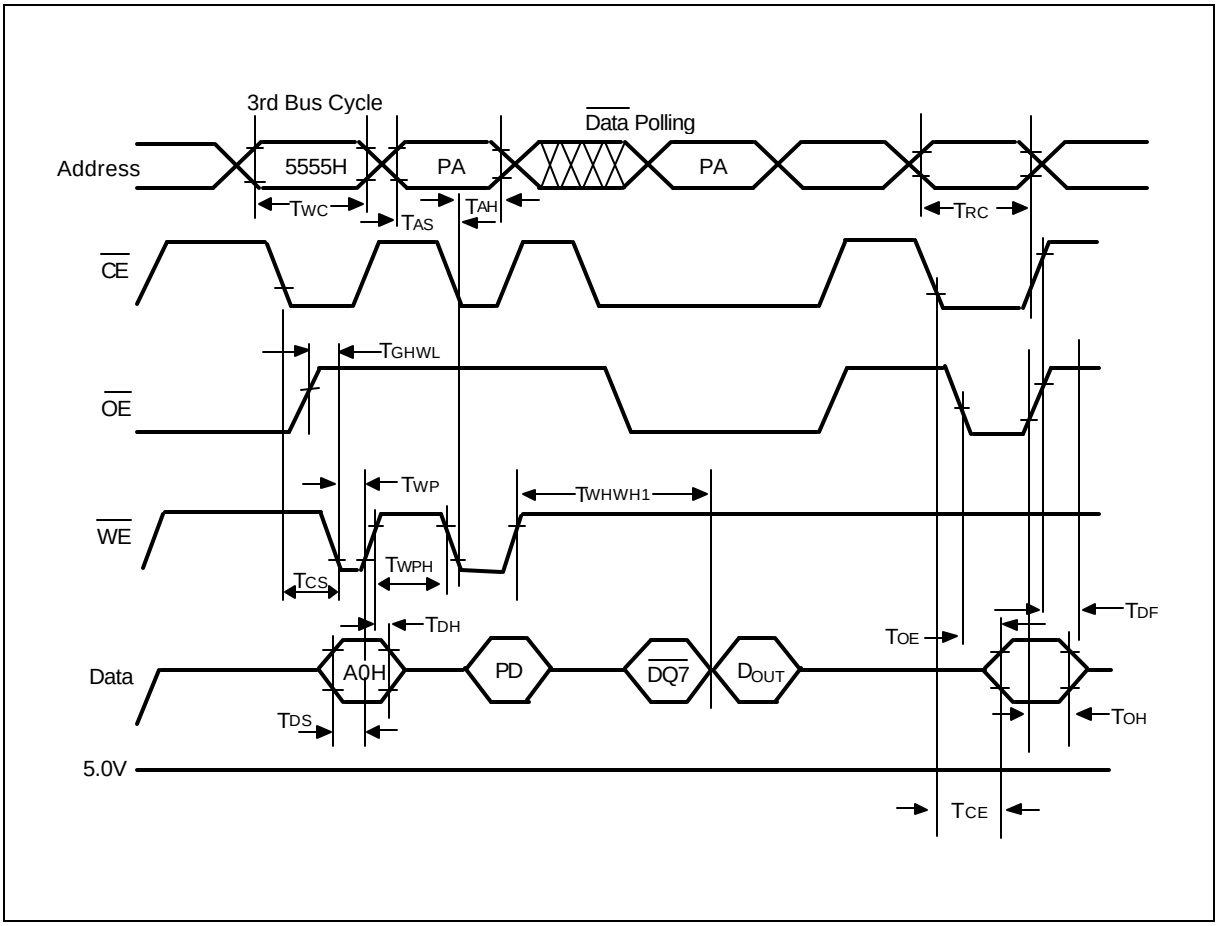


TIMING WAVEFORMS

Read Cycle Timing Diagram



$\overline{WE}$ Controlled Program Cycle Timing Diagram

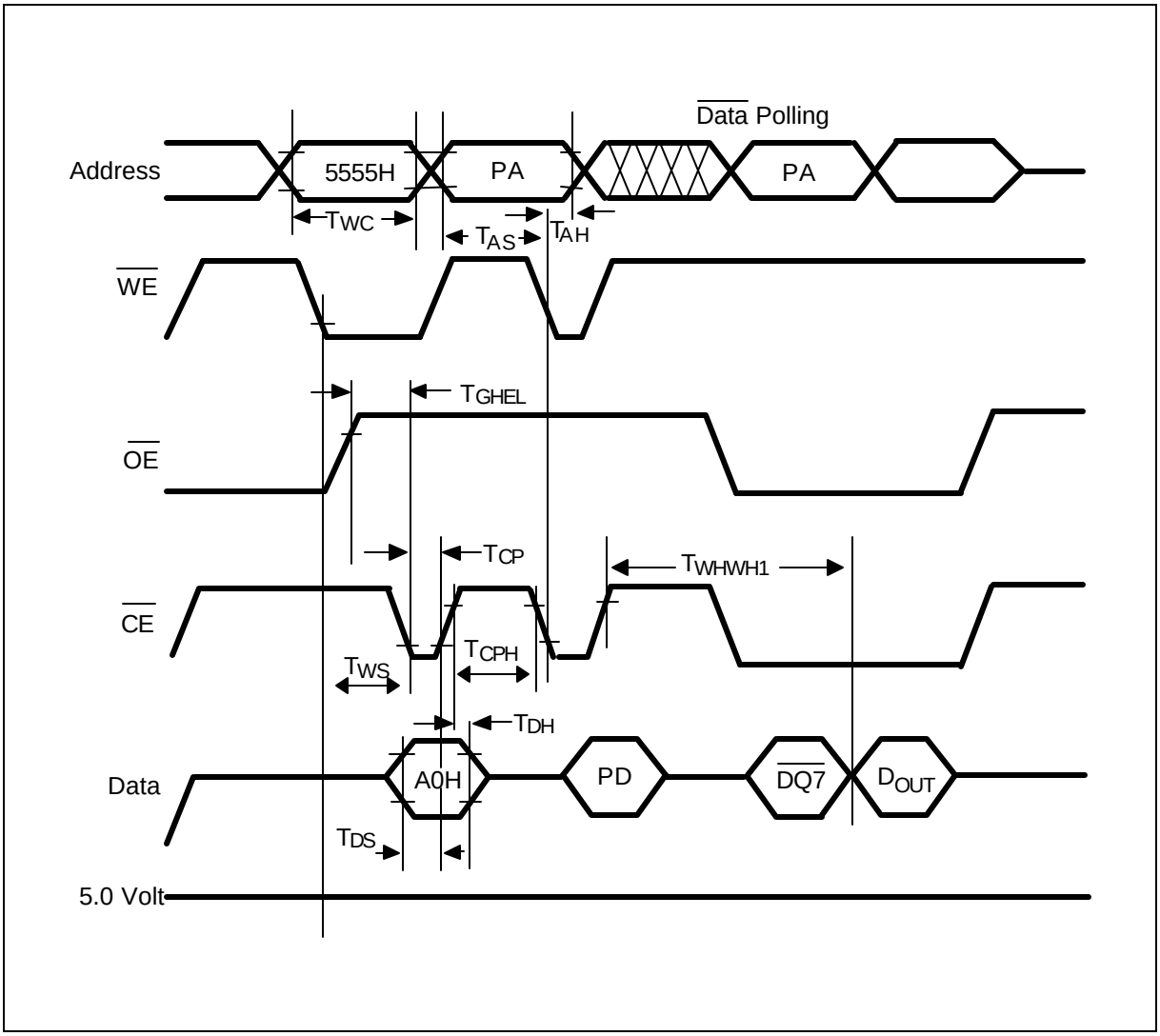


Note:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the x 16 mode.

Timing Waveforms, continued

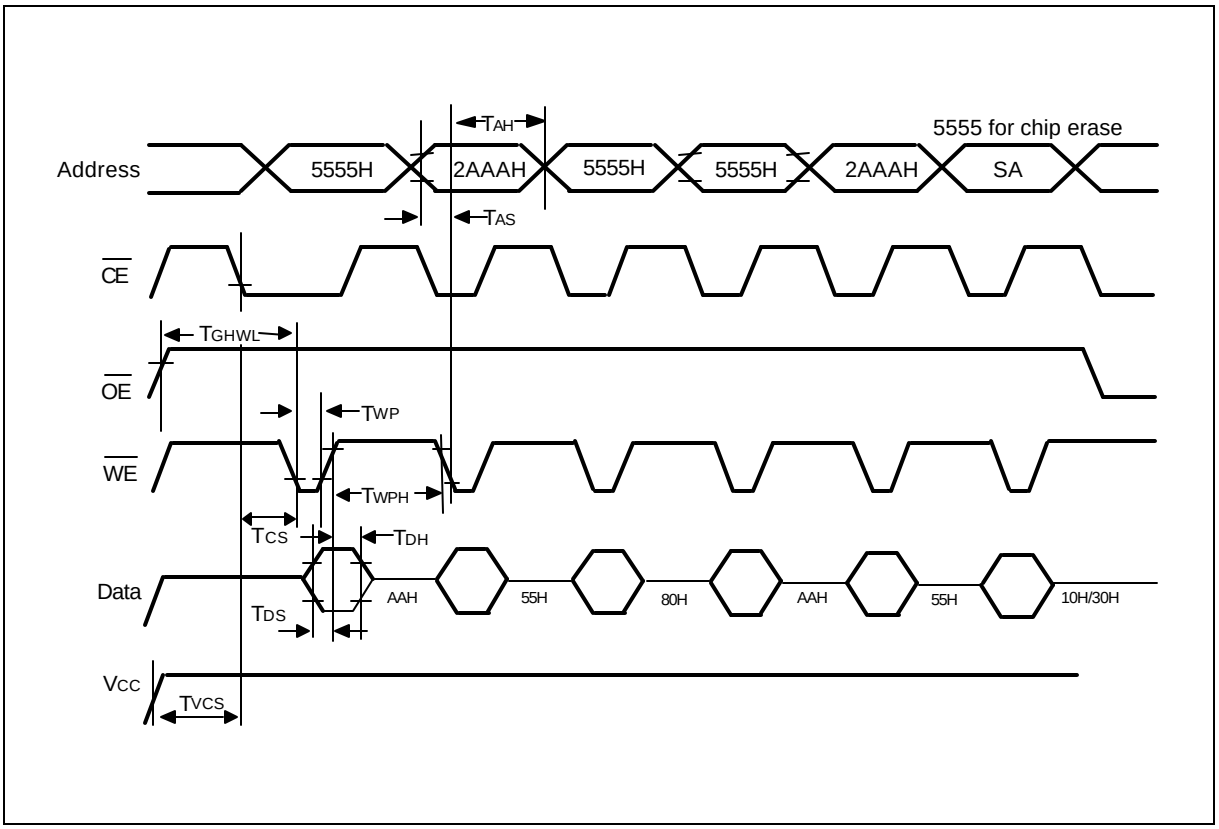
$\overline{CE}$ Controlled Program Cycle Timing Diagram



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four cycle sequence.
6. These waveforms are for the x 16 mode.

Chip/Sector Erase Cycle Timing Diagram

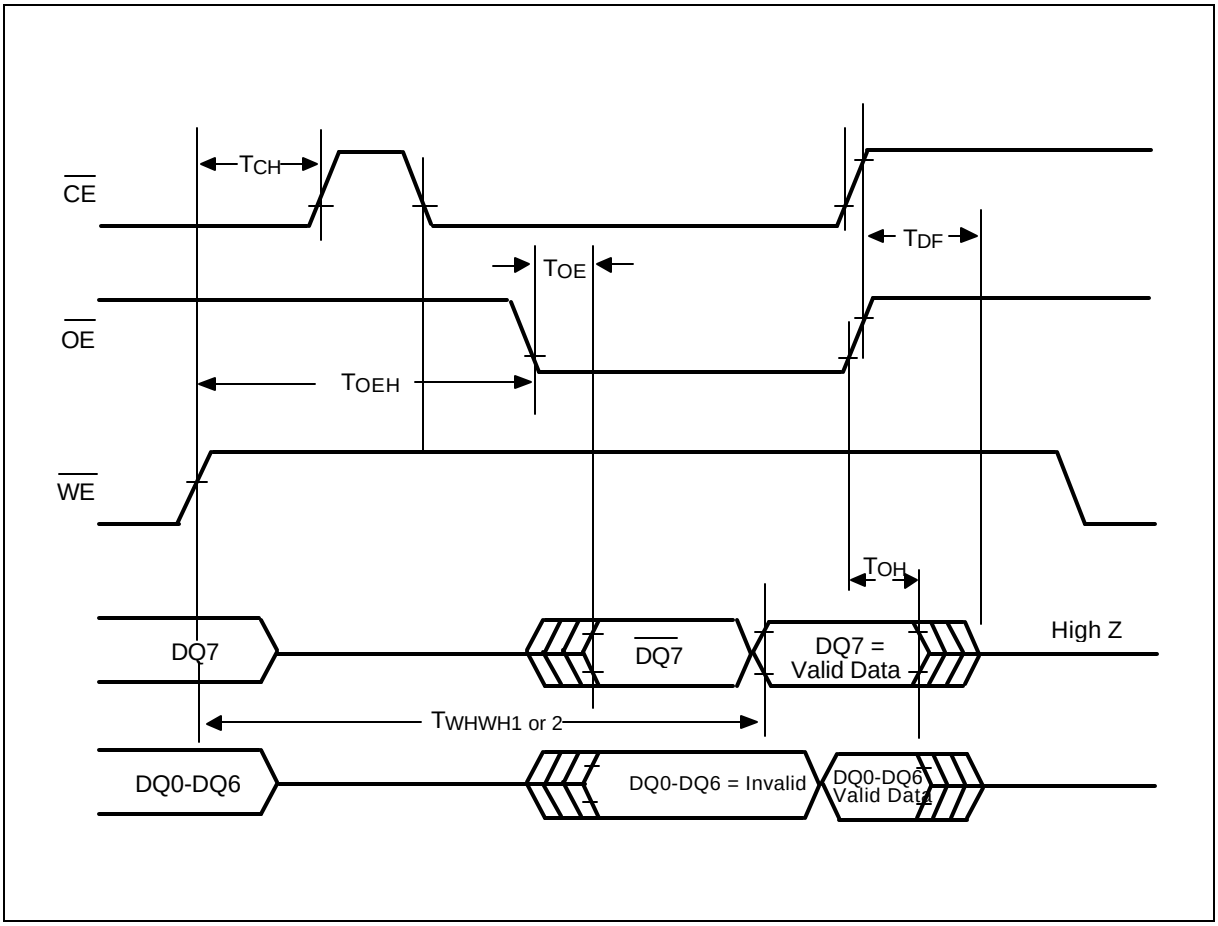


Note:

1. SA is the sector address for Sector Erase.
2. These waveforms are for the x 16 mode.

Timing Waveforms, continued

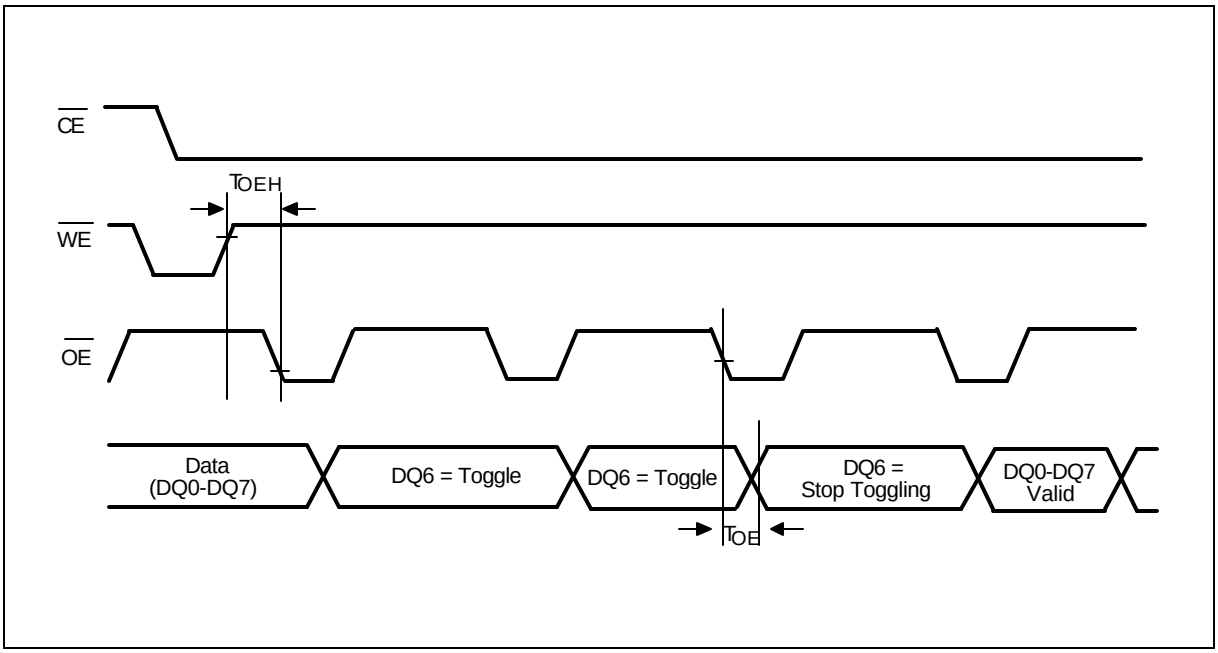
$\overline{\text{DATA}}$ Polling (During Embedded Algorithm) Timing Diagram



Note:

∗ DQ7 = Valid Data (The device has completed the Embedded operation).

Toggle Bit During Embedded Algorithm Timing Diagram



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (mA)	PACKAGE	CYCLE
W29D040C-55C	55	60	1	32-pin DIP	100K
W29D040C-70C	70	60	1	32-pin DIP	100K
W29D040CP55C	55	60	1	32-pin PLCC	100K
W29D040CP70C	70	60	1	32-pin PLCC	100K
W29D040CT55C	55	60	1	32-pin TSOP	100K
W29D040CT70C	70	60	1	32-pin TSOP	100K

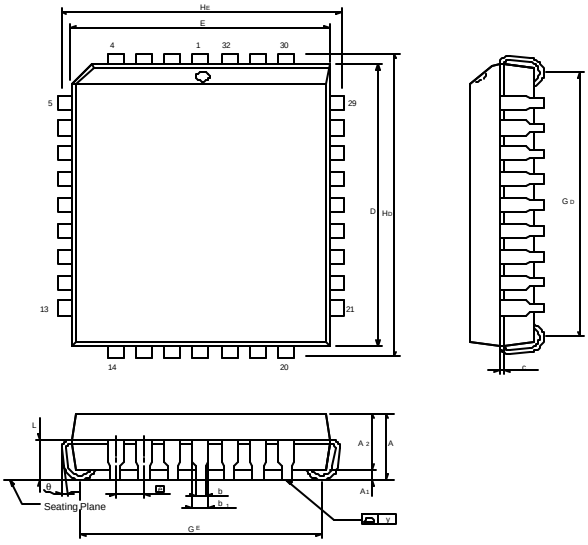
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

Winbond Electronics Corp.

PACKAGE DIMENSIONS

32-pin PLCC

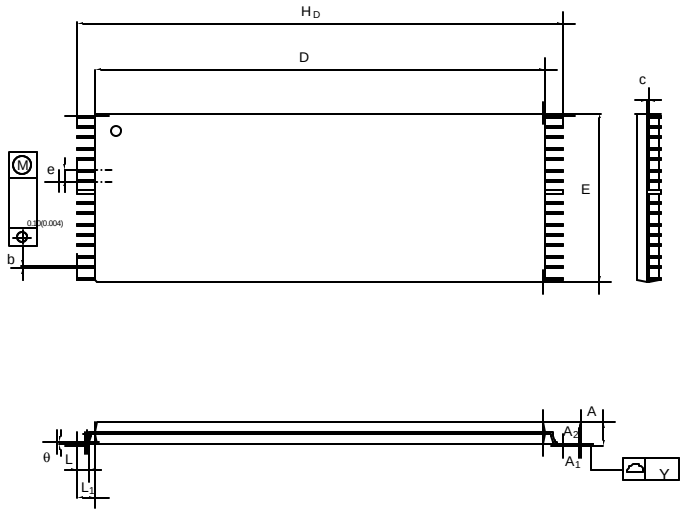


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection sepc.

32-pin TSOP



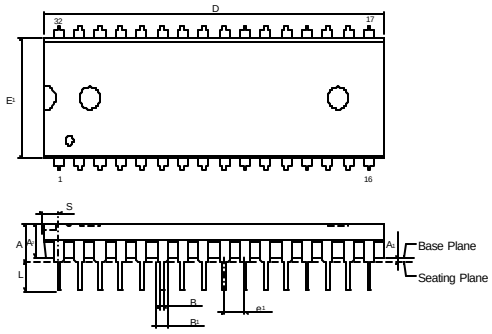
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:

Controlling dimension: Millimeters

Package Dimensions, continued

32-pin PDIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold flash
   tie bar burrs.
2. Dimension E1 does not include interlead fl
3. Dimensions D & E1 include mold mismatcl
   are determined at the mold parting line.
4. Dimension B1 does not include dambar
   protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be basec
   final visual inspection spec.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jan. 1999		Initial Issued

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Note: All data and specifications are subject to change without notice.