

## DESCRIPTION

The HY62V8200B is a high speed, low power and 2M bit CMOS SRAM organized as 262,144 words by 8bit. The HY62V8200B uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

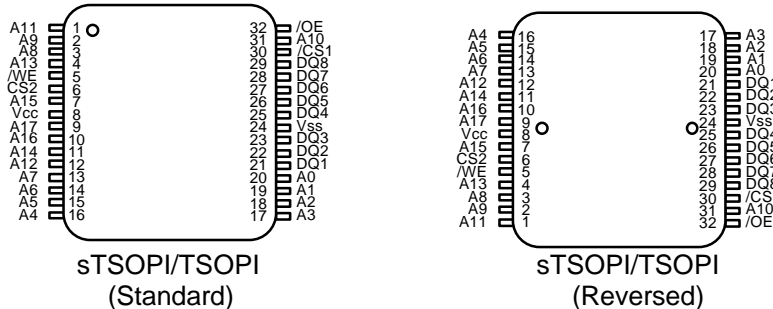
## FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup( LL-part )
  - . 2.0V(min) data retention
- Standard pin configuration
  - . 32-sTSOPI-8X13.4, 32-TSOPI -8X20 (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)	Temperature (°C)
HY62V8200B	3.0~3.6	70/85/100	5	25	0~70
HY62V8200B-E	3.0~3.6	70/85/100	5	25	-25~85(E)
HY62V8200B-I	3.0~3.6	70/85/100	5	25	-40~85(I)

Note 1. Blank : Commercial, E : Extended, I : Industrial  
 2. Current value is max.

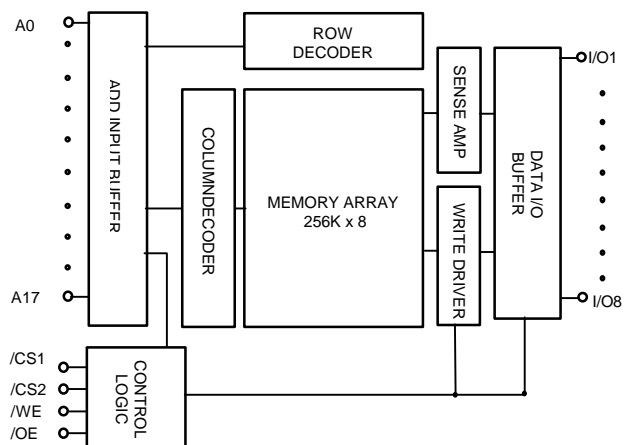
## PIN CONNECTION



## PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A17	Address Input
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(3.0V~3.6V)
Vss	Ground

## BLOCK DIAGRAM



**ORDERING INFORMATION**

Part No.	Speed	Power	Temp.	Package
HY62V8200BLLT1	70/85/100	LL-part		TSOPI(Standard)
HY62V8200BLLR1	70/85/100	LL-part		TSOPI(Reversed)
HY62V8200BLLST	70/85/100	LL-part		Smaller TSOPI(Standard)
HY62V8200BLLSR	70/85/100	LL-part		Smaller TSOPI(Reversed)
HY62V8200BLLT1-E	70/85/100	LL-part	E	TSOPI(Standard)
HY62V8200BLLR1-E	70/85/100	LL-part	E	TSOPI(Reversed)
HY62V8200BLLST-E	70/85/100	LL-part	E	Smaller TSOPI(Standard)
HY62V8200BLLSR-E	70/85/100	LL-part	E	Smaller TSOPI(Reversed)
HY62V8200BLLT1-I	70/85/100	LL-part	I	TSOPI(Standard)
HY62V8200BLLR1-I	70/85/100	LL-part	I	TSOPI(Reversed)
HY62V8200BLLST-I	70/85/100	LL-part	I	Smaller TSOPI(Standard)
HY62V8200BLLSR-I	70/85/100	LL-part	I	Smaller TSOPI(Reversed)

Note 1. Blank : Commercial, E : Extended, I : Industrial

**ABSOLUTE MAXIMUM RATING (1)**

Symbol	Parameter	Rating	Unit	Remark
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.2 to 3.9	V	
V <sub>CC</sub>	Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub>	-0.2 to 4.0	V	
T <sub>A</sub>	Operating Temperature	0 to 70	°C	HY62V8200B
		-25 to 85	°C	HY62V8200B-E
		-40 to 85	°C	HY62V8200B-I
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C	
P <sub>D</sub>	Power Dissipation	1.0	W	
I <sub>OUT</sub>	Data Output Current	50	mA	
T <sub>SOLDER</sub>	Lead Soldering Temperature & Time	260 • 5	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**TRUTH TABLE**

/CS1	CS2	/WE	/OE	Mode	I/O	Power
H	X	X	X	Deselected	High-Z	Standby
X	L	X	X	Deselected	High-Z	Standby
L	H	H	H	Output Disabled	High-Z	Active
L	H	H	L	Read	Dout	Active
L	H	L	X	Write	DIN	Active

Note :

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=don't care(V<sub>IH</sub> or V<sub>IL</sub>)

**RECOMMENDED DC OPERATING CONDITION**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.2	V
V <sub>IL</sub>	Input Low Voltage	-0.2(1)	-	0.4	V

Note

 1. V<sub>IL</sub> = -1.5V for pulse width less than 30ns

**DC ELECTRICAL CHARACTERISTICS**

 V<sub>CC</sub> = 3.0~3.6V, T<sub>A</sub> = 0°C to 70°C / -25°C to 85°C (E) / -40°C to 85°C (I), unless otherwise specified

Sym.	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	1	uA	
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , /CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-1	-	1	uA	
I <sub>CC</sub>	Operating Power Supply Current	/CS1 = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	-	5	mA	
I <sub>CC1</sub>	Average Operating Current	Min Duty Cycle = 100%, /CS1 = V <sub>IL</sub> CS2 = V <sub>IH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	70ns	-	-	60	mA
			85ns	-	-	50	mA
			100ns	-	-	50	mA
			Cycle time = 1us, I <sub>I/O</sub> = 0mA, /CS1 ; $\hat{A}$ 0.2V, CS2 ; $\hat{A}$ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ; $\hat{A}$ 0.2V or V <sub>IN</sub> ; $\hat{A}$ V <sub>CC</sub> - 0.2V	-	-	6	mA
I <sub>SB</sub>	TTL Standby Current (TTL Input)	/CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> -	-	-	0.5	mA	
I <sub>SB1</sub>	Standby Current (CMOS Input)	HY62V8200B	/CS1 ≥ V <sub>CC</sub> - 0.2V, CS2 ≥ 0.2V or CS2 ≥ V <sub>CC</sub> - 0.2V	-	-	25	uA
		HY62V8200B-E		-	-	25	uA
		HY62V8200B-I		-	-	25	uA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.2	-	-	V	

 Note : Typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C

**CAPACITANCE**

(Temp = 25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I/O</sub> = 0V	10	pF

Note : These parameters are sampled and not 100% tested

### AC CHARACTERISTICS

V<sub>CC</sub>= 2.7V~3.6V, T<sub>A</sub> = 0°C to 70°C/ -25°C to 85°C(E)/ -40°C to 85°C(I), unless otherwise specified

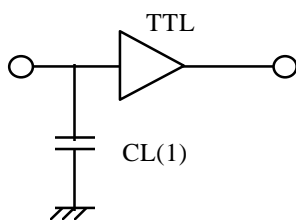
#	Symbol	Parameter	-70		-85		-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
1	t <sub>RC</sub>	Read Cycle Time	70	-	85	-	100	-	ns
2	t <sub>AA</sub>	Address Access Time	-	70	-	85	-	100	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	70	-	85	-	100	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	40	-	45	-	50	ns
5	t <sub>CLZ</sub>	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	t <sub>CHZ</sub>	Chip Deselection to Output in High Z	0	20	0	25	0	30	ns
8	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	t <sub>OH</sub>	Output Hold from Address Change	15	-	15	-	15	-	ns
WRITE CYCLE									
10	t <sub>WC</sub>	Write Cycle Time	70	-	85	-	100	-	ns
11	t <sub>CW</sub>	Chip Selection to End of Write	60	-	70	-	80	-	ns
12	t <sub>AW</sub>	Address Valid to End of Write	60	-	70	-	80	-	ns
13	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	0	-	ns
14	t <sub>WP</sub>	Write Pulse Width	50	-	60	-	70	-	ns
15	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	ns
16	t <sub>WHZ</sub>	Write to Output in High Z	0	20	0	25	0	30	ns
17	t <sub>DW</sub>	Data to Write Time Overlap	35	-	35	-	40	-	ns
18	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	5	-	ns

### AC TEST CONDITIONS

T<sub>A</sub> = 0°C to 70°C / -25°C to 85°C (E)/ -40°C to 85°C (I), unless otherwise specified

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
	CL = 100pF + 1TTL Load

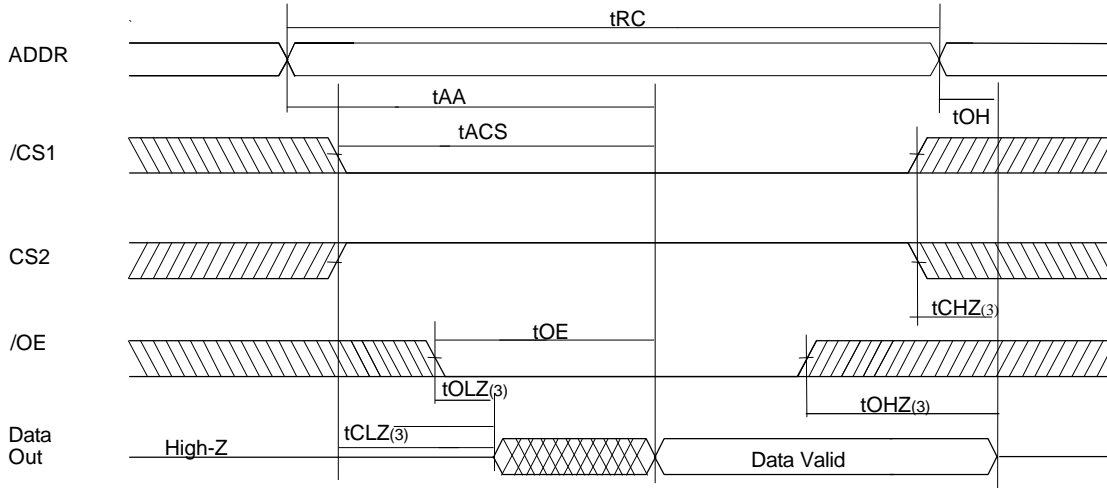
### AC TEST LOADS



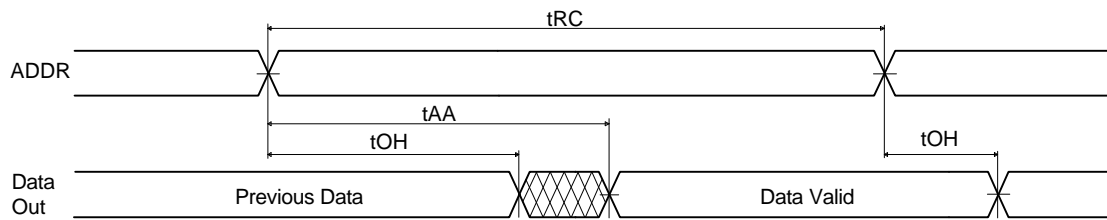
Note : 1 Including jig and scope capacitance

**TIMING DIAGRAM**

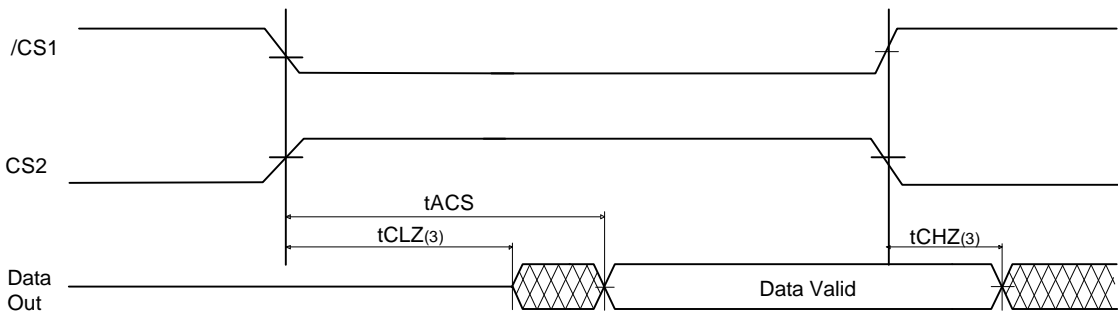
**READ CYCLE 1 (Note1,4)**



**READ CYCLE 2 (Note 1,2,4)**



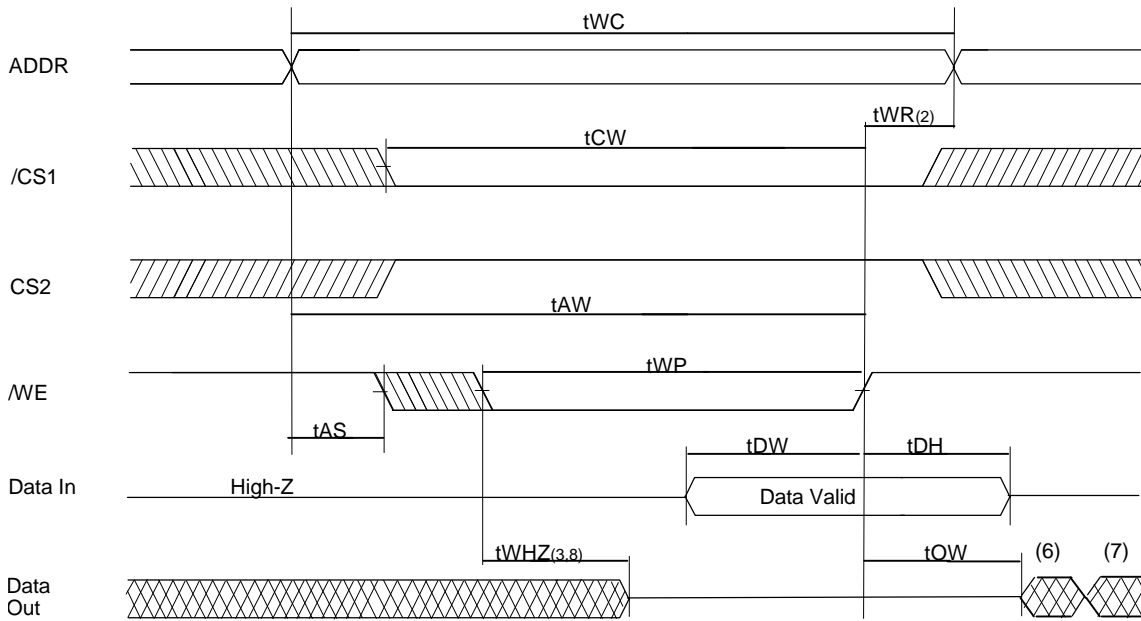
**READ CYCLE 3 (Note 1,2,4)**



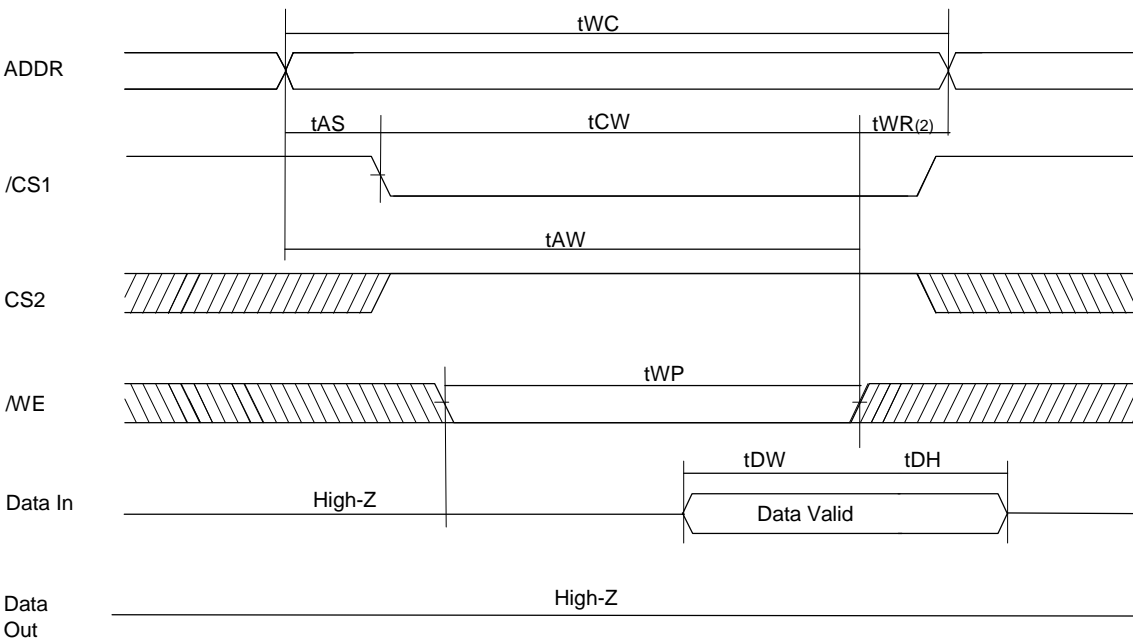
**Notes:**

1. Read Cycle occurs whenever a high on the /WE and /OE is low /CS1 and CS2 are in active status.
2. /OE = V<sub>IL</sub>
3. Transition is measured ; 200mV from steady state voltage.  
This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active  
CS2 in low for the standby, high for active

**WRITE CYCLE 1(1,4,5,9) (/WE Controlled)**



**WRITE CYCLE 1(1,4,5,9) (/CS1, CS2 Controlled)**



## Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low  $/CS1$ ,  $CS2$  and low  $/WE$ . A write begins at the latest transition among  $/CS1$  going low,  $CS2$  going high and  $/WE$  going low: A write ends at the earliest transition among  $/CS1$  going high,  $CS2$  low and  $/WE$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of  $/CS1$  going low or  $CS2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  is applied in case a write ends as  $/CS1$ , or  $/WE$  going high, and  $t_{WR2}$  is applied in case a write ends at  $CS2$  going low.
5. If  $/OE$ ,  $CS2$  and  $/WE$  are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If  $/CS1$  goes low simultaneously with  $/WE$  going low, the outputs remain in high impedance state.
7.  $Dout$  is the read data of the new address.
8. When  $/CS1$  is low and  $CS2$  is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

**DATA RETENTION ELECTRIC CHARACTERISTIC**

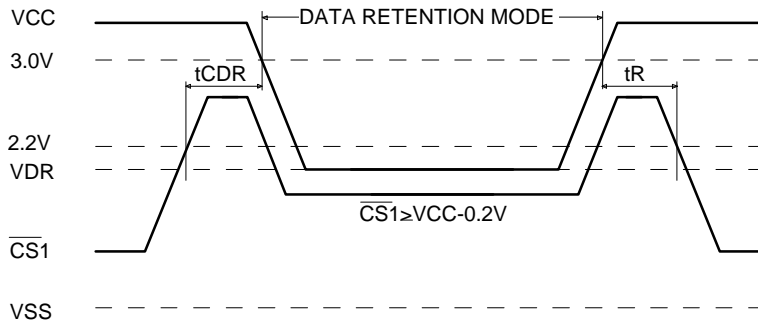
TA = 0°C to 70°C / -25°C to 85°C (E) / -40°C to 85°C (I)

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
VDR	Vcc for Data Retention		$/CS1 \geq V_{CC} - 0.2V, CS2 \leq 0.2V$ or $\geq V_{CC} - 0.2V, V_{SS} \leq V_{IN} \leq V_{CC}$	2.0	-	-	V
ICCDR	Data Retention Current	HY62V8200B	$V_{CC} = 3.0V, /CS1 \geq V_{CC} - 0.2V, CS2 \leq 0.2V$ or $\geq V_{CC} - 0.2V, V_{SS} \leq V_{IN} \leq V_{CC}$	-	-	25	uA
		HY62V8200B-E		-	-	25	uA
		HY62V8200B-I		-	-	25	uA
Tcdr	Chip Deselect to Data Retention Time		See Data Retention Timing Diagram	0	-	-	ns
Tr	Operating Recovery Time			5	-	-	ms

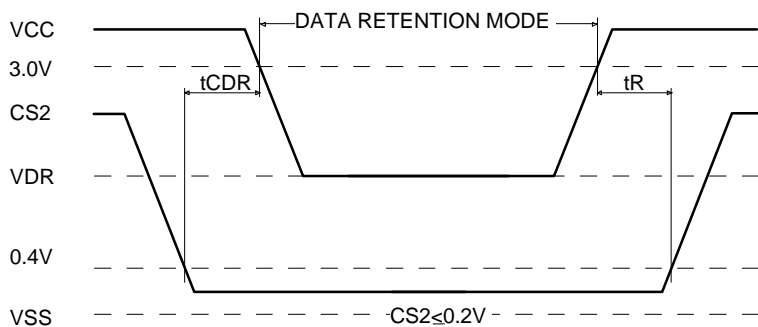
Notes:

1. Typical values are under the condition of TA = 25°C.

**DATA RETENTION TIMING DIAGRAM 1**



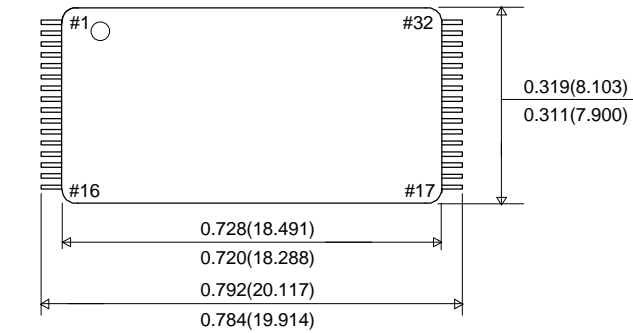
**DATA RETENTION TIMING DIAGRAM 2**



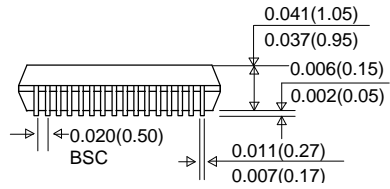
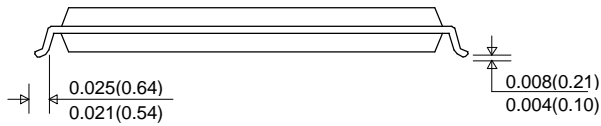


**PACKAGE INFORMATION**

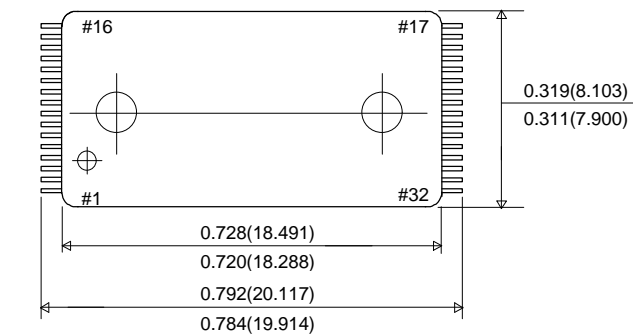
32pin 8x20mm Thin Small Outline Package Standard(T1)



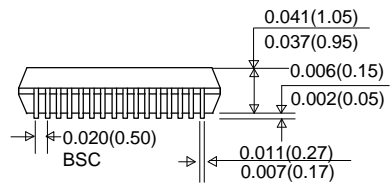
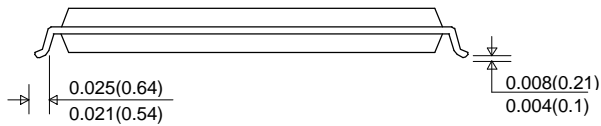
UNIT : INCH(mm)



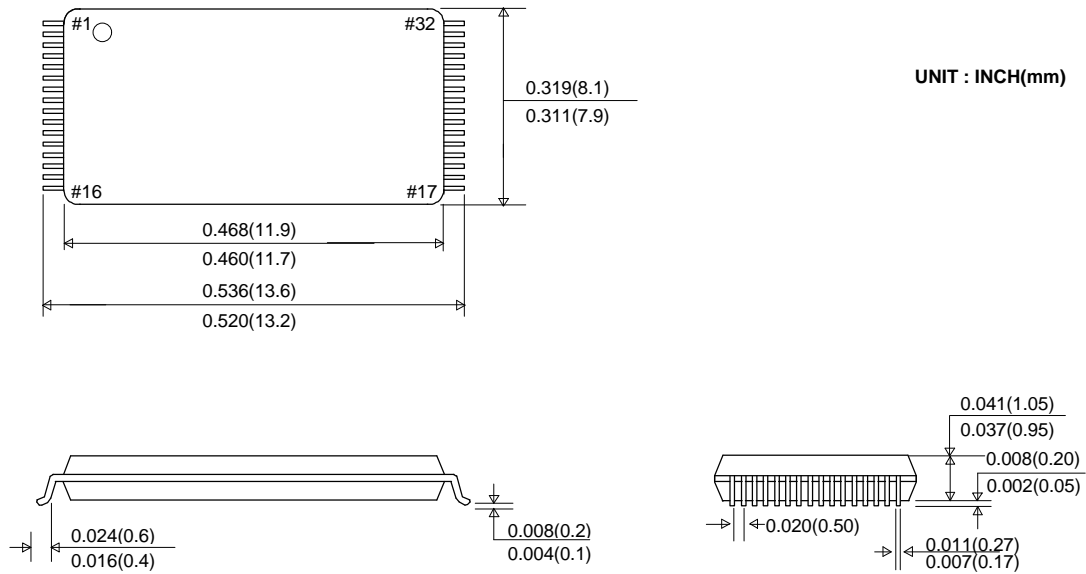
32pin 8x20mm Thin Small Outline Package Reversed(R1)



UNIT : INCH(mm)



32pin 8x13.4mm Smaller Thin Small Outline Package Standard(ST)



32pin 8x13.4mm Smaller Thin Small Outline Package Reversed (SR)

