

DM74LS112A

Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

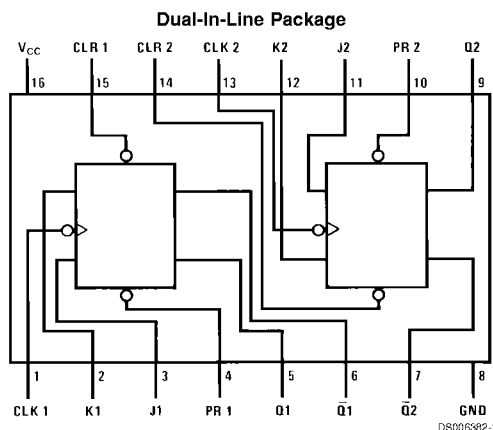
This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as the setup and hold times are

not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (54LS112) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



Order Number 54LS112DMQB, 54LS112FMQB,
54LS112LMQB, DM54LS112AJ, DM54LS112AW,
DM74LS112AM or DM74LS112AN
See Package Number E20A,
J16A, M16A, N16E or W16A

DM74LS112A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	\bar{Q}_0

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V	DM54LS and 54LS	-55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS112A			DM74LS112A			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
f _{CLK}	Clock Frequency (Note 4)	0		30	0		30	MHz
f _{CLK}	Clock Frequency (Note 5)	0		25	0		25	MHz
t _w	Pulse Width (Note 4)	Clock High	20		20			ns
		Preset Low	25		25			
		Clear Low	25		25			
t _w	Pulse Width (Note 5)	Clock High	25		25			ns
		Preset Low	30		30			
		Clear Low	30		30			
t _{SU}	Setup Time (Notes 3, 4)	20↓			20↓			ns
t _{SU}	Setup Time (Notes 3, 5)	25↓			25↓			ns
t _H	Hold Time (Notes 3, 4)	0↓			0↓			ns
t _H	Hold Time (Notes 3, 5)	5↓			5↓			ns
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 4: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 5: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max	DM54	2.5	3.4	V
		V _{IL} = Max, V _{IH} = Min	DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max	DM54		0.25	V
		V _{IL} = Max, V _{IH} = Min	DM74		0.35	
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.25	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V	J, K		0.1	mA
			Clear		0.3	
			Preset		0.3	
			Clock		0.4	
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V	J, K		20	μA
			Clear		60	
			Preset		60	
			Clock		80	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$	J, K			-0.4	mA
			Clear			-0.8	
			Preset			-0.8	
			Clock			-0.8	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 7)	DM54	-20		-100	mA
			DM74	-20		-100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 8)		4	6	mA	

Switching Characteristics

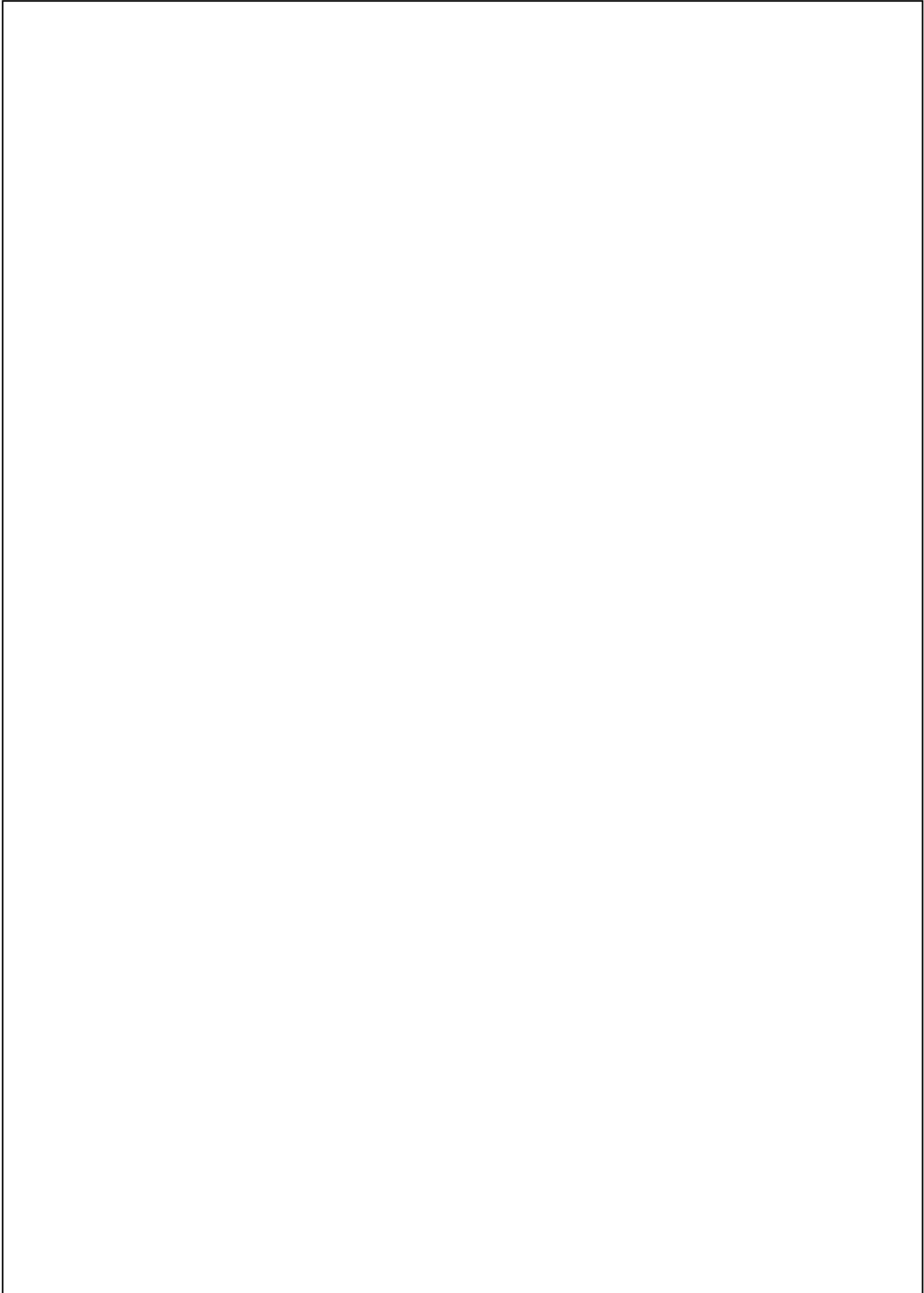
at $V_{CC} = 5V$ and $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to \bar{Q}		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to \bar{Q}		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or \bar{Q}		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or \bar{Q}		20		28	ns

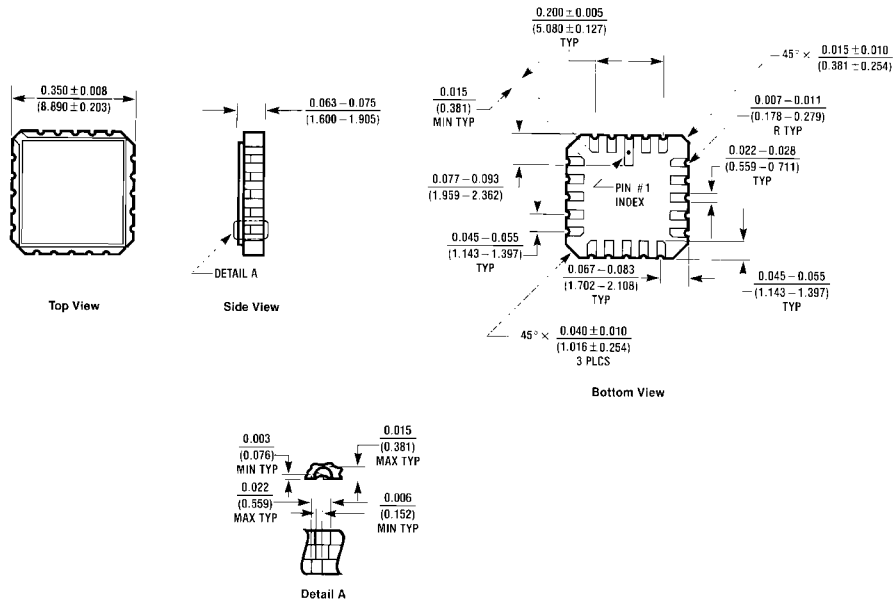
Note 6: All typicals are at $V_{CC} = 5V, T_A = 25^\circ C$.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $V_O = 2.25V$ and $2.125V$ for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

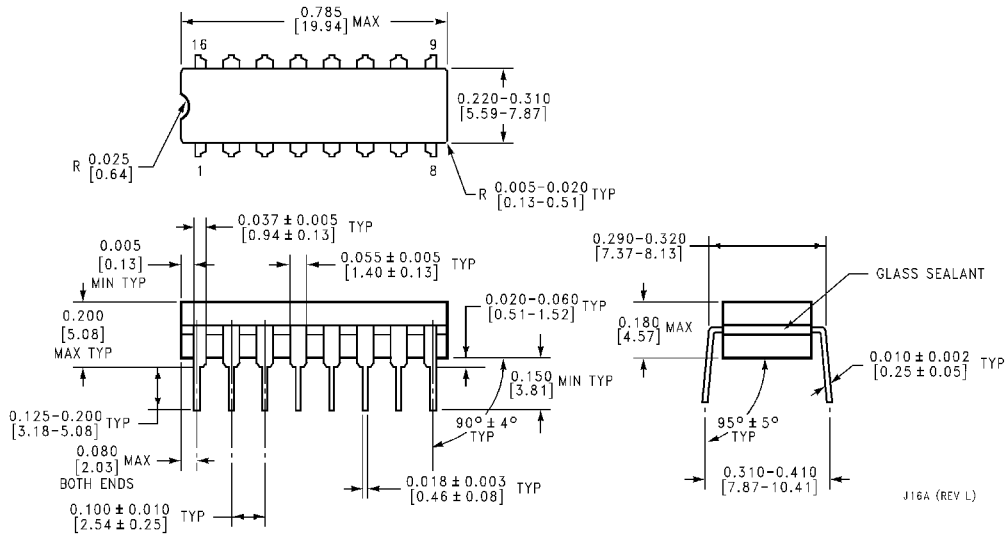
Note 8: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement the clock is grounded.



Physical Dimensions inches (millimeters) unless otherwise noted

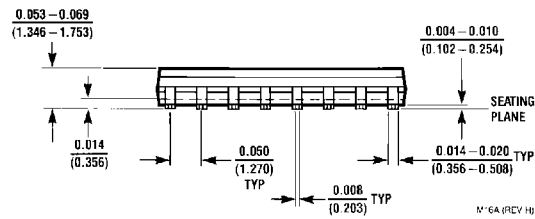
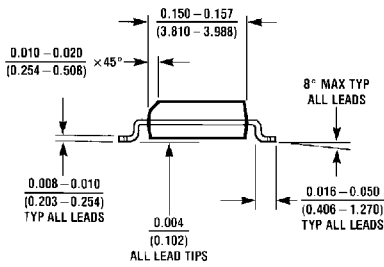
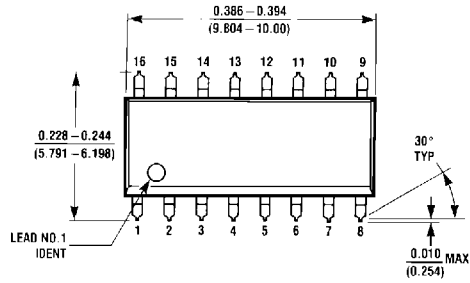


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS112LMQB
Package Number E20A

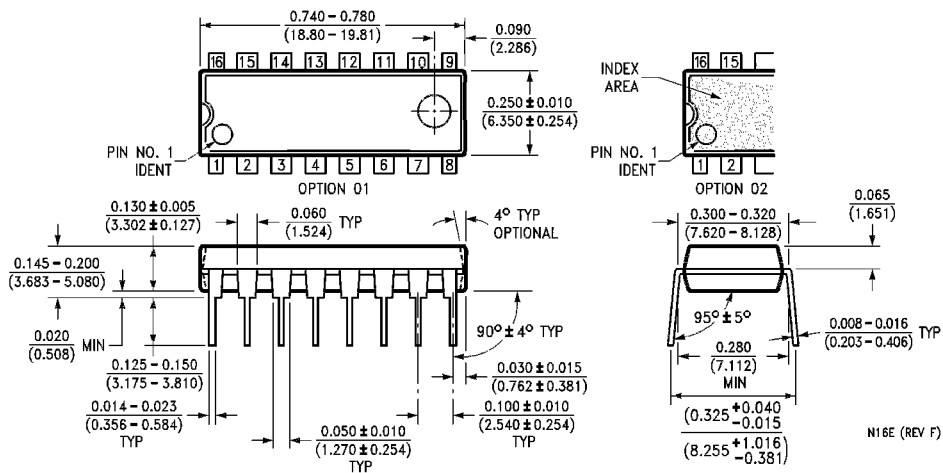


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS112DMQB or DM54LS112AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



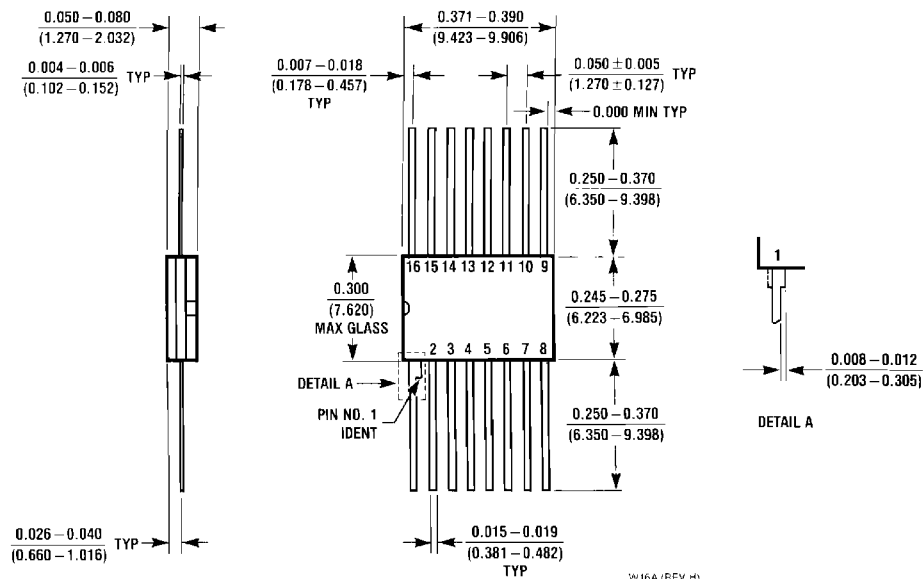
16-Lead Small Outline Molded Package (M)
Order Number DM74LS112AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS112AN
Package Number N16E

DM74LS112A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS112FMQB or DM54LS112AW
Package Number W16A

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