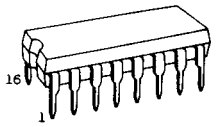
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

# TC40H375P/F

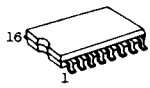
## TC40H375 4-BIT BISTABLE LATCH

The TC40H375 is a 4-bit latch having ENABLE input terminal common in two circuits.

When ENABLE input is at "H" level, DATA input is transmitted to output as it is. If ENABLE input is transfered from "H" level to "L" level, latch holds input DATA immediately before falling. When ENABLE input is at "L" level, output does not change even if input DATA changes.




DIP16(3D16A-P)

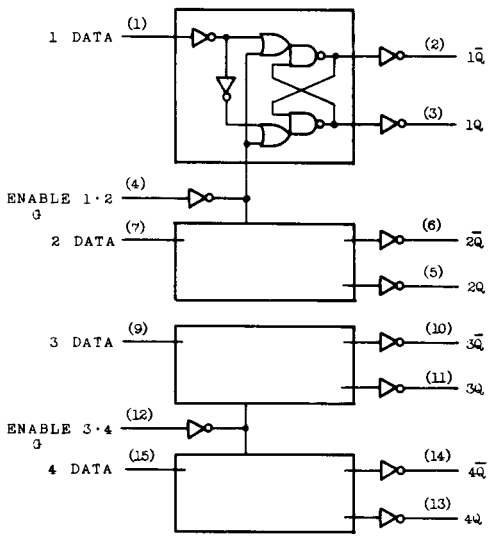



MFP16(F16GC-P)

## MAXIMUM RATINGS

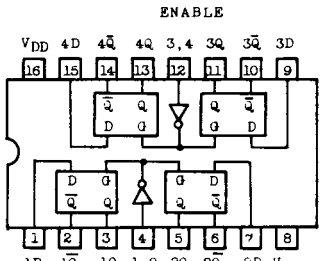
| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $V_{SS}$-0.5 ∿ $V_{SS}$+10 | V |
| Input Voltage | $V_{IN}$ | $V_{SS}$-0.5 ∿ $V_{DD}$+0.5 | V |
| Output Voltage | $V_{OUT}$ | $V_{SS}$-0.5 ∿ $V_{DD}$+0.5 | V |
| Input Current | $I_{IN}$ | ±10 | mA |
| Power Dissipation | $P_D$ | 300(DIP)/180(MFP) | mW |
| Storage Temperature | $T_{stg}$ | -65 ∿ 150 | °C |
| Lead Temp./Time | $T_{sol}$ | 260°C · 10 sec | |

## LOGIC DIAGRAN




※ ALL INPUTS ARE EQUIPPED WITH PROTECTION CIRCUIT.

## PIN CONNECTION




## TRUTH TABLE

| INPUT | | OUTPUT | |
|---|---|---|---|
| DATA | ENABLE | Q | Q̄ |
| L | H | L | H |
| H | H | H | L |
| X | L | No Change | |

X = Don't Care

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RECOMMENDED OPERATING CONDITIONS ($V_{SS}$=0.0V)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | - | 2.0 | - | 8.0 | V |
| Input Voltage | $V_{IN}$ | - | 0 | - | $V_{DD}$ | V |
| Operating Temperature | $T_{opr}$ | - | -40 | - | 85 | °C |

ELECTRICAL CHARACTERISTICS ($V_{SS}$=0.0V)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | $V_{DD}$ (V) | -40°C MIN. | -40°C MAX. | 25°C MIN. | 25°C TYP. | 25°C MAX. | 85°C MIN. | 85°C MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| High Level Output Voltage | $V_{OH}$ | $\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$ | 5 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | - | V |
| Low Level Output Voltage | $V_{OL}$ | $\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$ | 5 | - | 0.05 | - | 0.0 | 0.05 | | 0.05 | V |
| High Level Output Current | $I_{OH}$ | $V_{OH}$=4.6V $V_{IN}=V_{SS},V_{DD}$ | 5 | -0.52 | - | -0.44 | - | - | -0.36 | - | mA |
| Low Level Output Current | $I_{OL}$ | $V_{OL}$=0.4V $V_{IN}=V_{SS},V_{DD}$ | 5 | 1.4 | - | 1.1 | - | - | 0.8 | - | mA |
| Input Voltage "H" Level | $V_{IH}$ | $\|I_{OUT}\|$<1μA $V_{OUT}$=0.5V $V_{OUT}$=4.5V | 5 | 4.0 | - | 4.0 | - | - | 4.0 | - | V |
| Input Voltage "L" Level | $V_{IL}$ | | 5 | - | 1.0 | - | - | 1.0 | - | 1.0 | V |
| Input Current "H" Level | $I_{IH}$ | $V_{IH}$=8.0V | 8 | - | 0.3 | - | $10^{-5}$ | 0.3 | - | 1.0 | μA |
| Input Current "L" Level | $I_{IL}$ | $V_{IL}$=0.0V | 8 | - | -0.3 | - | $-10^{-5}$ | -0.3 | - | -1.0 | μA |
| Quiescent Supply Current | $I_{DD}$ | *$V_{IN}=V_{SS},V_{DD}$ | 5 | - | 12.5 | - | $10^{-3}$ | 12.5 | - | 75 | μA |

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, $V_{DD}$=5V, $C_L$=15pF)

| CHARACTERISTIC | | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Output Rise Time | | $t_{or}$ | | - | 18 | 35 | ns |
| Output Fall Time | | $t_{of}$ | | - | 15 | 30 | ns |
| Propagation Delay Time | Low-High Level | $t_{pLH}$ | DATA - Q, $\overline{Q}$ | - | 43 | 65 | ns |
| | High-Low Level | $t_{pHL}$ | | - | 35 | 53 | ns |
| Propagation Delay Time | Low-High Level | $t_{pLH}$ | ENABLE - Q, $\overline{Q}$ | - | 43 | 65 | ns |
| | High-Low Level | $t_{pHL}$ | | - | 35 | 53 | ns |
| Minimum Enable Pulse Width | | $t_w$ | | - | 40 | 60 | ns |
| Minimum Hold Time | | $t_{hold}$ | | - | - | 6 | ns |
| Minimum Set-up Time | | $t_{set-up}$ | | - | 25 | 44 | ns |
| Input Capacitance | | $C_{IN}$ | | - | 5 | | pF |

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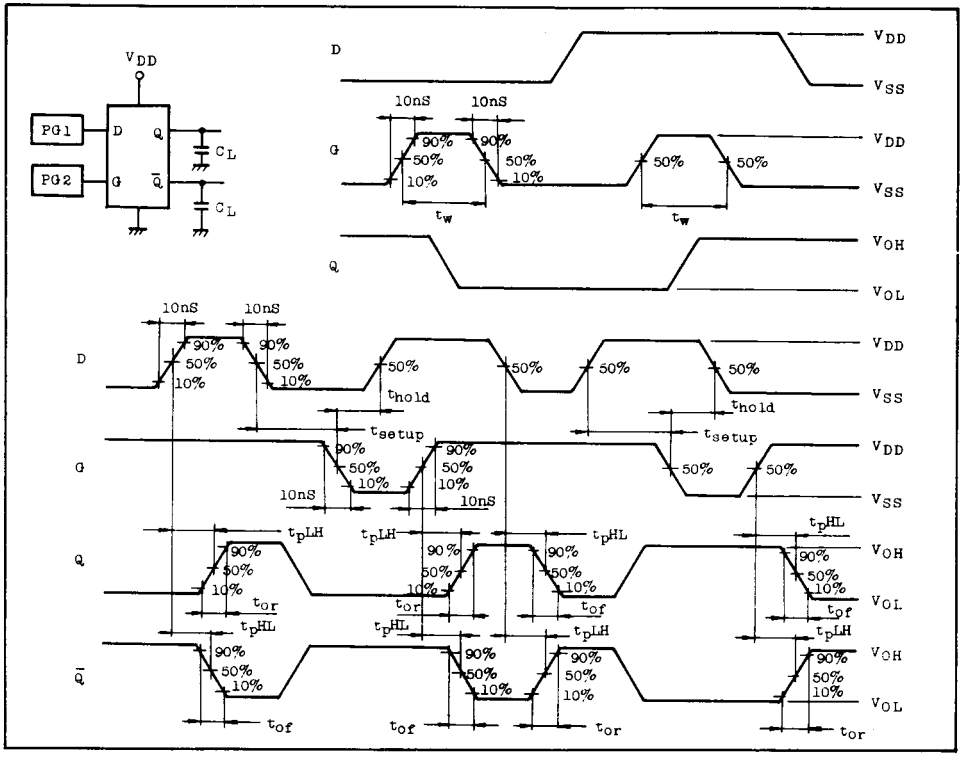
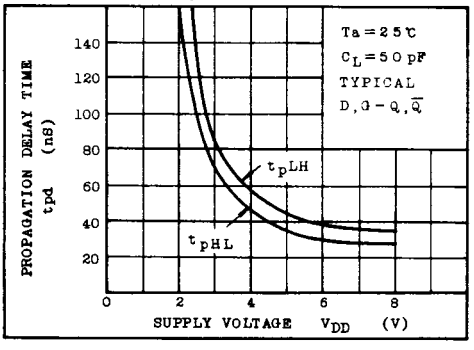
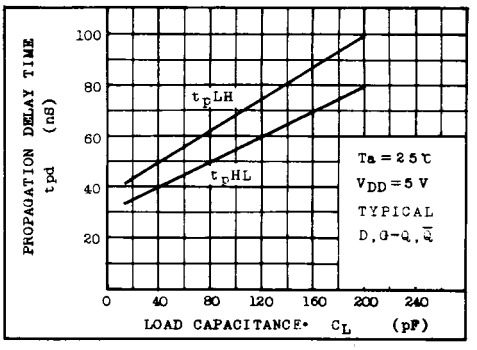
## SWITCHING TIME TEST CIRCUIT AND WAVEFORM

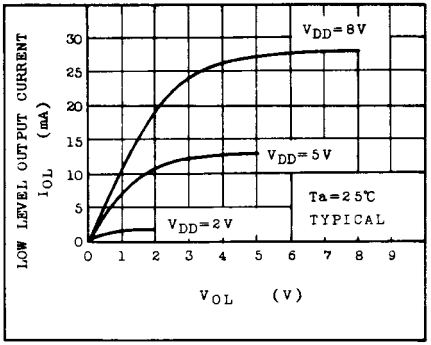


# TC40H375P/F

$I_{OL}$ - $V_{OL}$




$I_{OH}$ - ($V_{DD}$ - $V_{OH}$)