GS5586

Dual High-Efficiency PWM Step-Down DC-DC Converter

Product Description

The GS5586 is a dual high-efficiency Pulse-Width- Modulated (PWM) step-down DC-DC converter with an input voltage range of 2.7V to 5.5V and output voltage as low as 0.6V. It is optimized to react quickly to a load variation. The GS5586 incorporates a unique low noise architecture which reduces ripple and spectral noise.
The GS5586 is available in fixed voltage versions with internal feedback and a programmable version with external feedback resistors. It can deliver 1A of load cur- rent while maintaining a low 37μA no load quiescent current. The 2MHz switching frequency minimizes the size of external components while keeping switching losses low.
The GS5586 is designed to maintain high efficiency throughout the operating range, which is critical for por- table applications.
The GS5586 is available in the Pb-free, thermally enhanced 3x3mm DFN-12 package and is rated over the -40°C to +85°C temperature range.

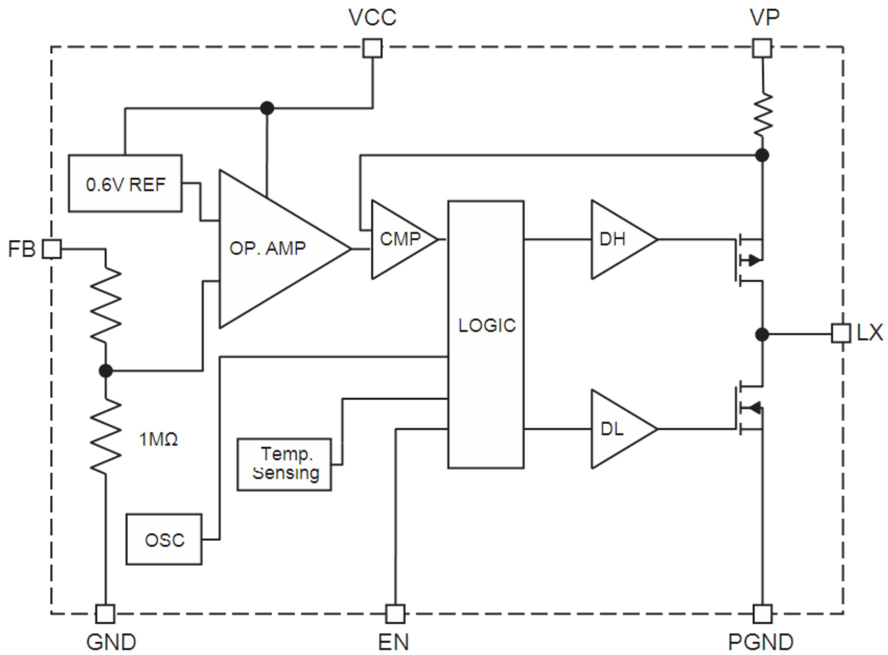
Features

- V_{IN} Range: 2.7V to 5.5V
- Low Noise Light Load Mode
- Low Ripple PWM Mode
- V_{OUT} Fixed or Adjustable from 0.6V to V_{IN}
- 37μA No Load Quiescent Current
- Up to 98% Efficiency
- 1A Max Output Current
- 2MHz Switching Frequency
- 150μs Soft Start
- Fast Load Transient
- Over-Temperature Protection
- Current Limit Protection
- 100% Duty Cycle Low-Dropout Operation
- <1μA Shutdown Current
- DFN3x3-12 Package

Applications

- Smart Phones and Cellular Phones
- PDAs and Handheld Computers
- Handheld Instruments
- Digital Still Cameras
- USB Devices
- Microprocessor / DSP Core / IO Power

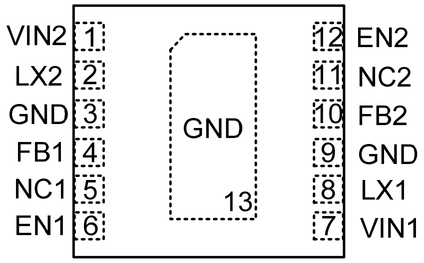
Block Diagram



GS5586

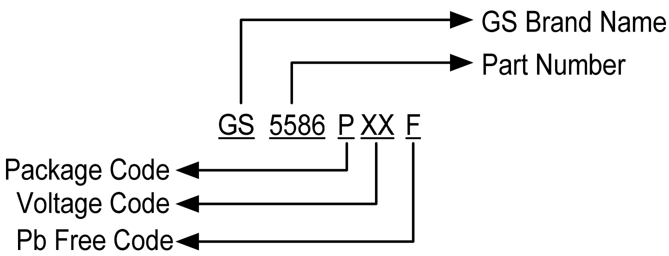
Packages & Pin Assignment

GS5586
DFN3x3-12(Top View)

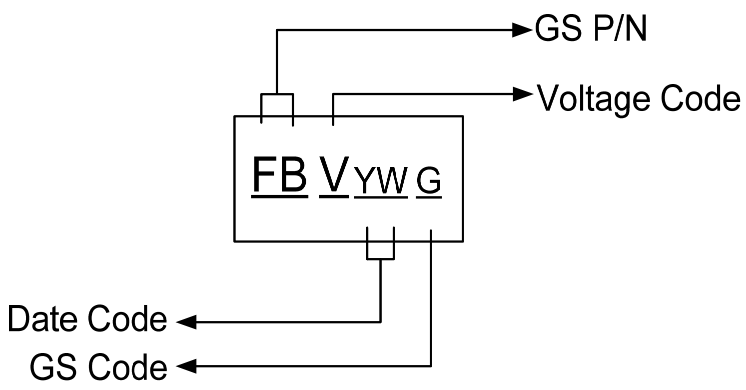


Pin	Symbol	Function
1	VIN2	Power Input of Channel 2.
2	LX2	Pin for Switching of Channel 2.
3, 9, Exposed Pad (13)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	FB1	Feedback of Channel 1.
5, 11	NC1, NC2	No Connection or Connect to V_{IN}.
6	EN1	Chip Enable of Channel 1 (Active High). $V_{EN1} \leqq V_{IN1}$.
7	VIN1	Power Input of Channel 1.
8	LX1	Pin for Switching of Channel 1.
10	FB2	Feedback of Channel 2.
12	EN2	Chip Enable of Channel 2 (Active High). $V_{EN2} \leqq V_{IN2}$.

Ordering Information



Marking Information



Part Number	Package	GS P/N	Voltage Code	Date Code
GS5586FAAF	DFN3*3-12	FB	A	YW
GS5586FRFF	DFN3*3-12	FB	F(3.3/1.8)	YW
GS5586FRDF	DFN3*3-12	FB	D(3.3/1.2)	YW
GS5586FRGF	DFN3*3-12	FB	G(3.3/1.5)	YW
GS5586FRHF	DFN3*3-12	FB	H(3.3/2.5)	YW

Absolute Maximum Rating

Symbol	Parameter	Value	Units
V_{IN}	Input Voltage GND	6.0	V
V_{LX}	LX to GND	-0.3 to V_{IN} + 0.3	V
V_{OUT}	OUT to GND	-0.3 to V_{IN} + 0.3	V
V_{EN}	EN to GND	-0.3 to V_{IN} + 0.3	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10	300	°C
P_D	Maximum Power Dissipation[2, 3]	2	W
θ_{JA}	Thermal Resistance[2]	50	°C/W

Electrical Characteristics

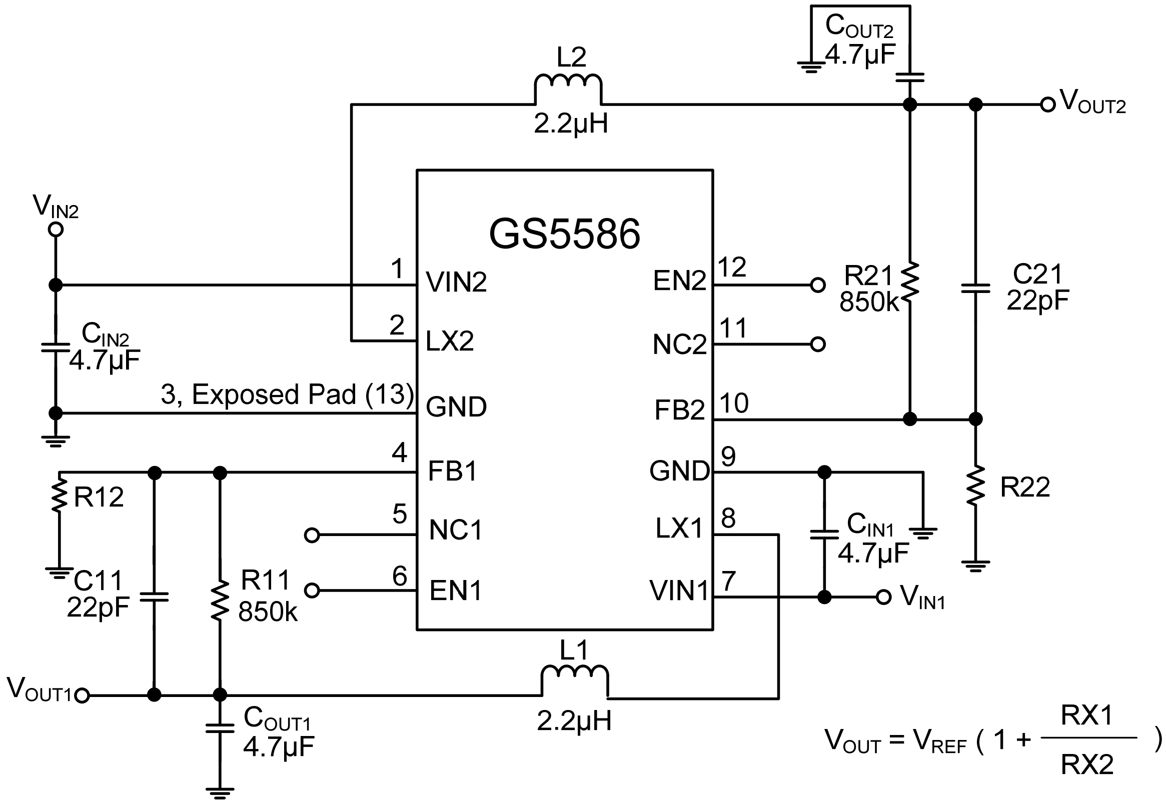
T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C, V_{IN} = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Step-Down Converter						
V_{IN}	Input Voltage		2.7		5.5	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising		1.8	2.7	V
		Hysteresis		100		mV
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0mA to 1A, V_{IN} = 2.7V to 5.5V	-3.0		+3.0	%
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
I_Q	Quiescent Current	No Load, 0.6V Adjustable Version		40	70	µA
I_{SHDN}	Shutdown Current	EN = AGND = PGND			1.0	µA
I_{LIM}	P-Channel Current Limit		1300	1700		mA
$R_{DS(ON)H}$	High Side Switch On Resistance			0.35		Ω
$R_{DS(ON)L}$	Low Side Switch On Resistance			0.30		Ω
$\Delta V_{Linereg}$	Line Regulation	V_{IN} = 2.7V to 5.5V; I_{OUT} = 1A		0.1		%/V
V_{FB}	Feedback Threshold Voltage Accuracy	0.6V Output, No Load; T_A = 25°C	591	600	609	mV
I_{FB}	Feedback Leakage Current	0.6V Output			1	µA
T_S	Start-Up Time	From Enable to Output Regulation		150		µs
F_{OSC}	Oscillator Frequency	T_A = 25°C	0.9	2.0	2.6	MHz
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
EN						
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
I_{EN}	Input Low Current	V_{IN} = V_{OUT} = 5.5V	-1.0		1.0	µA

Note 1: Production test at +25ºC. Specifications over the temperature range are guaranteed by design and characterization.

Note 2: Level and body temperature defined by IPC/JEDEC J-STD-020

Diagram



$$V_{OUT} = V_{REF}\left(1 + \frac{RX1}{RX2}\right)$$

Figure1. GS5586 Adjustable Output Voltage

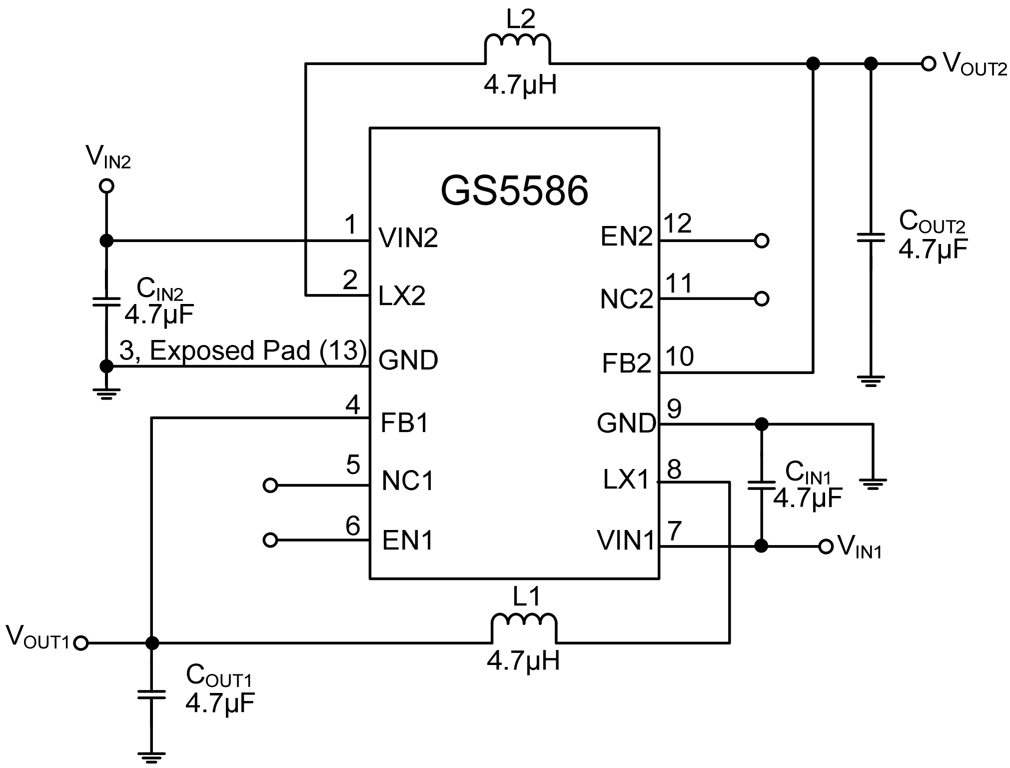
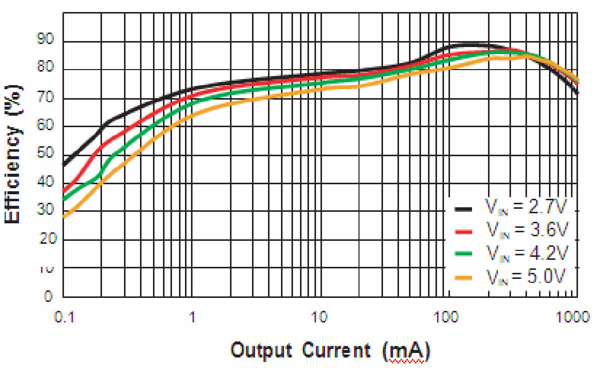


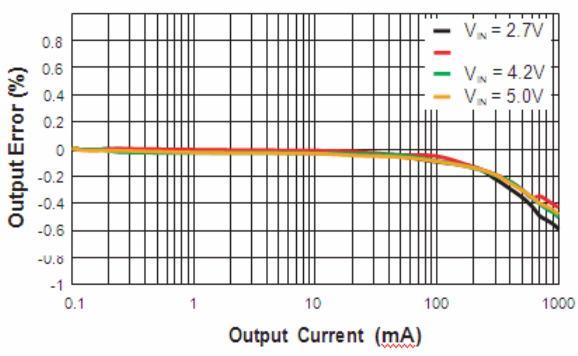
Figure2. GS5586 Fixed Output Voltage

Typical Performance Characteristics

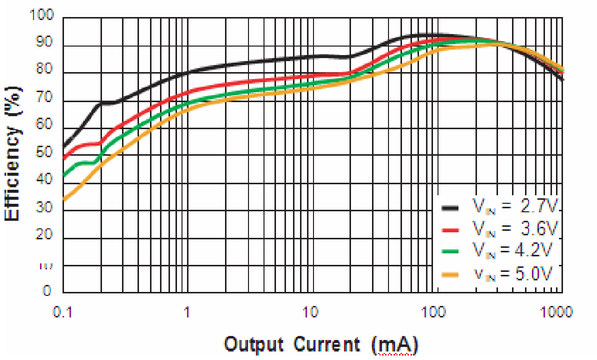
Efficiency vs. Output Current
(V_{OUT} = 1.2V; L = 2.2µH; C_{OUT} = 10µF)



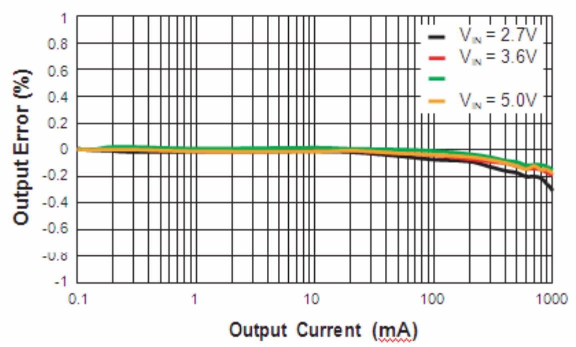
Load Regulation
(V_{OUT} = 1.2V; L = 2.2µH; C_{OUT} = 10µF)



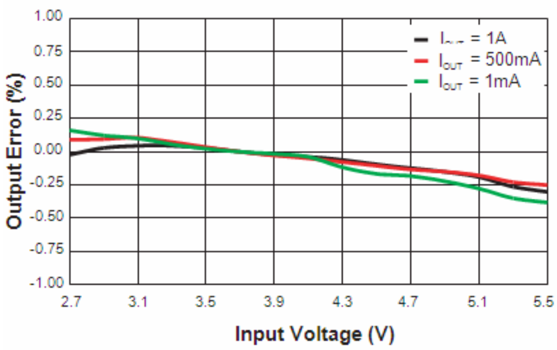
Efficiency vs. Output Current
(V_{OUT} = 1.8V; L = 4.7µH; C_{OUT} = 4.7µF)



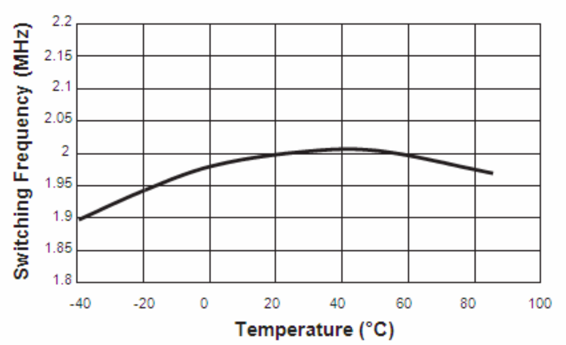
Load Regulation
(V_{OUT} = 1.8V; L = 4.7µH; C_{OUT} = 4.7µF)



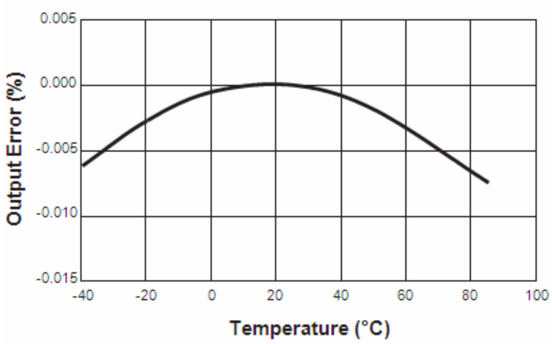
Line Regulation
(V_{OUT} = 1.8V; C_{OUT} = 10µF; C_{FF} = 100pF)



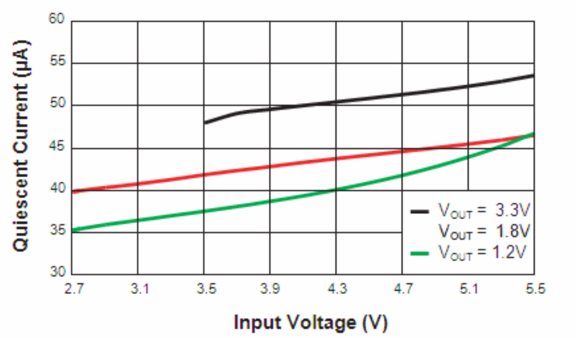
Switching Frequency vs. Temperature



Output Error vs. Temperature
(I_{OUT} = 500mA)



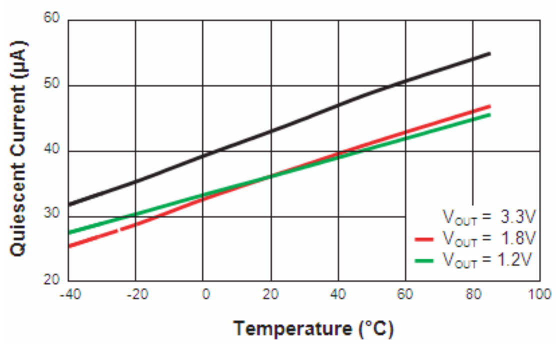
Quiescent Current vs. Input Voltage



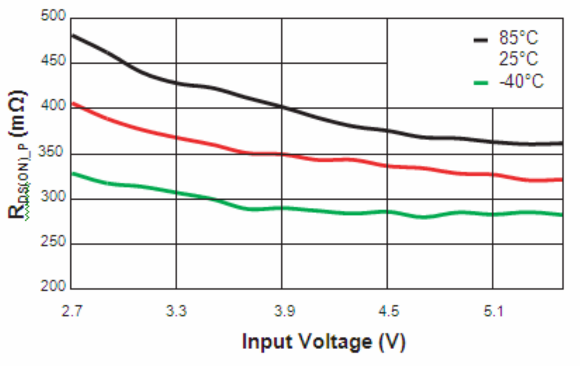
Typical Performance Characteristics(Continue)

Qulescent Current vs. Temperature

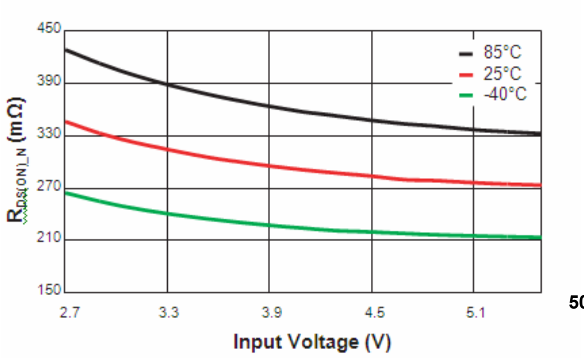
(V_{IN} = 3.6V)



P-ChannelRDS(ON) vs. Input Voltage

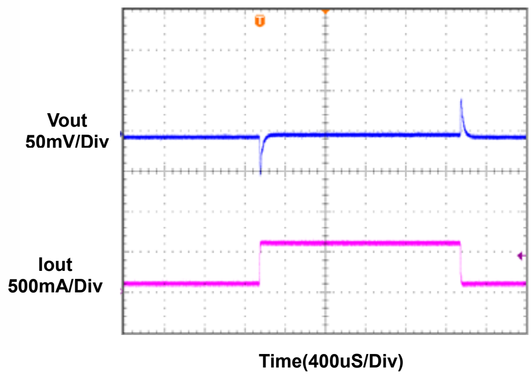


N-ChannelRDS(ON) vs. Input Voltage



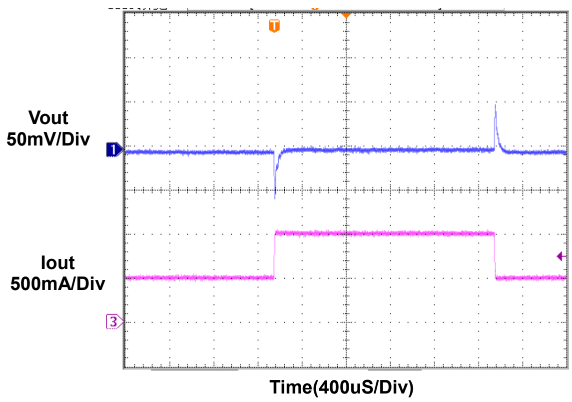
Load Transient Respone

Vin=3.6V Vout=1.8V C1=100pF Cout=10uF



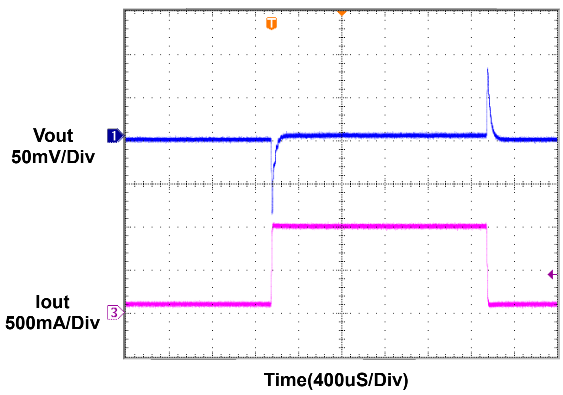
Load Transient Response

Vin=3.6V Vout=1.8V C1=100pF Cout=10uF



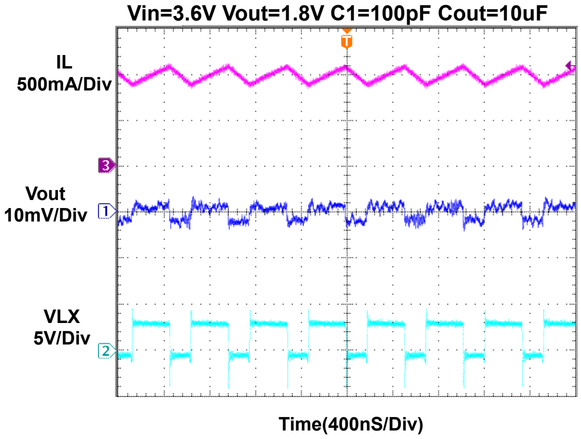
Load Transient Response

Vin=3.6V Vout=1.8V C1=100pF Cout=10uF



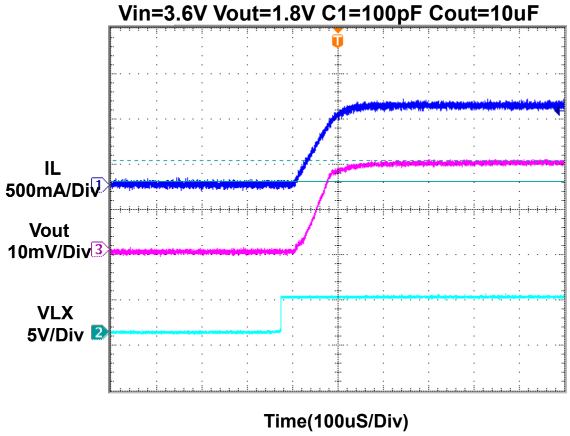
Output Ripple

Vin=3.6V Vout=1.8V C1=100pF Cout=10uF



Power On

Vin=3.6V Vout=1.8V C1=100pF Cout=10uF



Functional Description

The GS5586 is a high performance 1A 2MHz monolithic step-down converter. It has been designed with the goal of minimizing external component size and optimizing efficiency over the complete load range, and produces reduced ripple and spectral noise. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. Typically, a 4.7μH inductor and a 4.7μF ceramic capacitor are recommended (see table of values).

The fixed output version requires only three external power components (CIN, COUT, and L). The adjustable version can be programmed with external feedback to any voltage, ranging from 0.6V to the input voltage. An additional feed-forward capacitor can also be added to the external feedback to provide improved transient response (see Figure 1).

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the RDSON drop of the P-channel high-side MOSFET.

The input voltage range is 2.7V to 5.5V. The converter efficiency has been optimized for all load conditions, ranging from no load to 1A.

The internal error amplifier and compensation provides excellent transient response, load, and line regulation. Soft start eliminates any output voltage overshoot and input inrush current when the enable or the input voltage is applied.

Control Loop

The GS5586 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak cur- rent mode loop appears as a voltage-programmed cur- rent source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. For fixed voltage versions, the error amplifier reference volt- age is internally set to program the converter output voltage. For the adjustable output, the error amplifier reference is fixed at 0.6V.

Soft Start / Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the GS5586 into a low-power, non-switching state. The total input current during shut- down is less than 1μA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limit- ed. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VIN input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low-voltage fixed versions of the GS5586 is 0.24A/μs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.5V output and 4.7μH inductor.

$$m = \frac{0.75 \cdot Vo}{L} = \frac{0.75 \cdot 1.5V}{4.7\mu H} = 0.24\ A/\mu s$$

This is the internal slope compensation for the adjust- able (0.6V) version or low-voltage fixed versions. When externally programming the 0.6V version to 2.5V, the calculated inductance is 7.5μH.

$$L = \frac{0.75 \cdot Vo}{m} = \frac{0.75 \cdot Vo}{0.24A/\mu s} \approx 3\frac{\mu s}{A} \cdot Vo = 3\frac{\mu s}{A} \cdot 2.5V = 7.5\mu H$$

In this case, a standard 6.8μH value is selected.
For high-voltage fixed versions (≥2.5V), m = 0.48A/μs. Table 1 displays inductor values for the GS5586 fixed and adjustable options.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 4.7μH SD3118 series inductor selected from Coilcraft has a 162mΩ typical DCR and a 1.31A saturation cur- rent. At full load, the inductor DC loss is 162mW which gives a 9% loss in efficiency for a 1A, 1.8V output.

Input Capacitor

Select a 4.7μF to 10μF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (VPP) and solve for C. The calculated value varies with input volt- age and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{Vpp}{Io} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} = \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{Vpp}{Io} - ESR\right) \cdot 4F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10μF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6μF.

Output Voltage (V)	Inductor (μH)	Output Capacitor (μF)
1, 1.2	2.2	10
1.5, 1.8	4.7	4.7
2.5, 3.3	6.8	4.7

Table 1: Inductor and Output Capacitor Values.

The maximum input capacitor RMS current is:

$$I_{RMS} = Io \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term Vo/Vin • (1-Vo/Vin). appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the GS5586. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage dur- ing load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and pro- vides holdup during large load transitions. A 4.7μF to 10μF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7μF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

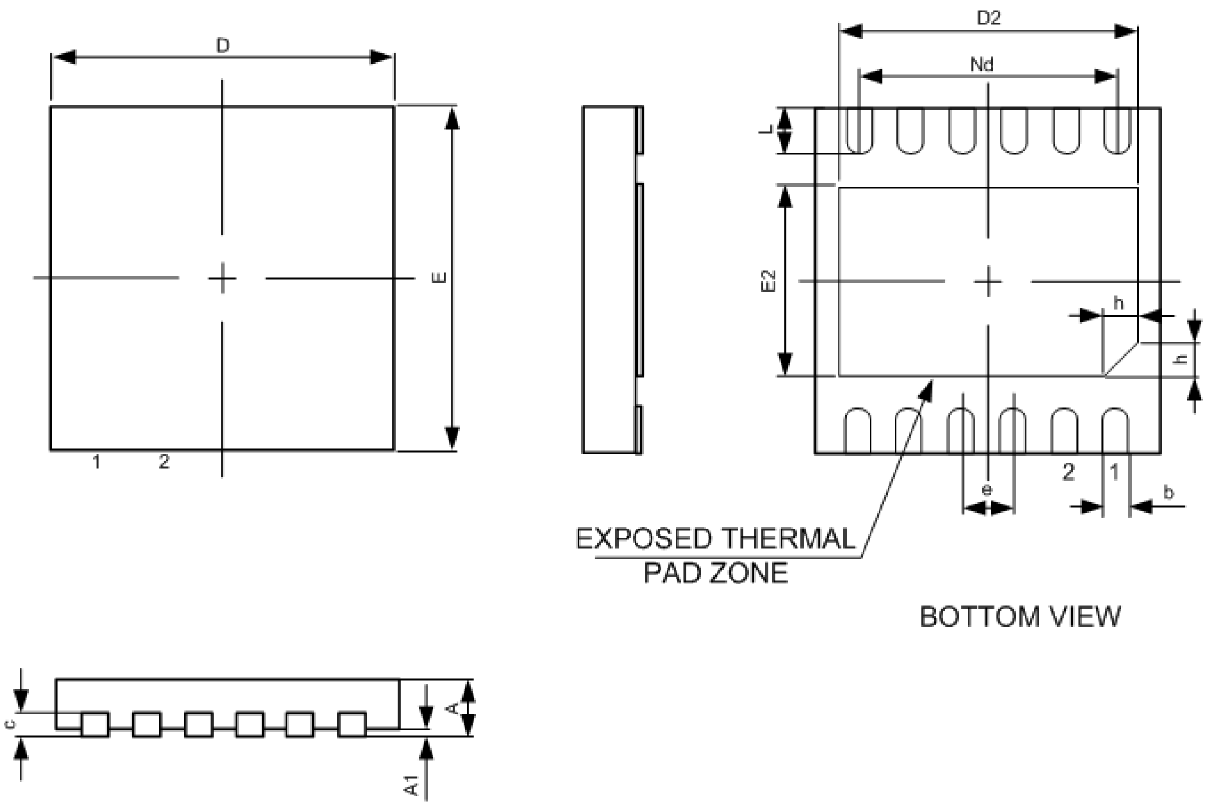
The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2\sqrt{3}} \cdot \frac{V_{OUT}\,(V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Package Dimension

DFN3x3-12



Dimension			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	--	0.02	0.05
b	0.16	0.23	0.28
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
e	0.45 BSC		
Nd	2.25 BSC		
E	2.90	3.00	3.10
E2	1.50	1.55	1.60
L	0.30	0.40	0.50
h	0.20	0.25	0.30

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