QUALITY SEMICONDUCTOR, INC.

QuickSwitch® Products 3.3V Quad 2:1 Mux/Demux for Hot Swap Applications (HotSwitch™)

FEATURES/BENEFITS

- N channel FET switches with no parasitic diode to V_{CC}
  – No DC path to V_{CC} or GND
  – 5V tolerant in OFF sate
- Bidirectional dataflow with near-zero delay
  – No added ground bounce
- Low R_{ON} - 4Ω typical
- Flat R_{ON} characteristics over operating range
- Excellent R_{ON} matching between channels
- Low capacitance
- LVTTL-compatible control inputs
- Undershoot clamp diodes on all control and switch inputs
- Available in QSOP, SOIC (S1) and TSSOP packages

DESCRIPTION

The QS3VH257 HotSwitch Quad 2:1 mulitplexer/ demultiplexer is specially designed for hot-swapping and multiplexing in a 3.3V supply environment. The QS3VH257 has very low ON resistance resulting in under 200ps propagation delay through the switch. In the OFF state, the switches are 5V-tolerant and offer very high impedance at the terminals.

The combination of near-zero propagation delay, high OFF impedance, and over-voltage tolerance makes QS3VH257 ideal for hot swapping applications. The low ON resistance of QS3VH257 makes it ideal for PCI and Compact PCI hot swapping environment.

Figure 1. Functional Block Diagram

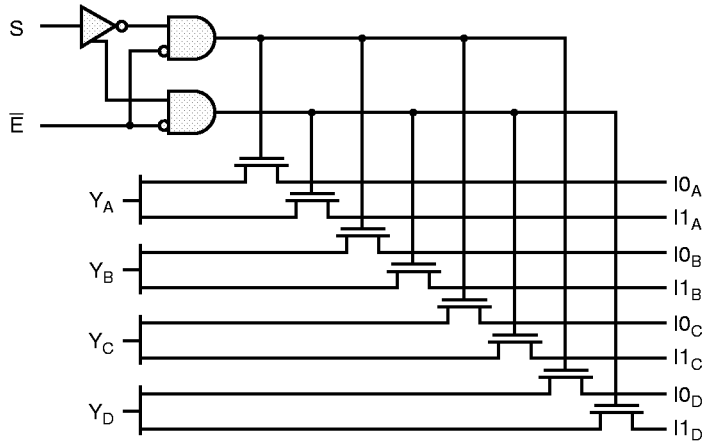

Table 1. Pin Description

Name	I/O	Description
1xx	I	Data Inputs
S	I	Select Input
$\overline{E}$	I	Enable Input
Y_A-Y_D	O	Data Outputs

Figure 2. Pin Configuration

(All Pins Top View)

QSOP, SOIC (S1), TSSOP

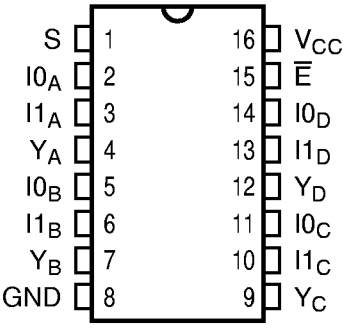

Table 2. Function Table

Inputs		Outputs				
$\overline{E}$	S	Y_A	Y_B	Y_C	Y_D	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	$I0_A$	$I0_B$	$I0_C$	$I0_D$	Select 0
L	H	$I1_A$	$I1_B$	$I1_C$	$I1_D$	Select 1

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 4.6V
DC Switch Voltage V_S	–0.5V to 5.5V
DC Input Voltage V_{IN}	–0.5V to 5.5V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4.Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins		SOIC, QSOP		Unit
		Typ	Max	
Control Inputs		3	5	pF
QuickSwitch Channels (Switch OFF)	Demux	4	6	pF
	Mux	7	9	pF

Note: Capacitance is guaranteed, but not production tested and are typical values. For total capacitance while the switch is ON, please see Section 1 under "Input and Switch Capacitance."

Table 5. DC Electrical Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$\| I_{IN} \|$	Input Leakage Current (Control Inputs)	$0V \le V_{IN} \le V_{CC}$	—	—	1	µA
$\| I_{OZ} \|$	Off-State Current (Hi-Z)	$0V \le V_{OUT} \le V_{CC}$, Switches OFF	—	—	1	µA
R_{ON}	Switch On Resistance(2,3)	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 30mA	—	4	6	Ω
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15mA	—	5	8	

Notes:
1. Typical values indicate V_{CC} = 3.3V and T_A = 25°C.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section 1 under "DC Electrical Characteristics."
3. R_{ON} guaranteed, but not production tested.

Figure 3. Typical ON Resistance vs V_{IN} at V_{CC} = 3.3V

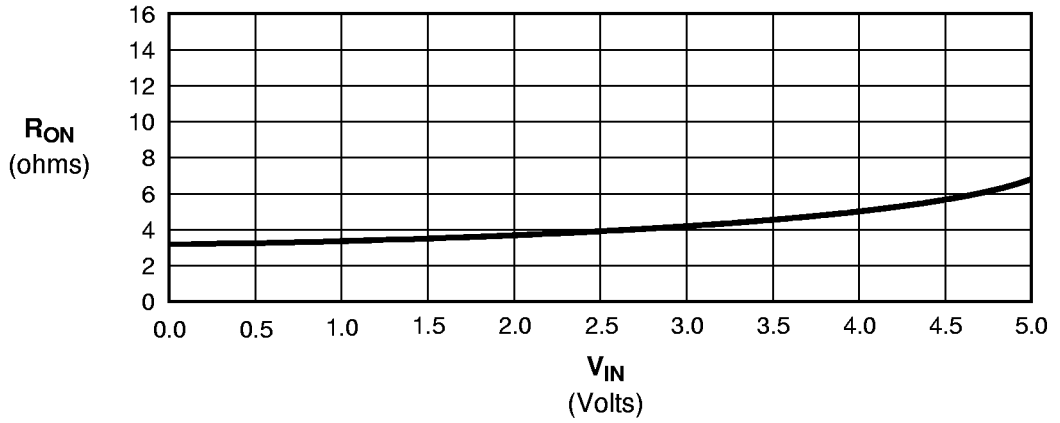

Table 6. Power Supply Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	3.0	mA
ΔI_{CC}	Power Supply Current[2,3] per Input HIGH	V_{CC} = Max., V_{IN} = 3.0V, f = 0 per Control Input	30	µA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A and Y Pins Open, per Control Inputs Toggling @ 50% Duty Cycle	0.25 MHz	mA/

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per LVTTL driven input. A and Y pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and Y inputs generate no significant AC or DC currents as they change states. This parameter is guaranteed, but not production tested.

Table 7. Switching Characteristics Over Operating Range

Commercial T_A = –40°C to 85°C, V_{CC} = 3.3V ±0.3V
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	Min[4]	Typ	Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] A to Y	—	—	0.25	ns
t_{PZH} t_{PZL}	Switch Turn-on Delay Sn, $\overline{En}$ to Y	1.5	—	9.0	ns
t_{PHZ} t_{PLZ}	Switch Turn-off Delay[2] Sn, $\overline{En}$ to Y	1.5	—	8.0	ns
f_S	Operating Frequency - Data[2, 5] $\overline{OE}$ = LOW	—	—	150	MHz
$f_{CONTROL}$	Operating Frequency - Enable, Select[2, 6]	—	—	1	MHz

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not production tested.
2. This parameter is guaranteed, but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.20ns for C_L = 50pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Minimums guaranteed, but not production tested.
5. Maximum frequency for bidirectional data flow.
6. Maximum toggle frequency for $\overline{E}$ and S control input.