Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HARRIS SEMICONDUCTOR

CD74HC151, CD74HCT151

High Speed CMOS Logic 8-Input Multiplexer

September 1997

Features

- Complementary Data Outputs
- Buffered inputs and Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The Harris CD74HC151 and CD74HCT151 are single 8-channel digital multiplexers having three binary control inputs, S0, S1 and S2 and an active low enable (E) input. The three binary signals select 1 of 8 channels. Outputs are both inverting ($\overline{Y}$) and non-inverting (Y).

Ordering Information

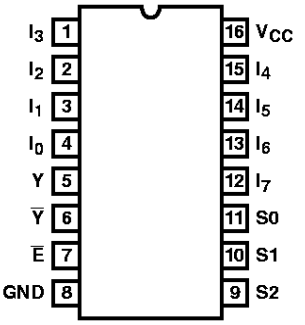
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC151E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT151E	-55 to 125	16 Ld PDIP	E16.3
CD74HC151M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT151M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

CD74HC151, CD74HCT151
(PDIP, SOIC)
TOP VIEW



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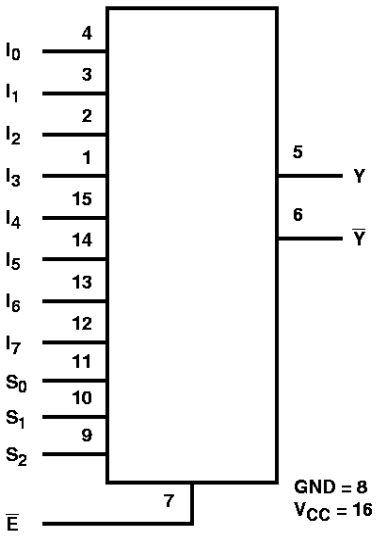
Functional Diagram



TRUTH TABLE

SELECT INPUTS			DATA INPUTS								ENABLE	OUTPUT	
S2	S1	S0	I0	$\overline{I1}$	I2	I3	I4	I5	I6	I7	$\overline{E}$	$\overline{Y}$	Y
X	X	X	X	X	X	X	X	X	X	X	H	H	L
L	L	L	L	X	X	X	X	X	X	X	L	H	L
L	L	L	H	X	X	X	X	X	X	X	L	L	H
L	L	H	X	L	X	X	X	X	X	X	L	H	L
L	L	H	X	H	X	X	X	X	X	X	L	L	H
L	H	L	X	X	L	X	X	X	X	X	L	H	L
L	H	L	X	X	H	X	X	X	X	X	L	L	H
L	H	H	X	X	X	L	X	X	X	X	L	H	L
L	H	H	X	X	X	H	X	X	X	X	L	L	H
H	L	L	X	X	X	X	L	X	X	X	L	H	L
H	L	L	X	X	X	X	H	X	X	X	L	L	H
H	L	H	X	X	X	X	X	L	X	X	L	H	L
H	L	H	X	X	X	X	X	H	X	X	L	L	H
H	H	L	X	X	X	X	X	X	L	X	L	H	L
H	H	L	X	X	X	X	X	X	H	X	L	L	H
H	H	H	X	X	X	X	X	X	X	L	L	H	L
H	H	H	X	X	X	X	X	X	X	H	L	L	H

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 115
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
Select	1.5
Data	0.45
Enable	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay (Figure 1) Any Data Input to Y	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	170	-	215	-	255	ns
			4.5	-	-	34	-	43	-	51	ns
		C_L =15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	29	-	37	-	43	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Any Data Input to $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C_L =15pF	5	-	15	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	31	-	39	-	48	ns
Any Select to Y	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C_L =15pF	5	-	15	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	31	-	39	-	48	ns
Any Select to $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	205	-	255	-	310	ns
			4.5	-	-	41	-	51	-	62	ns
		C_L =15pF	5	-	17	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	35	-	43	-	53	ns
Enable to Y	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	140	-	175	-	210	ns
			4.5	-	-	28	-	35	-	42	ns
		C_L =15pF	5	-	11	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	24	-	30	-	36	ns
Enable to $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	145	-	180	-	220	ns
			4.5	-	-	29	-	36	-	44	ns
		C_L =15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	25	-	31	-	38	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	59	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay (Figure 2) Any Data Input to Y	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	38	-	48	-	57	ns
		C_L =15pF	5	-	16	-	-		-	-	ns
Any Data Input to $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	36	-	45	-	54	ns
		C_L =15pF	5	-	15	-	-	-	-	-	ns
Any Select to Y	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-		41	-	51	-	62	ns
		C_L =15pF	5	-	17	-	-	-	-	-	ns
Any Select to $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C_L =15pF	5	-	18	-	-	-	-	-	ns
Enable to Y	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	29	-	36	-	44	ns
		C_L =15pF	5	-	12	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Enable to $\overline{Y}$	C_L = 50pF	C_L = 50pF	4.5	-	-	36	-	46	-	54	ns
	C_L =15pF	C_L =15pF	5	15	-	-	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5		58	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per gate.
5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuit and Waveform

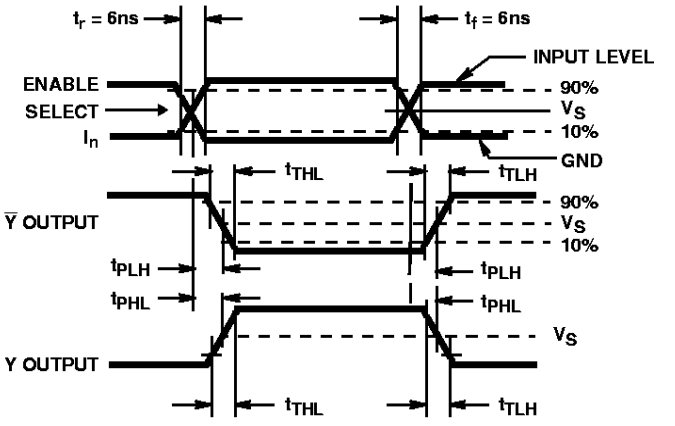


FIGURE 1.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Sales Office Headquarters

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