Document Title

8M X 8 Bit / 4M X 16 Bit CMOS 3.0 Volt-only, Boot Sector Flash Memory

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	October 16, 2008	Preliminary
1.0	Final version release	May 12, 2009	Final
1.1	Page 1: Change from typical 100,000 cycles to minimum 100,000 cycles	December 1, 2010	

A29L640 Series

8M X 8 Bit / 4M X 16 Bit CMOS 3.0 Volt-only, Boot Sector Flash Memory

Features

- Single power supply operation
  - Regulated voltage range: 2.7 to 3.6 volt read and write operations for compatibility with high performance 3 volt microprocessors
- Access times:
  - 70ns (max.)
- Current:
  - 2mA active read current at 1MHz
  - 10mA active read current at 5MHz
  - 20mA typical program/erase current
  - 1μA typical CMOS standby or Automatic Sleep Mode current
- Flexible sector architecture
  - 8KB x 8 sectors
  - 64KB x 127 sectors
  - Any combination of sectors can be erased
  - Supports full chip erase
  - Sector protection:
- Extra 128-word sector for security
- Unlock Bypass Program Command
  - Reduces overall programming time when issuing multiple program command sequence
- Top or bottom boot block available
- Embedded Algorithms
  - Embedded Erase algorithm will automatically erase the entire chip or any combination of designated sectors and verify the erased sectors
- Embedded Program algorithm automatically writes and verifies data at specified addresses
- Minimum 100,000 program/erase cycles per sector
- 20-year data retention at 125°C
  - Reliable operation for the life of the system
- CFI (Common Flash Interface) compliant
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Compatible with JEDEC-standards
  - Pinout and software compatible with single-power-supply Flash memory standard
  - Superior inadvertent write protection
- $\overline{\text{Data}}$ Polling and toggle bits
  - Provides a software method of detecting completion of program or erase operations
- Ready / $\overline{\text{BUSY}}$ pin (RY / $\overline{\text{BY}}$)
  - Provides a hardware method of detecting completion of program or erase operations (not available on 44-pin SOP)
- Erase Suspend/Erase Resume
  - Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation
- Hardware reset pin ($\overline{\text{RESET}}$)
  - Hardware method to reset the device to reading array data
- $\overline{\text{WP}}$ /ACC input pin
  - Write protect ($\overline{\text{WP}}$) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function provides accelerated program times
- Hardware/Software temporary sector block unprotect command allows code changes in previously locked sectors
- Hardware/Software sector protect/unprotect command
- Package options
  - 44-pin SOP or 48-pin TSOP (I) or 48-ball TFBGA
  - All Pb-free (Lead-free) products are RoHS compliant

General Description

The A29L640 is a 64Mbit, 3.3 volt-only Flash memory organized as 4,194,304 words of 16 bits or 8,388,608 bytes of 8 bits each. The 8 bits of data appear on I/O_0 - I/O_7; the 16 bits of data appear on I/O_0~I/O_{15}. The A29L640 is offered in 44-Pin SOP, 48-Pin TSOP and 48-ball TFBGA packages. This device is designed to be programmed in-system with the standard system 3.3 volt VCC supply. Additional 12.0 volt VPP is not required for in-system write or erase operations. However, the A29L640 can also be programmed in standard EPROM programmers.

The A29L640 has the first toggle bit, I/O_6, which indicates whether an Embedded Program or Erase is in progress, or it is in the Erase Suspend. Besides the I/O_6 toggle bit, the A29L640 has a second toggle bit, I/O_2, to indicate whether the addressed sector is being selected for erase. The A29L640 also offers the ability to program in the Erase Suspend mode. The standard A29L640 offers access times of 70ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$) and output enable ($\overline{\text{OE}}$) controls.

The device requires only a single 3.3 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The A29L640 is entirely software command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the

erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by writing the proper program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper program margin.

Device erasure occurs by executing the proper erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper erase margin. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

The host system can detect whether a program or erase operation is complete by observing the RY / $\overline{BY}$ pin, or by reading the I/O7 ($\overline{Data}$ Polling) and I/O6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The A29L640 is fully erased when shipped from the factory.

The hardware sector protection feature disables operations for both program and erase in any combination of the sectors of memory. This can be achieved via programming equipment.

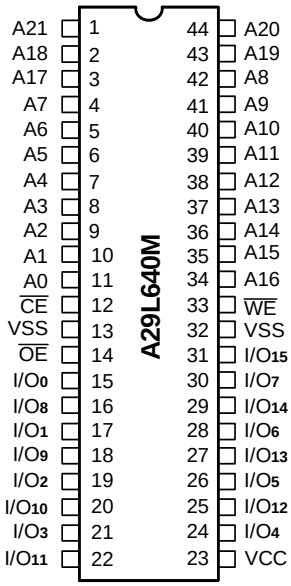
The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any other sector that is not selected for erasure. True background erase can thus be achieved.

The hardware $\overline{RESET}$ pin terminates any operation in progress and resets the internal state machine to reading array data. The $\overline{RESET}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

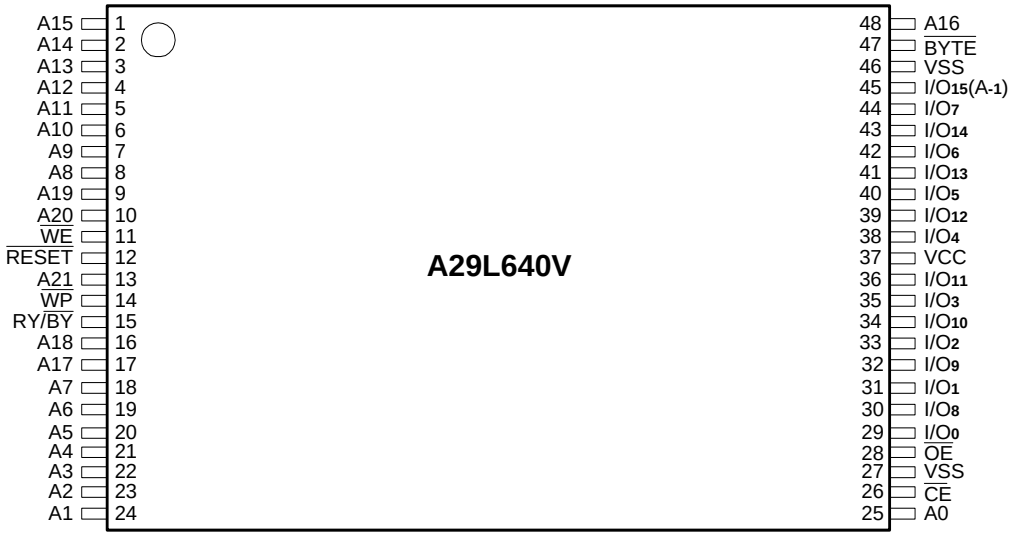
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

Pin Configurations

■ SOP



■ TSOP (I)



Pin Configurations (continued)

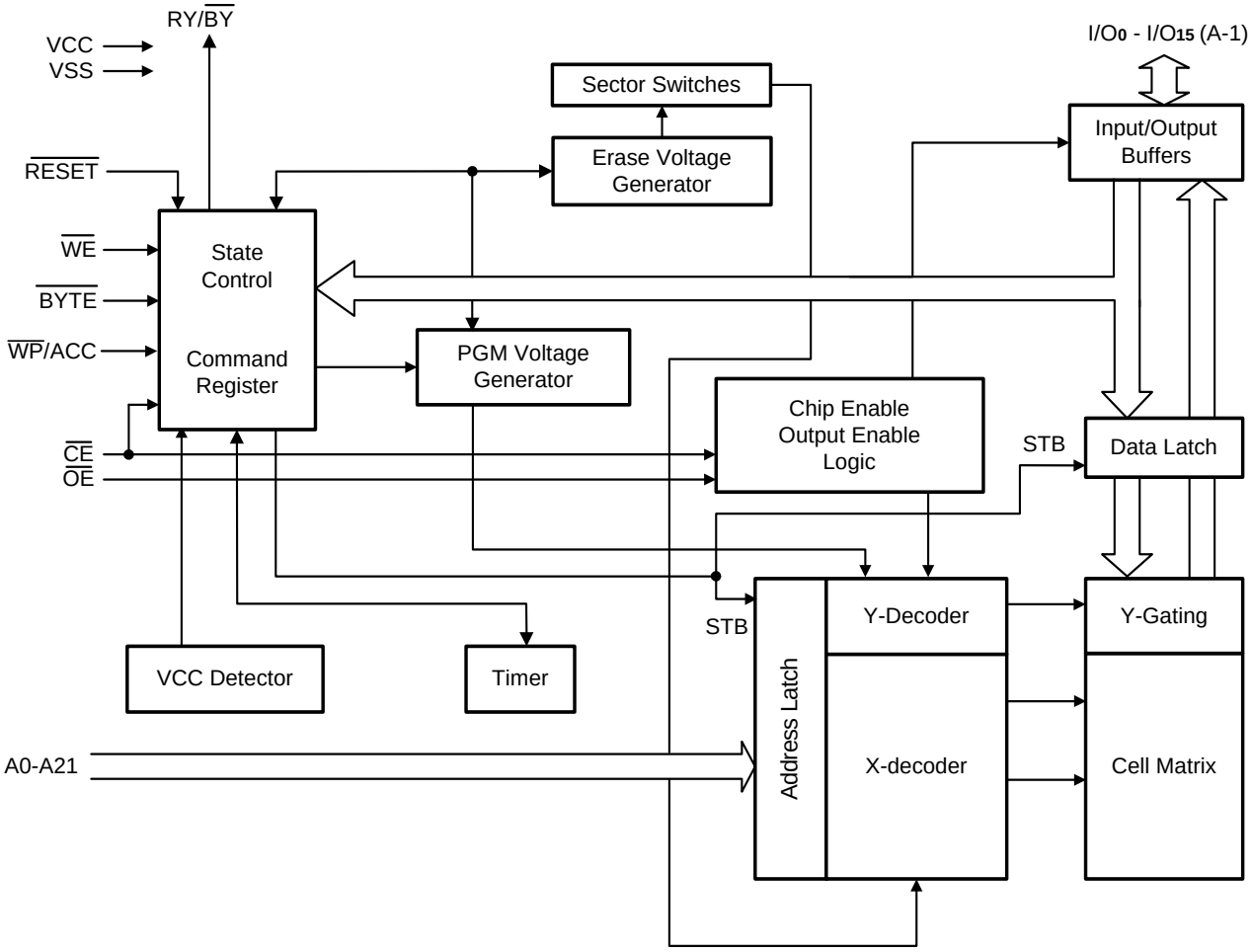
■ **TFBGA**

TFBGA
Top View, Balls Facing Down

A6 A13	B6 A12	C6 A14	D6 A15	E6 A16	F6 $\overline{BYTE}$	**G6** I/O_{15}(A-1)	H6 VSS
A5 A9	B5 A8	C5 A10	D5 A11	E5 I/O_7	F5 I/O_{14}	**G5** I/O_{13}	H5 I/O_6
A4 $\overline{WE}$	B4 $\overline{RESET}$	C4 A21	D4 A19	E4 I/O_5	F4 I/O_{12}	**G4** VCC	H4 I/O_4
A3 RY/$\overline{BY}$	B3 $\overline{WP}$/ACC	C3 A18	D3 A20	E3 I/O_2	F3 I/O_{10}	**G3** I/O_{11}	H3 I/O_3
A2 A7	B2 A17	C2 A6	D2 A5	E2 I/O_0	F2 I/O_8	**G2** I/O_9	H2 I/O_1
A1 A3	B1 A4	C1 A2	D1 A1	E1 A0	F1 $\overline{CE}$	**G1** $\overline{OE}$	H1 VSS

●

Block Diagram



Pin Descriptions

Pin No.		Description
A0 – A21		Address Inputs
I/O0 - I/O14		Data Inputs/Outputs
I/O15 (A-1)	I/O15	Data Input/Output, Word Mode
	A-1	LSB Address Input, Byte Mode
$\overline{CE}$		Chip Enable
$\overline{WE}$		Write Enable
$\overline{OE}$		Output Enable
$\overline{RESET}$		Hardware Reset
$\overline{BYTE}$		Selects Byte Mode or Word Mode
RY/$\overline{BY}$		Ready/$\overline{BUSY}$ - Output
VSS		Ground
VCC		Power Supply
NC		Pin not connected internally
$\overline{WP}$ /ACC		Hardware Write Protect / Acceleration Pin

Absolute Maximum Ratings*

Storage Temperature Plastic Packages. . . -65°C to + 150°C
Ambient Temperature with Power Applied. -55°C to + 125°C
Voltage with Respect to Ground
VCC (Note 1) . . . . . -0.5V to +4.0V
A9, $\overline{OE}$ & $\overline{RESET}$ (Note 2) . . . . . -0.5V to +10.5V
$\overline{WP}$ /ACC . . . . . -0.5V to +10.5V
All other pins (Note 1) . . . . . -0.5V to VCC + 0.5V
Output Short Circuit Current (Note 3) 200mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is VCC +0.5V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0V for periods up to 20ns.
2. Minimum DC input voltage on A9, $\overline{OE}$ and $\overline{RESET}$ is -0.5V. During voltage transitions, A9, $\overline{OE}$ and $\overline{RESET}$ may overshoot VSS to -2.0V for periods of up to 20ns. Maximum DC input voltage on A9 is +10.5V which may overshoot to 14.0V for periods up to 20ns.
3. No more than one output is shorted at a time. Duration of the short circuit should not be greater than one second.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Extended Range Devices

Ambient Temperature (T_A)
For –U series . . . . . -40°C to +85°C
For –I series . . . . . -25°C to +85°C

VCC Supply Voltages

VCC for all devices . . . . . +2.7V to +3.6V
Operating ranges define those limits between which the functionally of the device is guaranteed.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. A29L640 Device Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{WP}$ / ACC	A0 - A21 (Note 1)	I/O_0 - I/O_7	I/O_8 - I/O_{15}	
								$\overline{BYTE}$ =V_{IH}	$\overline{BYTE}$ =V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	I/O_8~I/O_{14}=High-Z I/O_{15}=A-1
Write	L	H	L	H	(Note 3)	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 4)	(Note 4)	High-Z
Standby	VCC ± 0.3 V	X	X	VCC ± 0.3 V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	Sector Address, A6=L, A1=H, A0=L	(Note 4)	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	L/H	Sector Address, A6=H, A1=H, A0=L	(Note 4)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	L/H	A_{IN}	(Note 4)	(Note 4)	High-Z

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 9V-10.5V, V_{HH} = 9V-10.5V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In
Notes:
1. Addresses are A21:A0 in word mode ($\overline{BYTE}$ =V_{IH}), A21: A-1 in byte mode ($\overline{BYTE}$=V_{IL}).
2. The sector protect and sector unprotect functions may also be implemented via programming equipment. See “Sector/Sector Block Protection and Unprotection”.
3. If $\overline{WP}$ /ACC=V_{IL}, the two outermost boot sectors remain protected. If $\overline{WP}$ /ACC=V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in “Sector/Sector Block Protection and Unprotection. If $\overline{WP}$/ACC = V_{HH}, all sectors are unprotected. If $\overline{WP}$ /ACC is left floating, it is internally held to VDD via a pull-up resistor.
4. D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protection algorithm.

Word/Byte Configuration

The $\overline{BYTE}$ pin determines whether the I/O pins I/O_{15}-I/O_0 operate in the byte or word configuration. If the $\overline{BYTE}$ pin is set at logic ”1”, the device is in word configuration, I/O_{15}-I/O_0 are active and controlled by $\overline{CE}$ and $\overline{OE}$.

If the $\overline{BYTE}$ pin is set at logic “0”, the device is in byte configuration, and only I/O_0-I/O_7 are active and controlled by $\overline{CE}$ and $\overline{OE}$. I/O_8-I/O_{14} are tri-stated, and I/O_{15} pin is used as an input for the LSB(A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to V_{IL}. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at V_{IH} all the time during read operation. The $\overline{BYTE}$ pin determines whether the device outputs array data in words and bytes. The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.
See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms, I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}. For program operations, the $\overline{BYTE}$ pin determines whether the device accepts program data in bytes or words, Refer to “Word/Byte Configuration” for more information. The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “
Word / Byte Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequence. An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address range that each sector occupies. A "sector address" consists of the address inputs required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.
After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on I/O_7 - I/O_0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on I/O_7 - I/O_0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the $\overline{OE}$ input.
The device enters the CMOS standby mode when the $\overline{CE}$ & $\overline{RESET}$ pins are both held at VCC ± 0.3V. (Note that this is a more restricted voltage range than V_{IH}.) If $\overline{CE}$ and $\overline{RESET}$ are held at V_{IH}, but not within VCC ± 0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires the standard access time (t_{CE}) before it is ready to read data.
If the device is deselected during erasure or programming, the device draws active current until the operation is completed.
I_{CC3} and I_{CC4} in the DC Characteristics tables represent the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} +30ns. The automatic sleep mode is independent of the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

Output Disable Mode

When the $\overline{OE}$ input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

$\overline{RESET}$: Hardware Reset Pin

The $\overline{RESET}$ pin provides a hardware method of resetting the device to reading array data. When the system drives the $\overline{RESET}$ pin low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.
Current is reduced for the duration of the $\overline{RESET}$ pulse. When $\overline{RESET}$ is held at VSS ± 0.3V, the device draws

CMOS standby current (I_{CC4}). If $\overline{RESET}$ is held at V_{IL} but not within $V_{SS} \pm 0.3V$, the standby current will be greater.
The $\overline{RESET}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.
If $\overline{RESET}$ is asserted during a program or erase operation, the RY/$\overline{BY}$ pin remains a "0" (busy) until the internal reset operation is complete, which requires a time t_{READY} (during Embedded Algorithms). The system can thus monitor RY/$\overline{BY}$ to determine whether the reset operation is complete. If $\overline{RESET}$ is asserted when a program or erase operation is not executing (RY/$\overline{BY}$ pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the $\overline{RESET}$ pin return to V_{IH}.
Refer to the AC Characteristics tables for $\overline{RESET}$ parameters and diagram.

Table 2. A29L640 Top Boot Block Sector Address Table

Sector	A21-A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
			Byte Mode (x8)	Word Mode (x16)
SA0	0000000XXX	64/32	000000–00FFFF	000000–007FFF
SA1	0000001XXX	64/32	010000–01FFFF	008000–00FFFF
SA2	0000010XXX	64/32	020000–02FFFF	010000–017FFF
SA3	0000011XXX	64/32	030000–03FFFF	018000–01FFFF
SA4	0000100XXX	64/32	040000–04FFFF	020000–027FFF
SA5	0000101XXX	64/32	050000–05FFFF	028000–02FFFF
SA6	0000110XXX	64/32	060000–06FFFF	030000–037FFF
SA7	0000111XXX	64/32	070000–07FFFF	038000–03FFFF
SA8	0001000XXX	64/32	080000–08FFFF	040000–047FFF
SA9	0001001XXX	64/32	090000–09FFFF	048000–04FFFF
SA10	0001010XXX	64/32	0A0000–0AFFFF	050000–057FFF
SA11	0001011XXX	64/32	0B0000–0BFFFF	058000–05FFFF
SA12	0001100XXX	64/32	0C0000–0CFFFF	060000–067FFF
SA13	0001101XXX	64/32	0D0000–0DFFFF	068000–06FFFF
SA14	0001110XXX	64/32	0E0000–0EFFFF	070000–077FFF
SA15	0001111XXX	64/32	0F0000–0FFFFF	078000–07FFFF
SA16	0010000XXX	64/32	100000–10FFFF	080000–087FFF
SA17	0010001XXX	64/32	110000–11FFFF	088000–08FFFF
SA18	0010010XXX	64/32	120000–12FFFF	090000–097FFF
SA19	0010011XXX	64/32	130000–13FFFF	098000–09FFFF
SA20	0010100XXX	64/32	140000–14FFFF	0A0000–0A7FFF
SA21	0010101XXX	64/32	150000–15FFFF	0A8000–0AFFFF
SA22	0010110XXX	64/32	160000–16FFFF	0B0000–0B7FFF
SA23	0010111XXX	64/32	170000–17FFFF	0B8000–0BFFFF
SA24	0011000XXX	64/32	180000–18FFFF	0C0000–0C7FFF
SA25	0011001XXX	64/32	190000–19FFFF	0C8000–0CFFFF
SA26	0011010XXX	64/32	1A0000–1AFFFF	0D0000–0D7FFF
SA27	0011011XXX	64/32	1B0000–1BFFFF	0D8000–0DFFFF
SA28	0011100XXX	64/32	1C0000–1CFFFF	0E0000–0E7FFF
SA29	0011101XXX	64/32	1D0000–1DFFFF	0E8000–0EFFFF
SA30	0011110XXX	64/32	1E0000–1EFFFF	0F0000–0F7FFF
SA31	0011111XXX	64/32	1F0000–1FFFFF	0F8000–0FFFFF
SA32	0100000XXX	64/32	200000–20FFFF	100000–107FFF
SA33	0100001XXX	64/32	210000–21FFFF	108000–10FFFF
SA34	0100010XXX	64/32	220000–22FFFF	110000–117FFF
SA35	0100011XXX	64/32	230000–23FFFF	118000–11FFFF
SA36	0100100XXX	64/32	240000–24FFFF	120000–127FFF
SA37	0100101XXX	64/32	250000–25FFFF	128000–12FFFF
SA38	0100110XXX	64/32	260000–26FFFF	130000–137FFF

Table 2. A29L640 Top Boot Block Sector Address Table (continued)

Sector	A21-A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
			Byte Mode (x8)	Word Mode (x16)
SA39	0100111XXX	64/32	270000–27FFFF	138000–13FFFF
SA40	0101000XXX	64/32	280000–28FFFF	140000–147FFF
SA41	0101001XXX	64/32	290000–29FFFF	148000–14FFFF
SA42	0101010XXX	64/32	2A0000–2AFFFF	150000–157FFF
SA43	0101011XXX	64/32	2B0000–2BFFFF	158000–15FFFF
SA44	0101100XXX	64/32	2C0000–2CFFFF	160000–167FFF
SA45	0101101XXX	64/32	2D0000–2DFFFF	168000–16FFFF
SA46	0101110XXX	64/32	2E0000–2EFFFF	170000–177FFF
SA47	0101111XXX	64/32	2F0000–2FFFFF	178000–17FFFF
SA48	0110000XXX	64/32	300000–30FFFF	180000–187FFF
SA49	0110001XXX	64/32	310000–31FFFF	188000–18FFFF
SA50	0110010XXX	64/32	320000–32FFFF	190000–197FFF
SA51	0110011XXX	64/32	330000–33FFFF	198000–19FFFF
SA52	0110100XXX	64/32	340000–34FFFF	1A0000–1A7FFF
SA53	0110101XXX	64/32	350000–35FFFF	1A8000–1AFFFF
SA54	0110110XXX	64/32	360000–36FFFF	1B0000–1B7FFF
SA55	0110111XXX	64/32	370000–37FFFF	1B8000–1BFFFF
SA56	0111000XXX	64/32	380000–38FFFF	1C0000–1C7FFF
SA57	0111001XXX	64/32	390000–39FFFF	1C8000–1CFFFF
SA58	0111010XXX	64/32	3A0000–3AFFFF	1D0000–1D7FFF
SA59	0111011XXX	64/32	3B0000–3BFFFF	1D8000–1DFFFF
SA60	0111100XXX	64/32	3C0000–3CFFFF	1E0000–1E7FFF
SA61	0111101XXX	64/32	3D0000–3DFFFF	1E8000–1EFFFF
SA62	0111110XXX	64/32	3E0000–3EFFFF	1F0000–1F7FFF
SA63	0111111XXX	64/32	3F0000–3FFFFF	1F8000–1FFFFF
SA64	1000000XXX	64/32	400000–40FFFF	200000–207FFF
SA65	1000001XXX	64/32	410000–41FFFF	208000–20FFFF
SA66	1000010XXX	64/32	420000–42FFFF	210000–217FFF
SA67	1000011XXX	64/32	430000–43FFFF	218000–21FFFF
SA68	1000100XXX	64/32	440000–44FFFF	220000–227FFF
SA69	1000101XXX	64/32	450000–45FFFF	228000–22FFFF
SA70	1000110XXX	64/32	460000–46FFFF	230000–237FFF
SA71	1000111XXX	64/32	470000–47FFFF	238000–23FFFF
SA72	1001000XXX	64/32	480000–48FFFF	240000–247FFF
SA73	1001001XXX	64/32	490000–49FFFF	248000–24FFFF
SA74	1001010XXX	64/32	4A0000–4AFFFF	250000–257FFF
SA75	1001011XXX	64/32	4B0000–4BFFFF	258000–25FFFF
SA76	1001100XXX	64/32	4C0000–4CFFFF	260000–267FFF
SA77	1001101XXX	64/32	4D0000–4DFFFF	268000–26FFFF
SA78	1001110XXX	64/32	4E0000–4EFFFF	270000–277FFF
SA79	1001111XXX	64/32	4F0000–4FFFFF	278000–27FFFF
SA80	1010000XXX	64/32	500000–50FFFF	280000–287FFF
SA81	1010001XXX	64/32	510000–51FFFF	288000–28FFFF
SA82	1010010XXX	64/32	520000–52FFFF	290000–297FFF
SA83	1010011XXX	64/32	530000–53FFFF	298000–29FFFF
SA84	1010100XXX	64/32	540000–54FFFF	2A0000–2A7FFF
SA85	1010101XXX	64/32	550000–55FFFF	2A8000–2AFFFF
SA86	1010110XXX	64/32	560000–56FFFF	2B0000–2B7FFF

Table 2. A29L640 Top Boot Block Sector Address Table (continued)

Sector	A21-A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
			Byte Mode (x8)	Word Mode (x16)
SA87	1010111XXX	64/32	570000–57FFFF	2B8000–2BFFFF
SA88	1011000XXX	64/32	580000–58FFFF	2C0000–2C7FFF
SA89	1011001XXX	64/32	590000–59FFFF	2C8000–2CFFFF
SA90	1011010XXX	64/32	5A0000–5AFFFF	2D0000–2D7FFF
SA91	1011011XXX	64/32	5B0000–5BFFFF	2D8000–2DFFFF
SA92	1011100XXX	64/32	5C0000–5CFFFF	2E0000–2E7FFF
SA93	1011101XXX	64/32	5D0000–5DFFFF	2E8000–2EFFFF
SA94	1011110XXX	64/32	5E0000–5EFFFF	2F0000–2F7FFF
SA95	1011111XXX	64/32	5F0000–5FFFFF	2F8000–2FFFFF
SA96	1100000XXX	64/32	600000–60FFFF	300000–307FFF
SA97	1100001XXX	64/32	610000–61FFFF	308000–30FFFF
SA98	1100010XXX	64/32	620000–62FFFF	310000–317FFF
SA99	1100011XXX	64/32	630000–63FFFF	318000–31FFFF
SA100	1100100XXX	64/32	640000–64FFFF	320000–327FFF
SA101	1100101XXX	64/32	650000–65FFFF	328000–32FFFF
SA102	1100110XXX	64/32	660000–66FFFF	330000–337FFF
SA103	1100111XXX	64/32	670000–67FFFF	338000–33FFFF
SA104	1101000XXX	64/32	680000–68FFFF	340000–347FFF
SA105	1101001XXX	64/32	690000–69FFFF	348000–34FFFF
SA106	1101010XXX	64/32	6A0000–6AFFFF	350000–357FFF
SA107	1101011XXX	64/32	6B0000–6BFFFF	358000–35FFFF
SA108	1101100XXX	64/32	6C0000–6CFFFF	360000–367FFF
SA109	1101101XXX	64/32	6D0000–6DFFFF	368000–36FFFF
SA110	1101110XXX	64/32	6E0000–6EFFFF	370000–377FFF
SA111	1101111XXX	64/32	6F0000–6FFFFF	378000–37FFFF
SA112	1110000XXX	64/32	700000–70FFFF	380000–387FFF
SA113	1110001XXX	64/32	710000–71FFFF	388000–38FFFF
SA114	1110010XXX	64/32	720000–72FFFF	390000–397FFF
SA115	1110011XXX	64/32	730000–73FFFF	398000–39FFFF
SA116	1110100XXX	64/32	740000–74FFFF	3A0000–3A7FFF
SA117	1110101XXX	64/32	750000–75FFFF	3A8000–3AFFFF
SA118	1110110XXX	64/32	760000–76FFFF	3B0000–3B7FFF
SA119	1110111XXX	64/32	770000–77FFFF	3B8000–3BFFFF
SA120	1111000XXX	64/32	780000–78FFFF	3C0000–3C7FFF
SA121	1111001XXX	64/32	790000–79FFFF	3C8000–3CFFFF
SA122	1111010XXX	64/32	7A0000–7AFFFF	3D0000–3D7FFF
SA107	1101011XXX	64/32	6B0000–6BFFFF	358000–35FFFF
SA108	1101100XXX	64/32	6C0000–6CFFFF	360000–367FFF
SA109	1101101XXX	64/32	6D0000–6DFFFF	368000–36FFFF
SA110	1101110XXX	64/32	6E0000–6EFFFF	370000–377FFF
SA111	1101111XXX	64/32	6F0000–6FFFFF	378000–37FFFF
SA112	1110000XXX	64/32	700000–70FFFF	380000–387FFF
SA113	1110001XXX	64/32	710000–71FFFF	388000–38FFFF
SA114	1110010XXX	64/32	720000–72FFFF	390000–397FFF
SA115	1110011XXX	64/32	730000–73FFFF	398000–39FFFF
SA116	1110100XXX	64/32	740000–74FFFF	3A0000–3A7FFF
SA117	1110101XXX	64/32	750000–75FFFF	3A8000–3AFFFF
SA118	1110110XXX	64/32	760000–76FFFF	3B0000–3B7FFF

Table 2. A29L640 Top Boot Block Sector Address Table (continued)

Sector	A21-A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
			Byte Mode (x8)	Word Mode (x16)
SA119	1110111XXX	64/32	770000–77FFFF	3B8000–3BFFFF
SA120	1111000XXX	64/32	780000–78FFFF	3C0000–3C7FFF
SA121	1111001XXX	64/32	790000–79FFFF	3C8000–3CFFFF
SA122	1111010XXX	64/32	7A0000–7AFFFF	3D0000–3D7FFF
SA123	1111011XXX	64/32	7B0000–7BFFFF	3D8000–3DFFFF
SA124	1111100XXX	64/32	7C0000–7CFFFF	3E0000–3E7FFF
SA125	1111101XXX	64/32	7D0000–7DFFFF	3E8000–3EFFFF
SA126	1111110XXX	64/32	7E0000–7EFFFF	3F0000–3F7FFF
SA127	1111111000	8/4	7F0000–7F1FFF	3F8000–3F8FFF
SA128	1111111001	8/4	7F2000–7F3FFF	3F9000–3F9FFF
SA129	1111111010	8/4	7F4000–7F5FFF	3FA000–3FAFFF
SA130	1111111011	8/4	7F6000–7F7FFF	3FB000–3FBFFF
SA131	1111111100	8/4	7F8000–7F9FFF	3FC000–3FCFFF
SA132	1111111101	8/4	7FA000–7FBFFF	3FD000–3FDFFF
SA133	1111111110	8/4	7FC000–7FDFFF	3FE000–3FEFFF
SA134	1111111111	8/4	7FE000–7FFFFF	3FF000–3FFFFF

Top Boot Security Sector Addresses

Sector Size		Sector Address A21-A12	Address Range (in hexadecimal)	
Byte Mode (bytes)	Word Mode (words)		Byte Mode (x8)	Word Mode (x16)
256	128	1111111111	7FFF00–7FFFFF	3FFF80–3FFFFF

Note:
Address range is A21: A-1 in byte mode and A21 : A0 in word mode. See “Word/Byte Configuration” section.

Table 3. A29L640 Bottom Boot Block Sector Address Table

Sector	A21 -A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
			Byte Mode (x8)	Word Mode (x16)
SA0	0000000000	8/4	000000–001FFF	000000–000FFF
SA1	0000000001	8/4	002000–003FFF	001000–001FFF
SA2	0000000010	8/4	004000–005FFF	002000–002FFF
SA3	0000000011	8/4	006000–007FFF	003000–003FFF
SA4	0000000100	8/4	008000–009FFF	004000–004FFF
SA5	0000000101	8/4	00A000–00BFFF	005000–005FFF
SA6	0000000110	8/4	00C000–00DFFF	006000–006FFF
SA7	0000000111	8/4	00E000–00FFFF	007000–007FFF
SA8	0000001XXX	64/32	010000–01FFFF	008000–00FFFF
SA9	0000010XXX	64/32	020000–02FFFF	010000–017FFF
SA10	0000011XXX	64/32	030000–03FFFF	018000–01FFFF
SA11	0000100XXX	64/32	040000–04FFFF	020000–027FFF
SA12	0000101XXX	64/32	050000–05FFFF	028000–02FFFF
SA13	0000110XXX	64/32	060000–06FFFF	030000–037FFF
SA14	0000111XXX	64/32	070000–07FFFF	038000–03FFFF
SA15	0001000XXX	64/32	080000–08FFFF	040000–047FFF
SA16	0001001XXX	64/32	090000–09FFFF	048000–04FFFF
SA17	0001010XXX	64/32	0A0000–0AFFFF	050000–057FFF
SA18	0001011XXX	64/32	0B0000–0BFFFF	058000–05FFFF
SA19	0001100XXX	64/32	0C0000–0CFFFF	060000–067FFF
SA20	0001101XXX	64/32	0D0000–0DFFFF	068000–06FFFF
SA21	0001110XXX	64/32	0E0000–0EFFFF	070000–077FFF
SA22	0001111XXX	64/32	0F0000–0FFFFF	078000–07FFFF
SA23	0010000XXX	64/32	100000–10FFFF	080000–087FFF
SA24	0010001XXX	64/32	110000–11FFFF	088000–08FFFF
SA25	0010010XXX	64/32	120000–12FFFF	090000–097FFF
SA26	0010011XXX	64/32	130000–13FFFF	098000–09FFFF
SA27	0010100XXX	64/32	140000–14FFFF	0A0000–0A7FFF
SA28	0010101XXX	64/32	150000–15FFFF	0A8000–0AFFFF
SA29	0010110XXX	64/32	160000–16FFFF	0B0000–0B7FFF
SA30	0010111XXX	64/32	170000–17FFFF	0B8000–0BFFFF
SA31	0011000XXX	64/32	180000–18FFFF	0C0000–0C7FFF
SA32	0011001XXX	64/32	190000–19FFFF	0C8000–0CFFFF
SA33	0011010XXX	64/32	1A0000–1AFFFF	0D0000–0D7FFF
SA34	0011011XXX	64/32	1B0000–1BFFFF	0D8000–0DFFFF
SA35	0011100XXX	64/32	1C0000–1CFFFF	0E0000–0E7FFF
SA36	0011101XXX	64/32	1D0000–1DFFFF	0E8000–0EFFFF
SA37	0011110XXX	64/32	1E0000–1EFFFF	0F0000–0F7FFF
SA38	0011111XXX	64/32	1F0000–1FFFFF	0F8000–0FFFFF
SA39	0100000XXX	64/32	200000–20FFFF	100000–107FFF
SA40	0100001XXX	64/32	210000–21FFFF	108000–10FFFF
SA41	0100010XXX	64/32	220000–22FFFF	110000–117FFF
SA42	0100011XXX	64/32	230000–23FFFF	118000–11FFFF
SA43	0100100XXX	64/32	240000–24FFFF	120000–127FFF
SA44	0100101XXX	64/32	250000–25FFFF	128000–12FFFF
SA45	0100110XXX	64/32	260000–26FFFF	130000–137FFF
SA46	0100111XXX	64/32	270000–27FFFF	138000–13FFFF
SA47	0101000XXX	64/32	280000–28FFFF	140000–147FFF

Table 3. A29L640 Bottom Boot Block Sector Address Table (continued)

Sector	A21 -A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
			Byte Mode (x8)	Word Mode (x16)
SA48	0101001XXX	64/32	290000–29FFFF	148000–14FFFF
SA49	0101010XXX	64/32	2A0000–2AFFFF	150000–157FFF
SA50	0101011XXX	64/32	2B0000–2BFFFF	158000–15FFFF
SA51	0101100XXX	64/32	2C0000–2CFFFF	160000–167FFF
SA52	0101101XXX	64/32	2D0000–2DFFFF	168000–16FFFF
SA53	0101110XXX	64/32	2E0000–2EFFFF	170000–177FFF
SA54	0101111XXX	64/32	2F0000–2FFFFF	178000–17FFFF
SA55	0110000XXX	64/32	300000–30FFFF	180000–187FFF
SA56	0110001XXX	64/32	310000–31FFFF	188000–18FFFF
SA57	0110010XXX	64/32	320000–32FFFF	190000–197FFF
SA58	0110011XXX	64/32	330000–33FFFF	198000–19FFFF
SA59	0110100XXX	64/32	340000–34FFFF	1A0000–1A7FFF
SA60	0110101XXX	64/32	350000–35FFFF	1A8000–1AFFFF
SA61	0110110XXX	64/32	360000–36FFFF	1B0000–1B7FFF
SA62	0110111XXX	64/32	370000–37FFFF	1B8000–1BFFFF
SA63	0111000XXX	64/32	380000–38FFFF	1C0000–1C7FFF
SA64	0111001XXX	64/32	390000–39FFFF	1C8000–1CFFFF
SA65	0111010XXX	64/32	3A0000–3AFFFF	1D0000–1D7FFF
SA66	0111011XXX	64/32	3B0000–3BFFFF	1D8000–1DFFFF
SA67	0111100XXX	64/32	3C0000–3CFFFF	1E0000–1E7FFF
SA68	0111101XXX	64/32	3D0000–3DFFFF	1E8000–1EFFFF
SA69	0111110XXX	64/32	3E0000–3EFFFF	1F0000–1F7FFF
SA70	0111111XXX	64/32	3F0000–3FFFFF	1F8000–1FFFFF
SA71	1000000XXX	64/32	400000–40FFFF	200000–207FFF
SA72	1000001XXX	64/32	410000–41FFFF	208000–20FFFF
SA73	1000010XXX	64/32	420000–42FFFF	210000–217FFF
SA74	1000011XXX	64/32	430000–43FFFF	218000–21FFFF
SA75	1000100XXX	64/32	440000–44FFFF	220000–227FFF
SA76	1000101XXX	64/32	450000–45FFFF	228000–22FFFF
SA77	1000110XXX	64/32	460000–46FFFF	230000–237FFF
SA78	1000111XXX	64/32	470000–47FFFF	238000–23FFFF
SA79	1001000XXX	64/32	480000–48FFFF	240000–247FFF
SA80	1001001XXX	64/32	490000–49FFFF	248000–24FFFF
SA81	1001010XXX	64/32	4A0000–4AFFFF	250000–257FFF
SA82	1001011XXX	64/32	4B0000–4BFFFF	258000–25FFFF
SA83	1001100XXX	64/32	4C0000–4CFFFF	260000–267FFF
SA84	1001101XXX	64/32	4D0000–4DFFFF	268000–26FFFF
SA85	1001110XXX	64/32	4E0000–4EFFFF	270000–277FFF
SA86	1001111XXX	64/32	4F0000–4FFFFF	278000–27FFFF
SA87	1010000XXX	64/32	500000–50FFFF	280000–287FFF
SA88	1010001XXX	64/32	510000–51FFFF	288000–28FFFF
SA89	1010010XXX	64/32	520000–52FFFF	290000–297FFF
SA90	1010011XXX	64/32	530000–53FFFF	298000–29FFFF
SA91	1010100XXX	64/32	540000–54FFFF	2A0000–2A7FFF
SA92	1010101XXX	64/32	550000–55FFFF	2A8000–2AFFFF
SA93	1010110XXX	64/32	560000–56FFFF	2B0000–2B7FFF
SA94	1010111XXX	64/32	570000–57FFFF	2B8000–2BFFFF
SA95	1011000XXX	64/32	580000–58FFFF	2C0000–2C7FFF

Table 3. A29L640 Bottom Boot Block Sector Address Table (continued)

Sector	A21 -A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
			Byte Mode (x8)	Word Mode (x16)
SA96	1011001XXX	64/32	590000–59FFFF	2C8000–2CFFFF
SA97	1011010XXX	64/32	5A0000–5AFFFF	2D0000–2D7FFF
SA98	1011011XXX	64/32	5B0000–5BFFFF	2D8000–2DFFFF
SA99	1011100XXX	64/32	5C0000–5CFFFF	2E0000–2E7FFF
SA100	1011101XXX	64/32	5D0000–5DFFFF	2E8000–2EFFFF
SA101	1011110XXX	64/32	5E0000–5EFFFF	2F0000–2F7FFF
SA102	1011111XXX	64/32	5F0000–5FFFFF	2F8000–2FFFFF
SA103	1100000XXX	64/32	600000–60FFFF	300000–307FFF
SA104	1100001XXX	64/32	610000–61FFFF	308000–30FFFF
SA105	1100010XXX	64/32	620000–62FFFF	310000–317FFF
SA106	1100011XXX	64/32	630000–63FFFF	318000–31FFFF
SA107	1100100XXX	64/32	640000–64FFFF	320000–327FFF
SA108	1100101XXX	64/32	650000–65FFFF	328000–32FFFF
SA109	1100110XXX	64/32	660000–66FFFF	330000–337FFF
SA110	1100111XXX	64/32	670000–67FFFF	338000–33FFFF
SA111	1101000XXX	64/32	680000–68FFFF	340000–347FFF
SA112	1101001XXX	64/32	690000–69FFFF	348000–34FFFF
SA113	1101010XXX	64/32	6A0000–6AFFFF	350000–357FFF
SA114	1101011XXX	64/32	6B0000–6BFFFF	358000–35FFFF
SA115	1101100XXX	64/32	6C0000–6CFFFF	360000–367FFF
SA116	1101101XXX	64/32	6D0000–6DFFFF	368000–36FFFF
SA117	1101110XXX	64/32	6E0000–6EFFFF	370000–377FFF
SA118	1101111XXX	64/32	6F0000–6FFFFF	378000–37FFFF
SA119	1110000XXX	64/32	700000–70FFFF	380000–387FFF
SA120	1110001XXX	64/32	710000–71FFFF	388000–38FFFF
SA121	1110010XXX	64/32	720000–72FFFF	390000–397FFF
SA122	1110011XXX	64/32	730000–73FFFF	398000–39FFFF
SA123	1110100XXX	64/32	740000–74FFFF	3A0000–3A7FFF
SA124	1110101XXX	64/32	750000–75FFFF	3A8000–3AFFFF
SA125	1110110XXX	64/32	760000–76FFFF	3B0000–3B7FFF
SA126	1110111XXX	64/32	770000–77FFFF	3B8000–3BFFFF
SA127	1111000XXX	64/32	780000–78FFFF	3C0000–3C7FFF
SA128	1111001XXX	64/32	790000–79FFFF	3C8000–3CFFFF
SA129	1111010XXX	64/32	7A0000–7AFFFF	3D0000–3D7FFF
SA130	1111011XXX	64/32	7B0000–7BFFFF	3D8000–3DFFFF
SA131	1111100XXX	64/32	7C0000–7CFFFF	3E0000–3E7FFF
SA132	1111101XXX	64/32	7D0000–7DFFFF	3E8000–3EFFFF
SA133	1111110XXX	64/32	7E0000–7EFFFF	3F0000–3F7FFF
SA134	1111111XXX	64/32	7F0000–7FFFFF	3F8000–3FFFFF

Bottom Boot Security Sector Addresses

Sector Size		Sector Address A21-A12	Address Range (in hexadecimal)	
Byte Mode (bytes)	Word Mode (words)		Byte Mode (x8)	Word Mode (x16)
256	128	0000000000	000000–0000FF	000000–00007F

Note:
Address range is A21 : A-1 in byte mode and A21 : A0 in word mode. See “Word/Byte Configuration” section.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on I/O7 -I/O0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.
When using programming equipment, the autoselect mode requires V_{ID} (**9**V to 10.5V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on I/O7 - I/O0.To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Security Sector Flash Memory Region

The Security Sector region is an extra memory space of 128 words in length. The security sectors can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device
In factory-locked device, security sector region is protected when shipping from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipping from factory and the security silicon indicator bit is set to "0".
Factory Locked: Security Sector Programmed and Protected at the factory
In a factory locked device, the security silicon region is permanently locked after shipping from factory. The device will have a 16-byte (8-word) ESN in the security region. In bottom boot device: 000000h – 000007h. In Top boot device: 3FFFF8 h– 3FFFFFh.
Customer Lockable: Security Sector NOT Programmed or Protected at the factory
When the security feature is not required, the security region can act as an extra memory space.
Security silicon sector can also be protected the method listed below. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.
The method is to write a three-cycle command of enter Security Region, and then follow the sector group protect algorithm as illustrated in Fig 2-1, except that /RESET pin may at either V_{IH} or V_{HH}.
After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

Table 4. A29L640 Autoselect Codes (High Voltage Method)

Description	Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A21 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	I/O_8 to I/O_{15}	I/O_7 to I/O_0
Manufacturer ID: AMIC		L	L	H	X	X	V_{ID}	X	L	X	L	L	X	37h
Device ID: A29L640 (Top Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	C9h
	Byte												X	C9h
Device ID: A29L640 (Bottom Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	CBh
	Byte												X	CBh
Indicator for Security Sector		L	L	H	X	X	V_{ID}	X	L	X	H	H	X	(Note 2)
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
													X	00h (unprotected)

L=Logic Low= V_{IL}, H=Logic High=V_{IH}, SA=Sector Address, X=Don't Care.
Note: 1. The autoselect codes may also be accessed in-system via command sequences.
2. Factory locked code: $\overline{WP}$ protects bottom two address sector: 88h.
$\overline{WP}$ protects top two address sector: 98h.
Factory unlocked code: $\overline{WP}$ protects bottom two address sector: 08h.
$\overline{WP}$ protects top two address sector: 18h.

Sector/Sector Block Protection and Unprotection

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Tables 5 and 6).

Table 5. Top Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector Group	Sectors	A21-A12	Sector Group Size
SG 0	SA0-SA3	00000XXXXX	64 Kbytes x 4
SG 1	SA4-SA 7	00001XXXXX	64 Kbytes x 4
SG 2	SA8-SA 11	00010XXXXX	64 Kbytes x 4
SG 3	SA 12-SA 15	00011XXXXX	64 Kbytes x 4
SG 4	SA 16-SA 19	00100XXXXX	64 Kbytes x 4
SG 5	SA 20-SA 23	00101XXXXX	64 Kbytes x 4
SG 6	SA 24-SA 27	00110XXXXX	64 Kbytes x 4
SG 7	SA 28-SA 31	00111XXXXX	64 Kbytes x 4
SG 8	SA 32-SA 35	01000XXXXX	64 Kbytes x 4
SG 9	SA 36-SA 39	01001XXXXX	64 Kbytes x 4
SG10	SA 40-SA 43	01010XXXXX	64 Kbytes x 4
SG11	SA 44-SA 47	01011XXXXX	64 Kbytes x 4
SG12	SA 48-SA 51	01100XXXXX	64 Kbytes x 4
SG13	SA 52-SA 55	01101XXXXX	64 Kbytes x 4
SG14	SA 56-SA 59	01110XXXXX	64 Kbytes x 4
SG15	SA 60-SA 63	01111XXXXX	64 Kbytes x 4
SG16	SA 64-SA 67	10000XXXXX	64 Kbytes x 4
SG17	SA 68-SA 71	10001XXXXX	64 Kbytes x 4
SG18	SA 72-SA 75	10010XXXXX	64 Kbytes x 4
SG19	SA 76-SA 79	10011XXXXX	64 Kbytes x 4
SG20	SA 80-SA 83	10100XXXXX	64 Kbytes x 4
SG21	SA 84-SA 87	10101XXXXX	64 Kbytes x 4
SG22	SA 88-SA 91	10110XXXXX	64 Kbytes x 4
SG23	SA 92-SA 95	10111XXXXX	64 Kbytes x 4
SG24	SA 96-SA 99	11000XXXXX	64 Kbytes x 4
SG25	SA100-SA103	11001XXXXX	64 Kbytes x 4
SG26	SA104-SA107	11010XXXXX	64 Kbytes x 4
SG27	SA108-SA111	11011XXXXX	64 Kbytes x 4
SG28	SA112-SA115	11100XXXXX	64 Kbytes x 4
SG29	SA116-SA119	11101XXXXX	64 Kbytes x 4
SG30	SA120-SA123	11110XXXXX	64 Kbytes x 4
SG31	SA124-SA126	1111100XXX 1111101XXX 1111110XXX	64 Kbytes x 3
SG32	SA127	1111111000	8 Kbytes
SG33	SA128	1111111001	8 Kbytes
SG34	SA129	1111111010	8 Kbytes
SG35	SA130	1111111011	8 Kbytes
SG36	SA131	1111111100	8 Kbytes
SG37	SA132	1111111101	8 Kbytes
SG38	SA133	1111111110	8 Kbytes
SG39	SA134	1111111111	8 Kbytes

Table 6. Bottom Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector Group	Sectors	A21-A12	Sector Group Size
SG39	SA134-SA131	11111XXXXX	64 Kbytes x 4
SG38	SA130-SA127	11110XXXXX	64 Kbytes x 4
SG37	SA126-SA123	11101XXXXX	64 Kbytes x 4
SG36	SA122-SA119	11100XXXXX	64 Kbytes x 4
SG35	SA118-SA115	11011XXXXX	64 Kbytes x 4
SG34	SA114-SA111	11010XXXXX	64 Kbytes x 4
SG33	SA110-SA107	11001XXXXX	64 Kbytes x 4
SG32	SA106-SA103	11000XXXXX	64 Kbytes x 4
SG31	SA102-SA 99	10111XXXXX	64 Kbytes x 4
SG30	SA 98-SA 95	10110XXXXX	64 Kbytes x 4
SG29	SA 94-SA 91	10101XXXXX	64 Kbytes x 4
SG28	SA 90-SA 87	10100XXXXX	64 Kbytes x 4
SG27	SA 86-SA 83	10011XXXXX	64 Kbytes x 4
SG26	SA 82-SA 79	10010XXXXX	64 Kbytes x 4
SG25	SA 78-SA 75	10001XXXXX	64 Kbytes x 4
SG24	SA 74-SA 71	10000XXXXX	64 Kbytes x 3
SG23	SA 70-SA 67	01111XXXXX	64 Kbytes x 4
SG22	SA 66-SA 63	01110XXXXX	64 Kbytes x 4
SG21	SA 62-SA 59	01101XXXXX	64 Kbytes x 4
SG20	SA 58-SA 55	01100XXXXX	64 Kbytes x 4
SG19	SA 54-SA 51	01011XXXXX	64 Kbytes x 4
SG18	SA 50-SA 47	01010XXXXX	64 Kbytes x 4
SG17	SA 46-SA 43	01001XXXXX	64 Kbytes x 4
SG16	SA 42-SA 39	01000XXXXX	64 Kbytes x 4
SG15	SA 38-SA 35	00111XXXXX	64 Kbytes x 4
SG14	SA 34-SA 31	00110XXXXX	64 Kbytes x 4
SG13	SA 30-SA 27	00101XXXXX	64 Kbytes x 4
SG12	SA 26-SA 23	00100XXXXX	64 Kbytes x 4
SG11	SA 22-SA 19	00011XXXXX	64 Kbytes x 4
SG10	SA 18-SA 15	00010XXXXX	64 Kbytes x 4
SG 9	SA 14-SA 11	00001XXXXX	64 Kbytes x 4
SG 8	SA 10-SA 8	0000011XXX 0000010XXX 0000001XXX	64 Kbytes x 3
SG 7	SA 7	0000000111	8 Kbytes
SG 6	SA 6	0000000110	8 Kbytes
SG 5	SA 5	0000000101	8 Kbytes
SG 4	SA 4	0000000100	8 Kbytes
SG 3	SA 3	0000000011	8 Kbytes
SG 2	SA 2	0000000010	8 Kbytes
SG 1	SA 1	0000000001	8 Kbytes
SG 0	SA 0	0000000000	8 Kbytes

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.
It is possible to determine whether a sector is protected or unprotected. See “Autoselect Mode” for details.
Sector protection / unprotection can be implemented via two methods. The primary method requires VID on the $\overline{\text{RESET}}$ pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithm and the Sector Protect / Unprotect Timing Diagram illustrates the timing waveforms for this feature. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. The alternate method for protection and unprotection is by software sector block protect/unprotect command. See Figure 2 for Command Flow.
The device is shipped with all sectors unprotected.
It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The requirement of command unlocking sequence for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up transitions, or from system noise. The device is powered up to read array data to avoid accidentally writing data to the array.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$ or $\overline{\text{WE}}$ do not initiate a write cycle.

Logical Inhibit

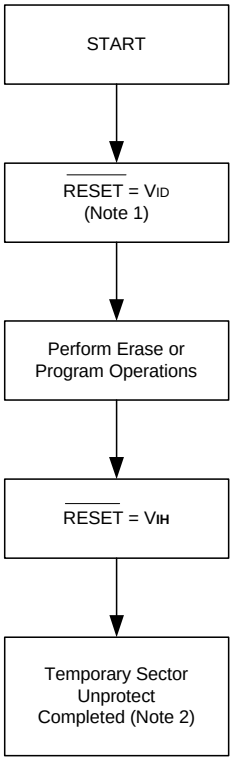
Write cycles are inhibited by holding any one of $\overline{\text{OE}}$ =V_{IL}, $\overline{\text{CE}}$ = V_{IH} or $\overline{\text{WE}}$ = V_{IH}. To initiate a write cycle, $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

Power-Up Write Inhibit

If $\overline{\text{WE}}$ = $\overline{\text{CE}}$ = V_{IL} and $\overline{\text{OE}}$ = V_{IH} during power up, the device does not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to reading array data on the initial power-up.

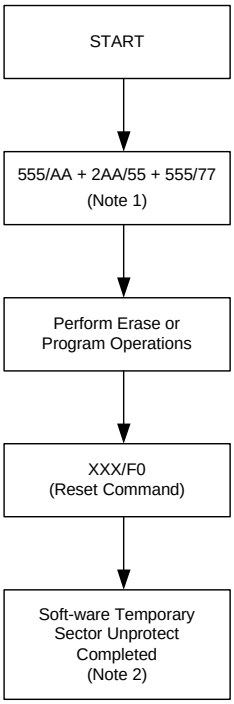
Temporary Sector Unprotect

This feature allows temporary unprotection of previous protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the $\overline{\text{RESET}}$ pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the $\overline{\text{RESET}}$ pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and the Temporary Sector Unprotect diagram shows the timing waveforms, for this feature.



Notes:
1. All protected sectors unprotected (If $\overline{WP}$/ACC=V_{IL}, outermost boot sectors will remain protected).
2. All previously protected sectors are protected once again.

Figure 1-1. Temporary Sector Unprotect Operation by $\overline{RESET}$ Mode



Notes:
1. All protected sectors unprotected (If $\overline{WP}$/ACC=V_{IL}, outermost boot sectors will remain protected).
2. All previously protected sectors are protected once again.

Figure 1-2. Temporary Sector Unprotect Operation by Software Mode

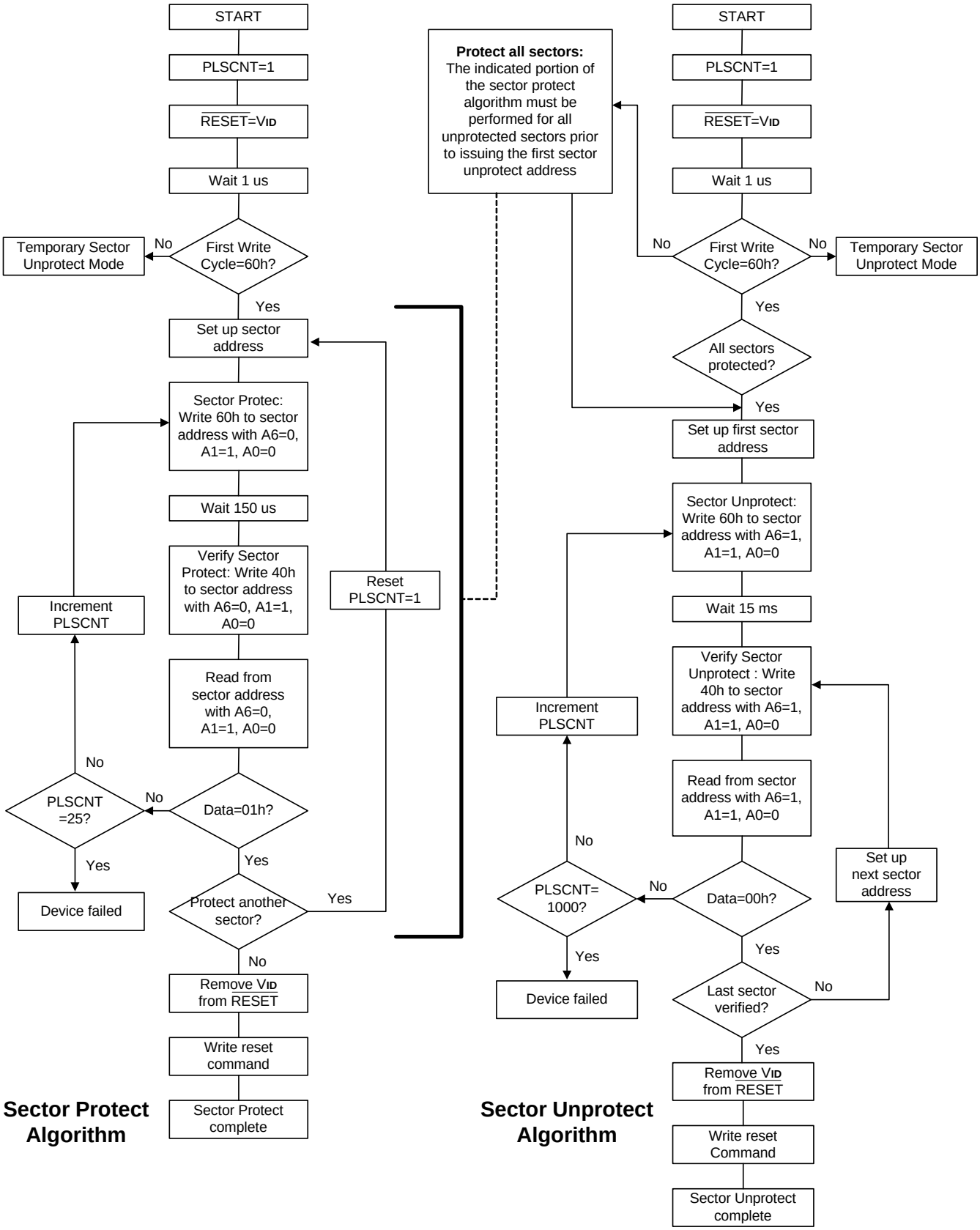
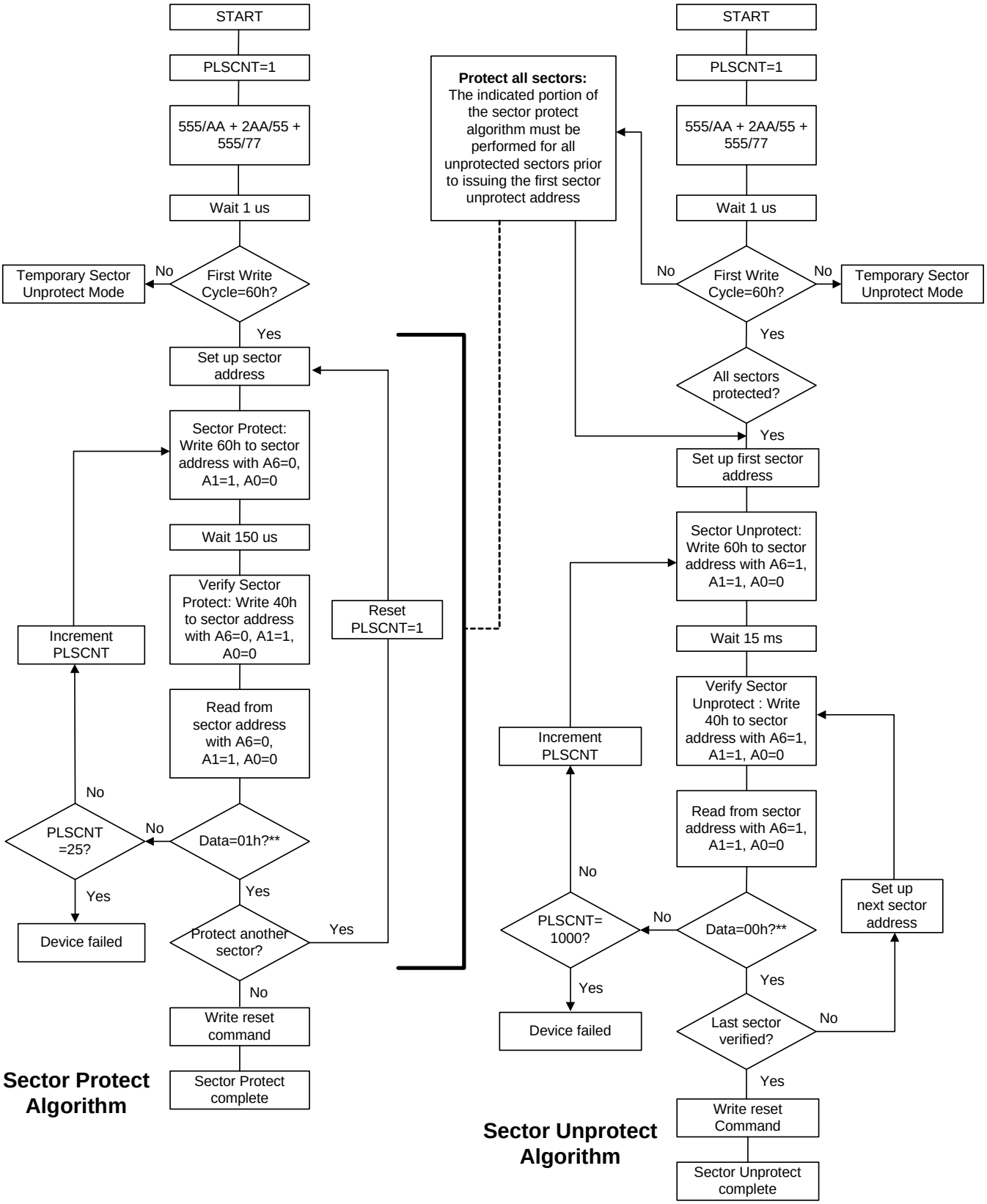


Figure 2-1. In-System Sector Protect/Unprotect Algorithms



Note: The term “sector” in the figure applies to both sectors and sector blocks
* No other command is allowed during this process
** Access time is 200ns-300ns

Figure 2-2. Software Sector/Sector Block Protection and Unprotection Algorithms

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interface for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 5-8. In word mode, the upper address bits (A7-MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 5-8. The system must write the reset command to return the device to the autoselect mode.

Table 7. CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 8. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	VCC Min. (write/erase) I/O7- I/O4 : volt, I/O3- I/O0: 100 millivolt
1Ch	38h	0036h	VCC Max. (write/erase) I/O7- I/O4: volt, I/O3- I/O0: 100 millivolt
1Dh	3Ah	0000h	Vpp Min. voltage (00h = no Vpp pin present)
1Eh	3Ch	0000h	Vpp Max. voltage (00h = no Vpp pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N μs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N μs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 9. Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0017h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification)
31h 32h 33h 34h	62h 64h 66h 68h	007Eh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 40h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3BH 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 10. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0031h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0004h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29L160 mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	0090h	ACC (Acceleration) Supply Minimum 00 = Not Supported, D7-D4: Volt, D3-D0: 100mV
4Eh	9Ch	00A5h	ACC (Acceleration) Supply Maximum 00 = Not Supported, D7-D4: Volt, D3-D0: 100mV
4Fh	9Eh	000Xh	Top/Bottom Boot Sector Flag 02 = Bottom Boot Device, 03h = Top Boot Device

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm. After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if I/O_5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If I/O_5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

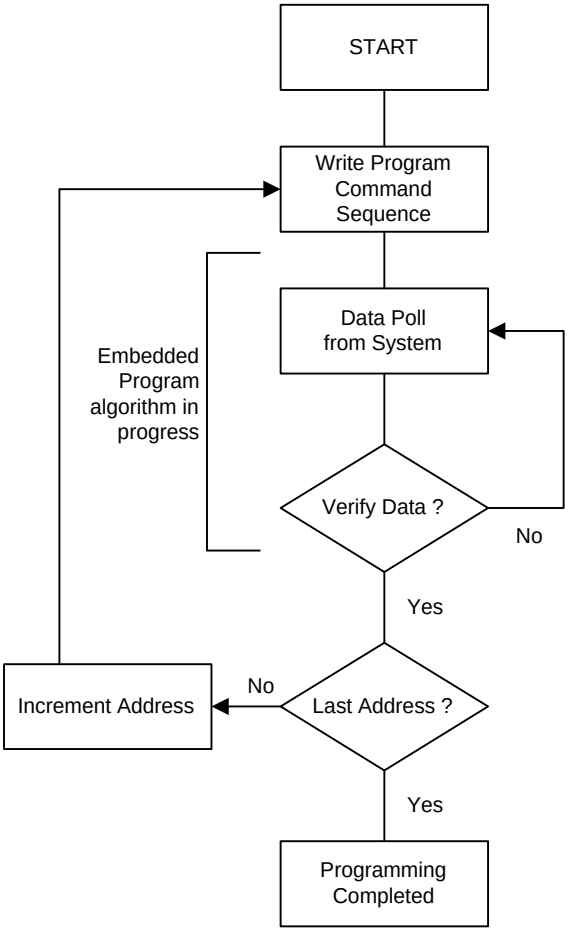
Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the $\overline{BYTE}$ pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. Table 9 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are longer latched. The system can determine the status of the program operation by using I/O_7, I/O_6, or RY/$\overline{BY}$. See “White Operation Status” for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a “0” back to a “1”. Attempting to do so may halt the operation and set I/O5 to “1”, or cause the $\overline{Data}$ Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.



Note : See the appropriate Command Definitions table for program command sequence.

Figure 3. Program Operation

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 9 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycle. The device returns to reading array data.

Figure 3 illustrates the algorithm for the program operation. See the Erase/Program Operations in "AC Characteristics" for parameters, and to Program Operation Timings for timing diagrams.

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The system can determine the status of the erase operation by using I/O_7, I/O_6, or I/O_2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six-bus-cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

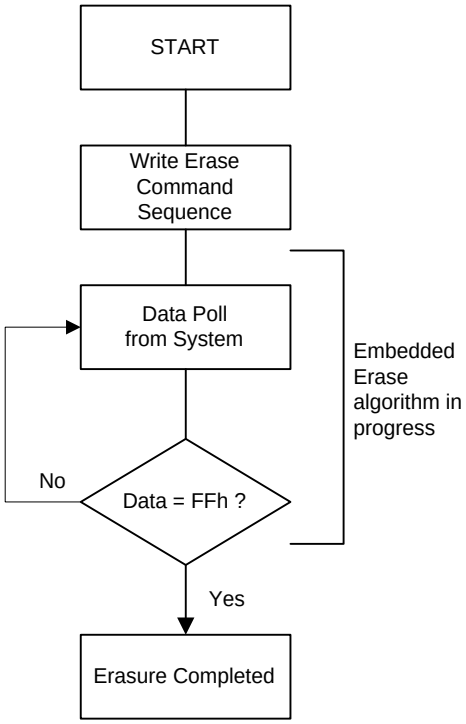
After the command sequence is written, a sector erase time-out of 50μs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50μs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50μs, the system need not monitor I/O_3. Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor I/O3 to determine if the sector erase timer has timed out. (See the " I/O3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.
Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.
When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using I/O7, I/O6, or I/O2. Refer to "Write Operation Status" for information on these status bits.
4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50μs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't cares" when writing the Erase Suspend command.
When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20μs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on I/O7 - I/O0. The system can use I/O7, or I/O6 and I/O2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.
After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the I/O7 or I/O6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.
The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Note :
1. See the appropriate Command Definitions table for erase command sequences.
2. See "I/O3 : Sector Erase Timer" for more information.

Figure 4. Erase Operation

Table 11. A29L640 Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2 - 5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	37				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	22F6				
		Byte		AAA		555		AAA		X02	F6				
	Security Sector Factory Protect Verify	Word	4	555	AA	2AA	55	555	90	X03	98/18(T) 88/08(B)				
		Byte		AAA	AA	555	55	AAA	90	X06	98/18(T) 88/08(B)				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
CFI Query (Note 11)		Word	1	55	98										
		Byte		AA											
Command Temporary Sector Unprotect (Note 10)		Word	3	555	AA	2AA	55	555	77						
		Byte		AAA		555		AAA							
Program		Byte	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 12)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 13)			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Enter Security Sector Region enable		Word	3	555	AA	2AA	55	555	88						
		Byte	3	AAA	AA	555	55	AAA	88						
Exit Security Sector		Word	4	555	AA	2AA	55	555	90	XXX	00				
		Byte	4	AAA	AA	555	55	AAA	90	XXX	00				
Erase Suspend (Note 14)			1	XXX	B0										
Erase Resume (Note 15)			1	XXX	30										

Legend:
X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A21- A12 select a unique sector.

Note:
1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operation.
4. Data bits DQ15-DQ8 are don't care in command sequences, except for RD and PD.
5. Address bits A21 - A11 are don't cares for unlock and command cycles, unless SA or PA required.
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the autoselect mode, or if I/O_5 goes high (while the device is providing status data).
8. The fourth cycle of the autoselect command sequence is a read cycle.
9. The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.
10. Once a reset command is applied, software temporary unprotect is exit to return to read array data. But under erase suspend condition, this command is still effective even a reset command has been applied. The reset command which can deactivate the software temporary unprotect command is useful only after the erase command is complete.
11. Command is valid when device is ready to read array data or when device is in autoselect mode.
12. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
13. The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.
14. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode.
15. The Erase Resume command is valid only during the Erase Suspend mode.

Write Operation Status

Several bits, I/O2, I/O3, I/O5, I/O6, I/O7, RY/$\overline{BY}$ are provided in the A29L640 to determine the status of a write operation. Table 10 and the following subsections describe the functions of these status bits. I/O7, I/O6 and RY/$\overline{BY}$ each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

I/O7: $\overline{Data}$ Polling

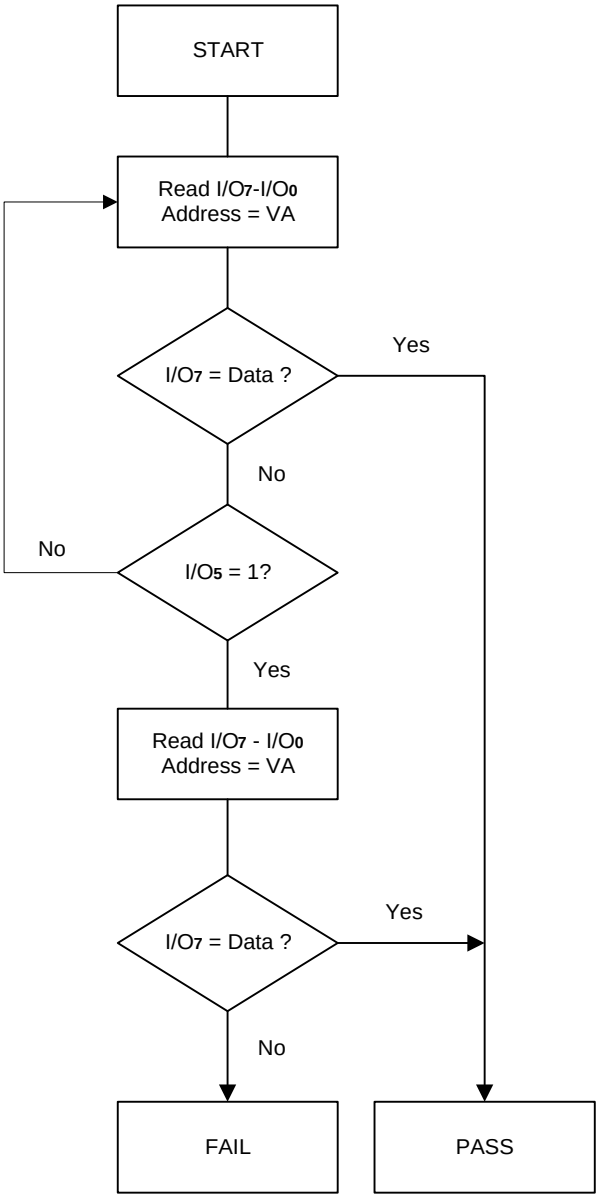
The $\overline{Data}$ Polling bit, I/O7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. $\overline{Data}$ Polling is valid after the rising edge of the final $\overline{WE}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on I/O7 the complement of the datum programmed to I/O7. This I/O7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to I/O7. The system must provide the program address to read valid status information on I/O7. If a program address falls within a protected sector, $\overline{Data}$ Polling on I/O7 is active for approximately 2μs, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{Data}$ Polling produces a "0" on I/O7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{Data}$ Polling produces a "1" on I/O7.This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on I/O7.

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{Data}$ Polling on I/O7 is active for approximately 100μs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects I/O7 has changed from the complement to true data, it can read valid data at I/O7 - I/O0 on the following read cycles. This is because I/O7 may change asynchronously with I/O0 - I/O6 while Output Enable ($\overline{OE}$) is asserted low. The $\overline{Data}$ Polling Timings (During Embedded Algorithms) figure in the "AC Characteristics" section illustrates this. Table 10 shows the outputs for $\overline{Data}$ Polling on I/O7. Figure 5 shows the $\overline{Data}$ Polling algorithm.



Note :
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 5. $\overline{Data}$ Polling Algorithm

RY/$\overline{BY}$: Read/$\overline{Busy}$

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Embedded algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to VCC (The RY/$\overline{BY}$ pin is not available on the 44-pin SOP package).
If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.
Table 10 shows the outputs for RY/$\overline{BY}$. Refer to "$\overline{RESET}$ Timings", "Timing Waveforms for Program Operation" and "Timing Waveforms for Chip/Sector Erase Operation" for more information.

I/O6: Toggle Bit I

Toggle Bit I on I/O6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.
During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause I/O6 to toggle. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) When the operation is complete, I/O6 stops toggling.
After an erase command sequence is written, if all sectors selected for erasing are protected, I/O6 toggles for approximately 100μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.
The system can use I/O6 and I/O2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), I/O6 toggles. When the device enters the Erase Suspend mode, I/O6 stops toggling. However, the system must also use I/O2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use I/O7 (see the subsection on " I/O7 : $\overline{Data}$ Polling").
If a program address falls within a protected sector, I/O6 toggles for approximately 2μs after the program command sequence is written, then returns to reading array data.
I/O6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.
The Write Operation Status table shows the outputs for Toggle Bit I on I/O6. Refer to Figure 6 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram. The I/O2 vs. I/O6 figure shows the differences between I/O2 and I/O6 in graphical form. See also the subsection on " I/O2: Toggle Bit II".

I/O2: Toggle Bit II

The "Toggle Bit II" on I/O2, when used with I/O6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence. I/O2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But I/O2 cannot distinguish whether the sector is actively erasing or is erase-suspended. I/O6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 10 to compare outputs for I/O2 and I/O6.
Figure 6 shows the toggle bit algorithm in flowchart form, and the section " I/O2: Toggle Bit II" explains the algorithm. See also the " I/O6: Toggle Bit I" subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The I/O2 vs. I/O6 figure shows the differences between I/O2 and I/O6 in graphical form.

Reading Toggle Bits I/O6, I/O2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read I/O7 - I/O0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on I/O7 - I/O0 on the following read cycle.
However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of I/O5 is high (see the section on I/O5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as I/O5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.
The remaining scenario is that the system initially determines that the toggle bit is toggling and I/O5 has not gone high. The system may continue to monitor the toggle bit and I/O5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

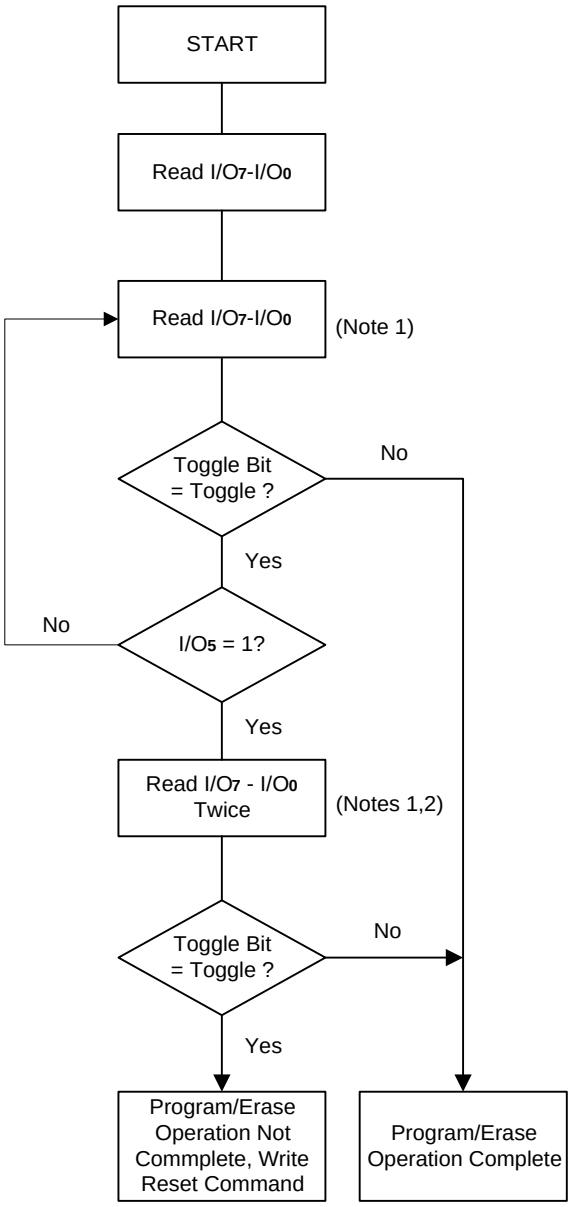
I/O5: Exceeded Timing Limits

I/O5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions I/O5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

The I/O_5 failure condition may appear if the system tries to program a "1 "to a location that is previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, I/O_5 produces a "1."
Under both these conditions, the system must issue the reset command to return the device to reading array data.

I/O_3: Sector Erase Timer

After writing a sector erase command sequence, the system may read I/O_3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, I/O_3 switches from "0" to "1." The system may ignore I/O_3 if the system can guarantee that the time between additional sector erase commands will always be less than 50μs. See also the "Sector Erase Command Sequence" section.
After the sector erase command sequence is written, the system should read the status on I/O_7 ($\overline{\text{Data}}$ Polling) or I/O_6 (Toggle Bit 1) to ensure the device has accepted the command sequence, and then read I/O_3. If I/O_3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If I/O_3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of I/O_3 prior to and following each subsequent sector erase command. If I/O_3 is high on the second status check, the last command might not have been accepted. Table 10 shows the outputs for I/O_3.



Notes :
1. Read toggle bit twice to determine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as I/O_5 changes to "1". See text.

Figure 6. Toggle Bit Algorithm

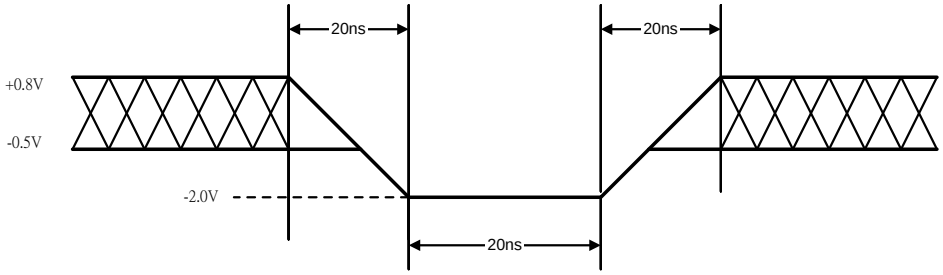
Table 12. Write Operation Status

Operation		I/O7 (Note 1)	I/O6	I/O5 (Note 2)	I/O3	I/O2 (Note 1)	RY/$\overline{BY}$
Standard Mode	Embedded Program Algorithm	$\overline{I/O_7}$	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspend Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	$\overline{I/O_7}$	Toggle	0	N/A	N/A	0

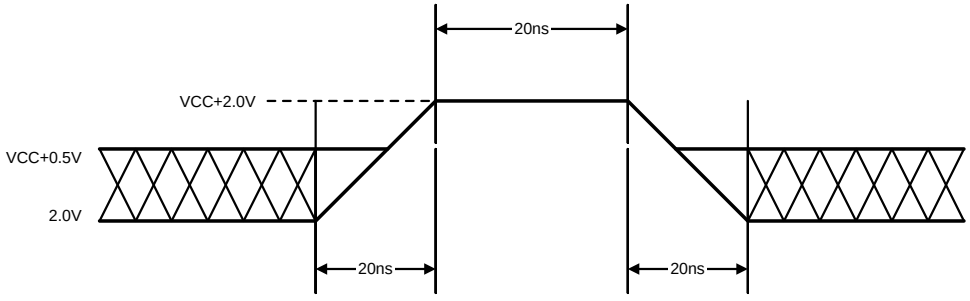
Notes:

1. I/O7 and I/O2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. I/O5 switches to “1” when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See “I/O5: Exceeded Timing Limits” for more information.

Maximum Negative Input Overshoot



Maximum Positive Input Overshoot



DC Characteristics

CMOS Compatible

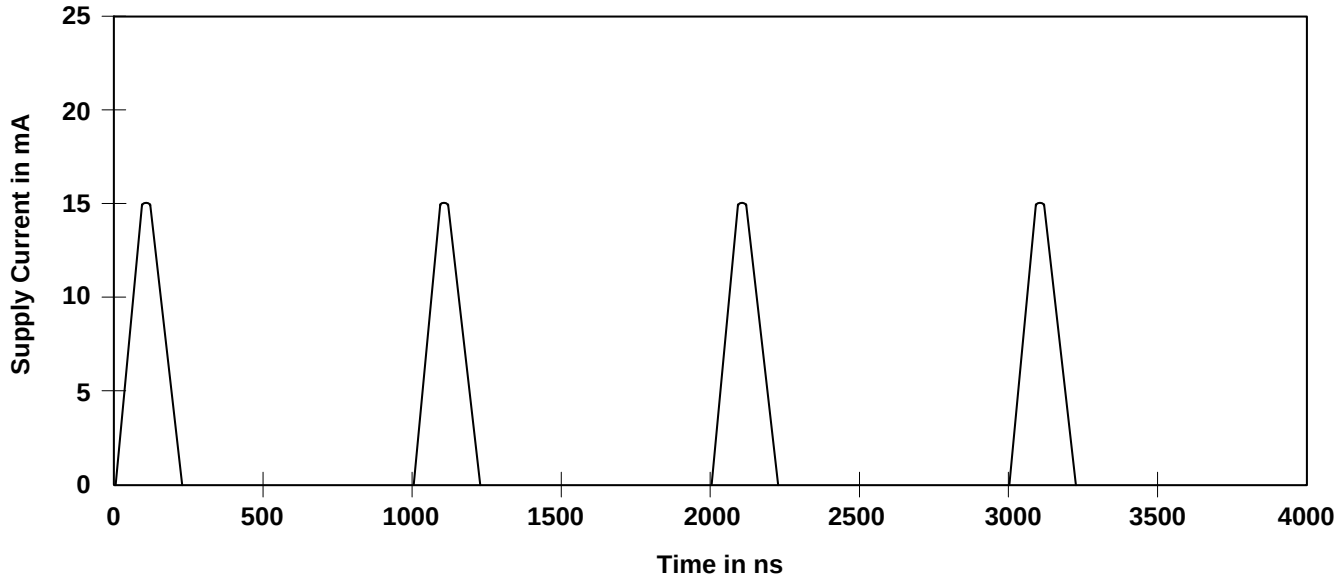
Parameter Symbol	Parameter Description	Test Description		Min.	Typ.	Max.	Unit
I_{LI}	Input Load Current	V_{IN} = VSS to VCC. VCC = VCC Max				±1.0	μA
I_{LIT}	A9 Input Load Current	VCC = VCC Max, A9 =12.5V				35	μA
I_{LO}	Output Leakage Current	V_{OUT} = VSS to VCC. VCC = VCC Max				±1.0	μA
I_{CC1}	VCC Active Read Current (Notes 1, 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} Byte Mode	5 MHz		10	16	mA
			1 MHz		2	4	
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} Word Mode	5 MHz		10	16	
			1 MHz		2	4	
I_{CC2}	VCC Active Write (Program/Erase) Current (Notes 2, 3, 4)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ =V_{IH}			20	30	Ma
I_{CC3}	VCC Standby Current (Note 2)	$\overline{CE}$ = $\overline{RESET}$= VCC ± 0.3V			1	5	μA
I_{CC4}	VCC Standby Current During Reset (Note 2)	$\overline{RESET}$= VSS ± 0.3V			1	5	μA
I_{CC5}	Automatic Sleep Mode (Note 2, 4, 5)	V_{IH} = VCC ± 0.3V; V_{IL} = VSS ± 0.3V			1	5	μA
V_{IL}	Input Low Level			-0.5		0.8	V
V_{IH}	Input High Level			0.7 x VCC		VCC + 0.3	V
V_{HH}	Voltage for $\overline{WP}$ /ACC Sector Protect/ Unprotect and Program Acceleration	VCC=3.0V ± 10%		9		10.5	V
V_{ID}	Voltage for Autoselect and Temporary Unprotect Sector	VCC = 3.0 V ± 10%		9		10.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0mA, VCC = VCC Min				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, VCC = VCC Min		0.85 x VCC			V
V_{OH2}		I_{OH} = -100 μA, VCC = VCC Min		VCC - 0.4			V

Notes:

1. The I_{CC} current listed is typically less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}. Typical VCC is 3.3V.
2. Maximum I_{CC} specifications are tested with VCC = VCC max. If $\overline{WP}$ is connected to ground, the I_{CC3} typical spec. would be 5uA.
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns. Typical sleep mode current is 1μA.
5. Not 100% tested.

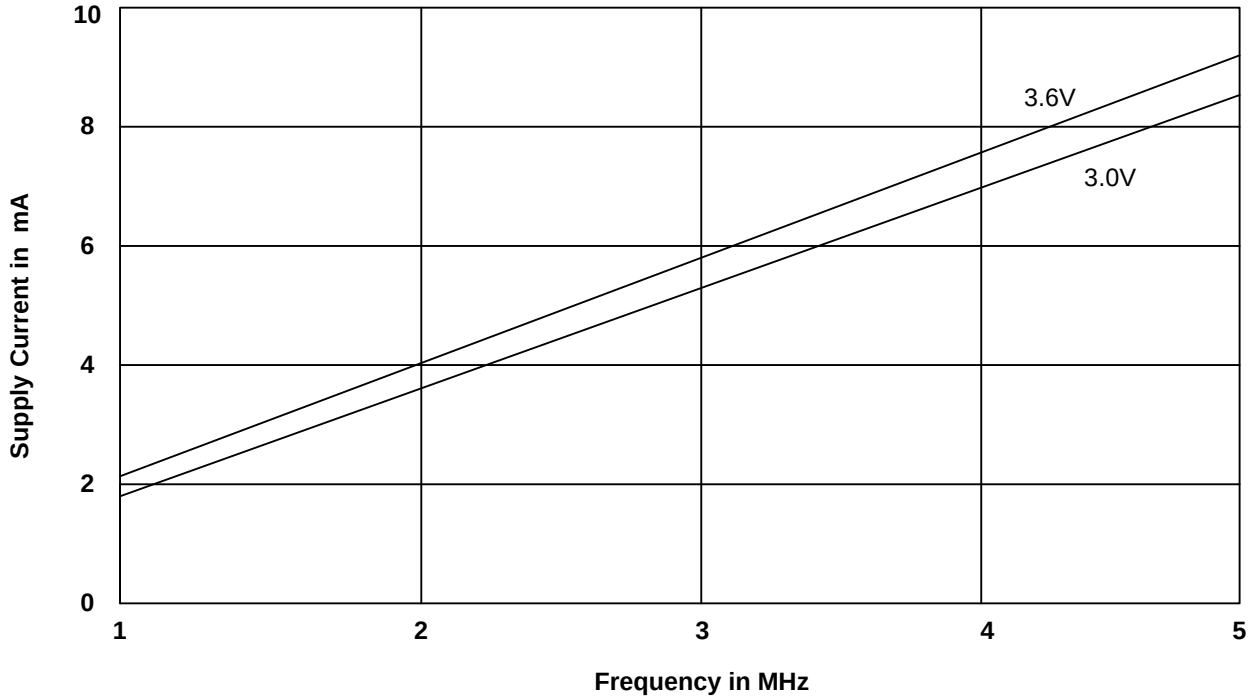
DC Characteristics (continued)

Zero Power Flash



Note: Addresses are switching at 1MHz

I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note : T = 25°C

Typical I_{CC1} vs. Frequency

AC Characteristics

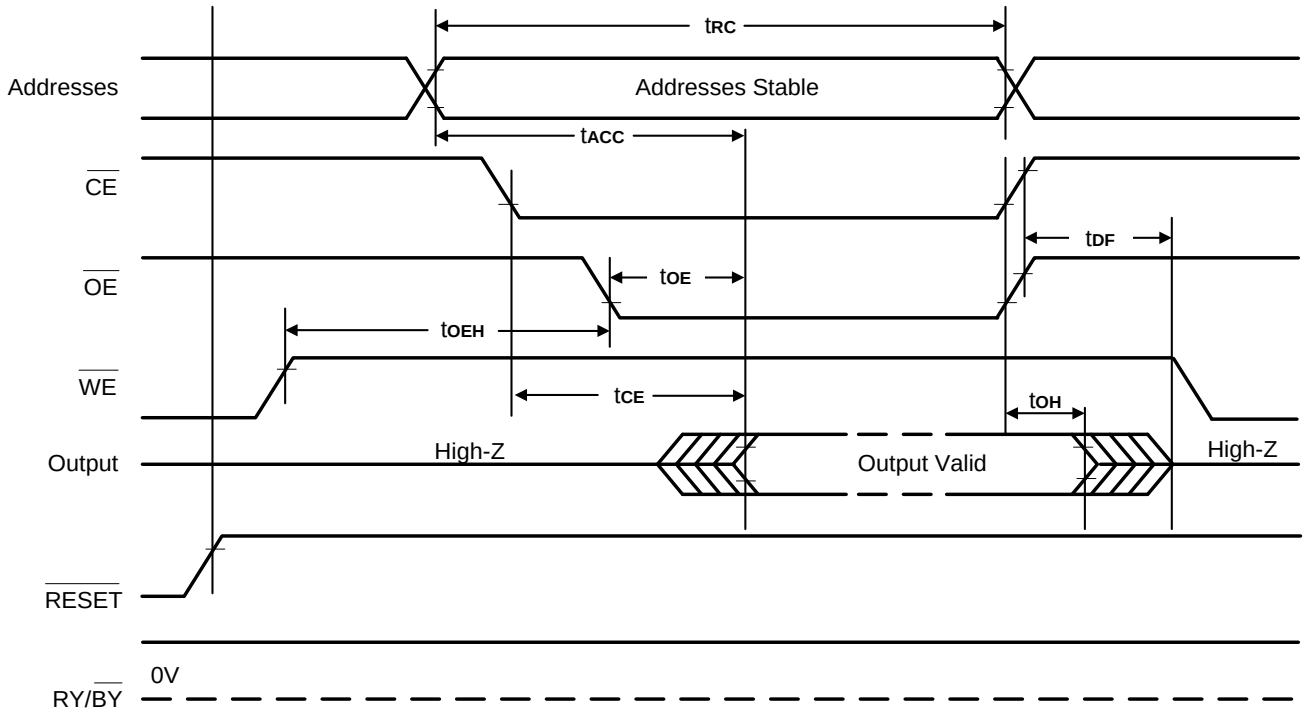
Read Only Operations

Parameter Symbols		Description		Test Setup		Speed	Unit
JEDEC	Std					-70	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min.	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$\overline{OE}$ = V_{IL}	Max.	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max.	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		0	0	ns
			Toggle and $\overline{Data}$ Polling		10	10	ns
t_{EHQZ}	t_{HZ}	Chip Enable to Output High Z (Notes 1)			Max.	16	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1)				16	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First (Note 1)			Min.	0	ns

Notes:

1. Not 100% tested.
2. See Test Conditions and Test Setup for test specifications.

Timing Waveforms for Read Only Operation



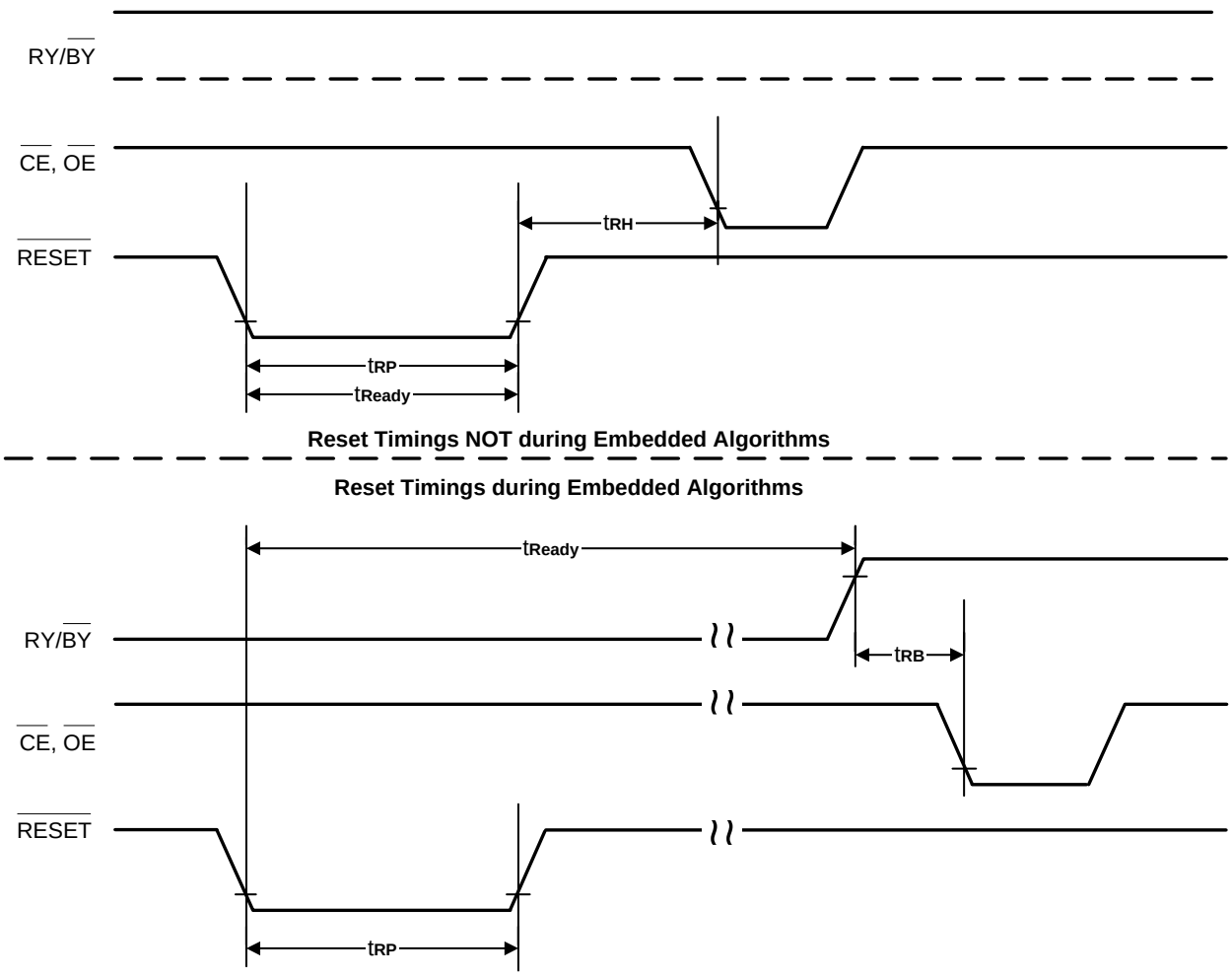
AC Characteristics

Hardware Reset ($\overline{RESET}$)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	μs
	t_{READY}	$\overline{RESET}$ Pin Low (Not During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	ns
	t_{RH}	$\overline{RESET}$ High Time Before Read (See Note)		Min	50	ns
	t_{RB}	RY/$\overline{BY}$ Recovery Time		Min	0	ns
	t_{RPD}	$\overline{RESET}$ Low to Standby Mode		Min	20	μs

Note: Not 100% tested.

$\overline{RESET}$ Timings

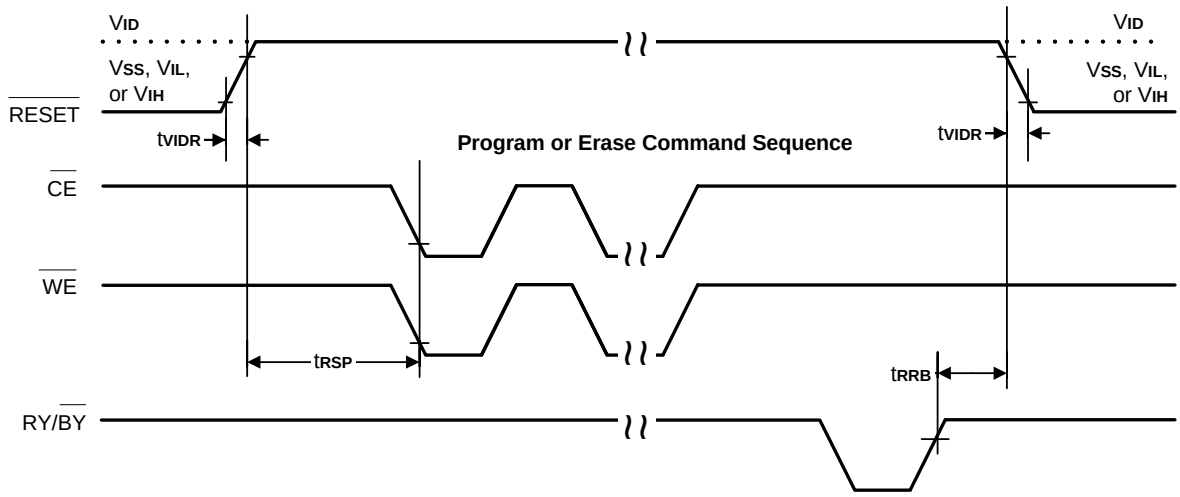


Temporary Sector Unprotect

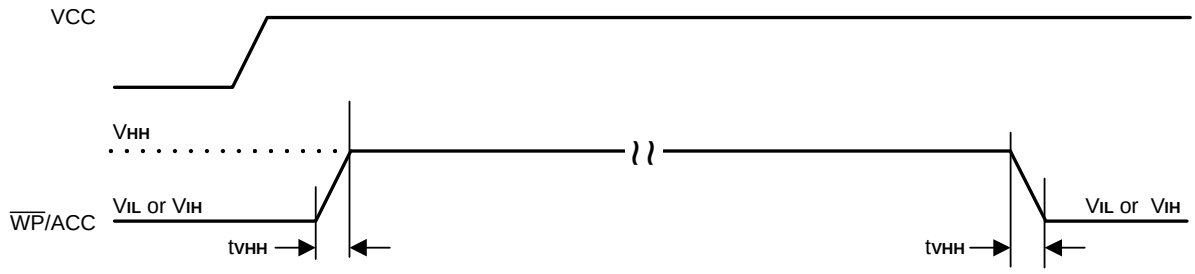
Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	$\overline{RESET}$ Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RRB}	$\overline{RESET}$ Hold Time from RY/$\overline{BY}$ High for Temporary Sector/Sector Block Unprotect	Min	4	µs

Note: Not 100% tested.

Temporary Sector Unprotect Timing Diagram



Accelerated Program Timing Diagram

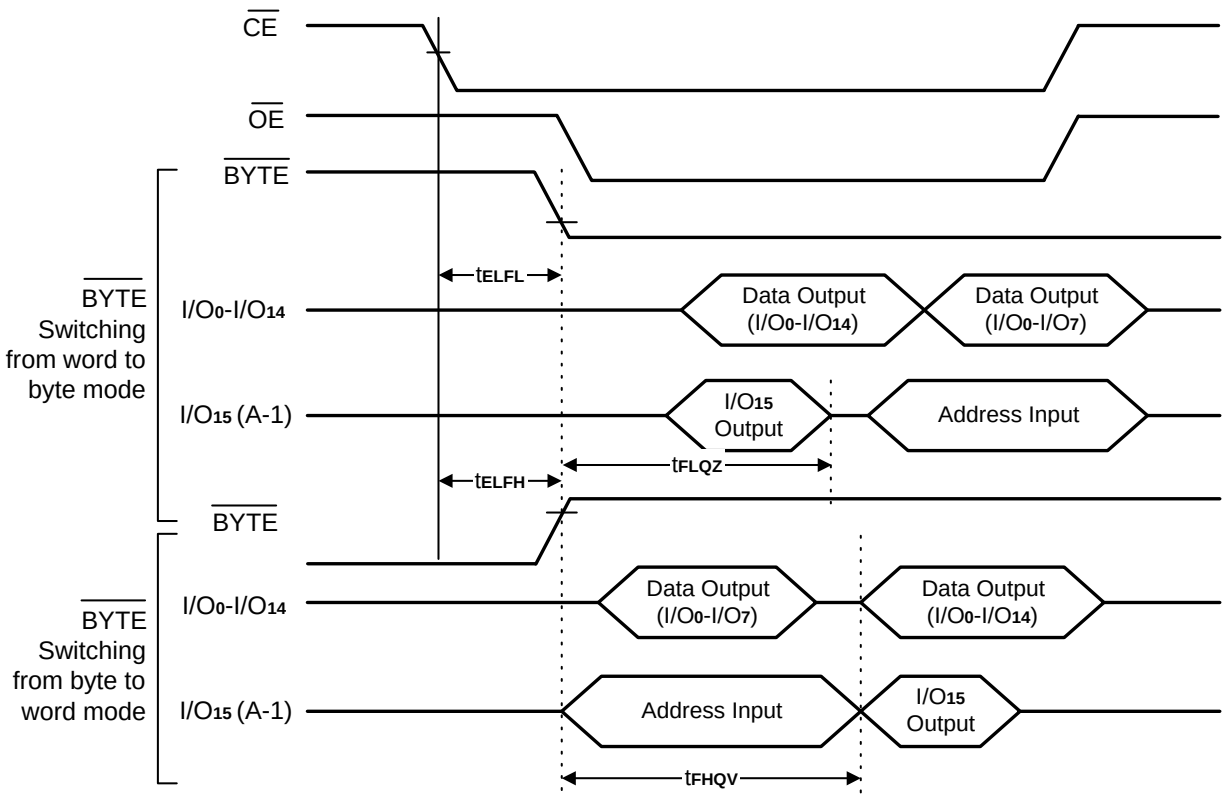


AC Characteristics

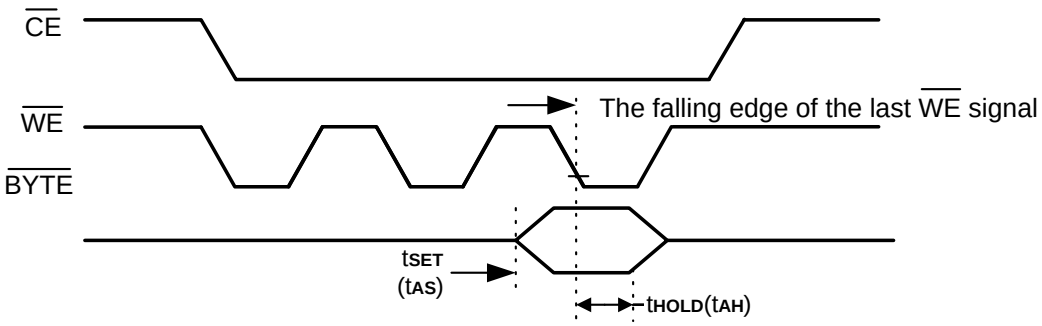
Word/Byte Configuration ($\overline{BYTE}$)

Parameter		Description		All Speed Options	Unit
JEDEC	Std			-70	
	t_{ELFL}/t_{ELFH}	$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	Max	5	ns
	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z	Max	25	ns
	t_{HQV}	$\overline{BYTE}$ Switching High to Output Active	Min	70	ns

$\overline{\text{BYTE}}$ Timings for Read Operations



$\overline{\text{BYTE}}$ Timings for Write Operations



Note:
Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

AC Characteristics

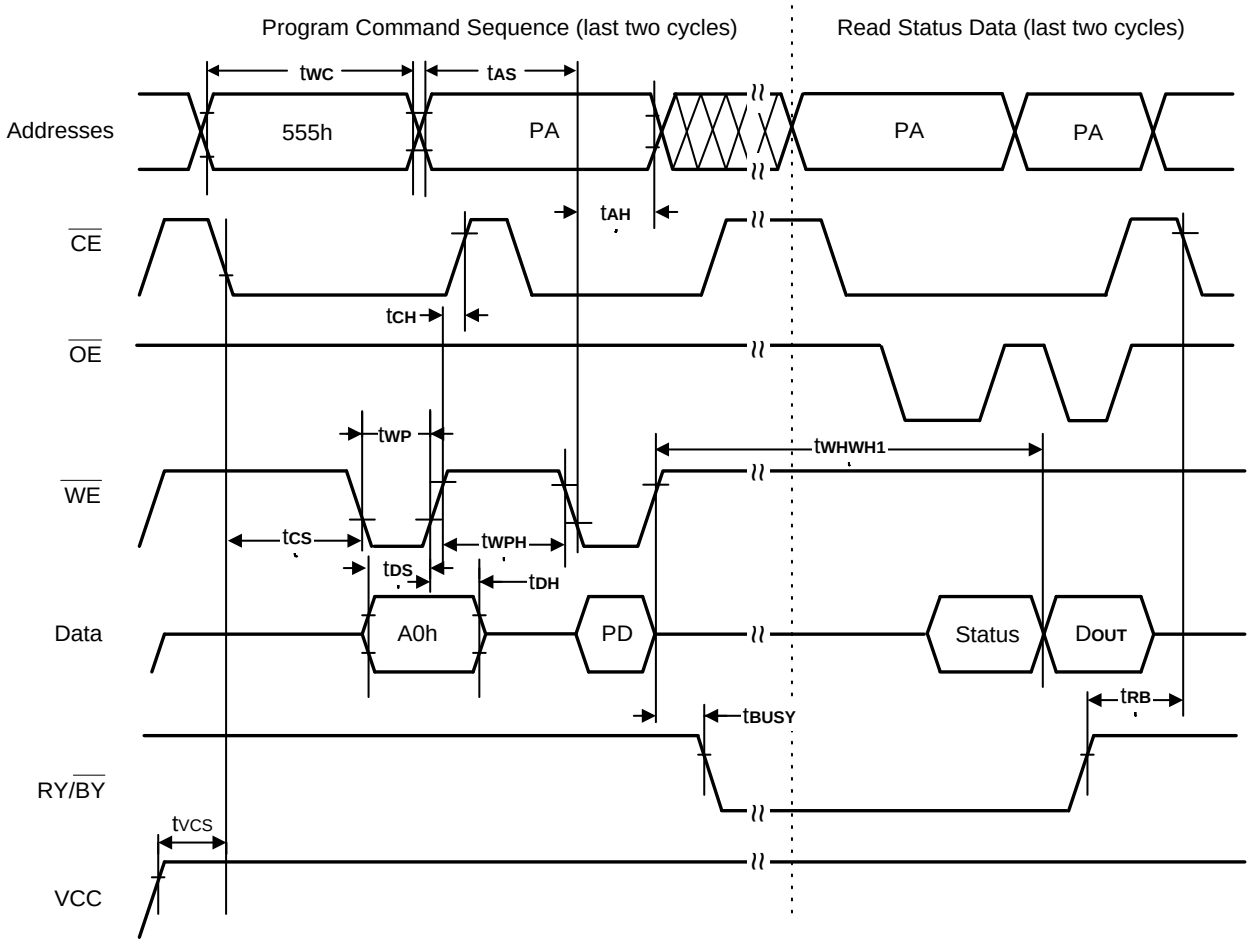
Erase and Program Operations

Parameter		Description			Speed	Unit
JEDEC	Std				-70	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min.	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	40	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	40	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	ns
	t_{OES}	Output Enable Setup Time		Min.	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ high to $\overline{WE}$ low)		Min.	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min.	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min.	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	30	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Byte	Typ.	6	µs
			Word	Typ.	9	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ.	0.7	sec
	t_{VCS}	VCC Set Up Time (Note 1)		Min.	50	µs
	t_{RB}	Recovery Time from RY/$\overline{BY}$ (Note 1)		Min	0	ns
	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay (Note 1)		Min	90	ns

Notes:

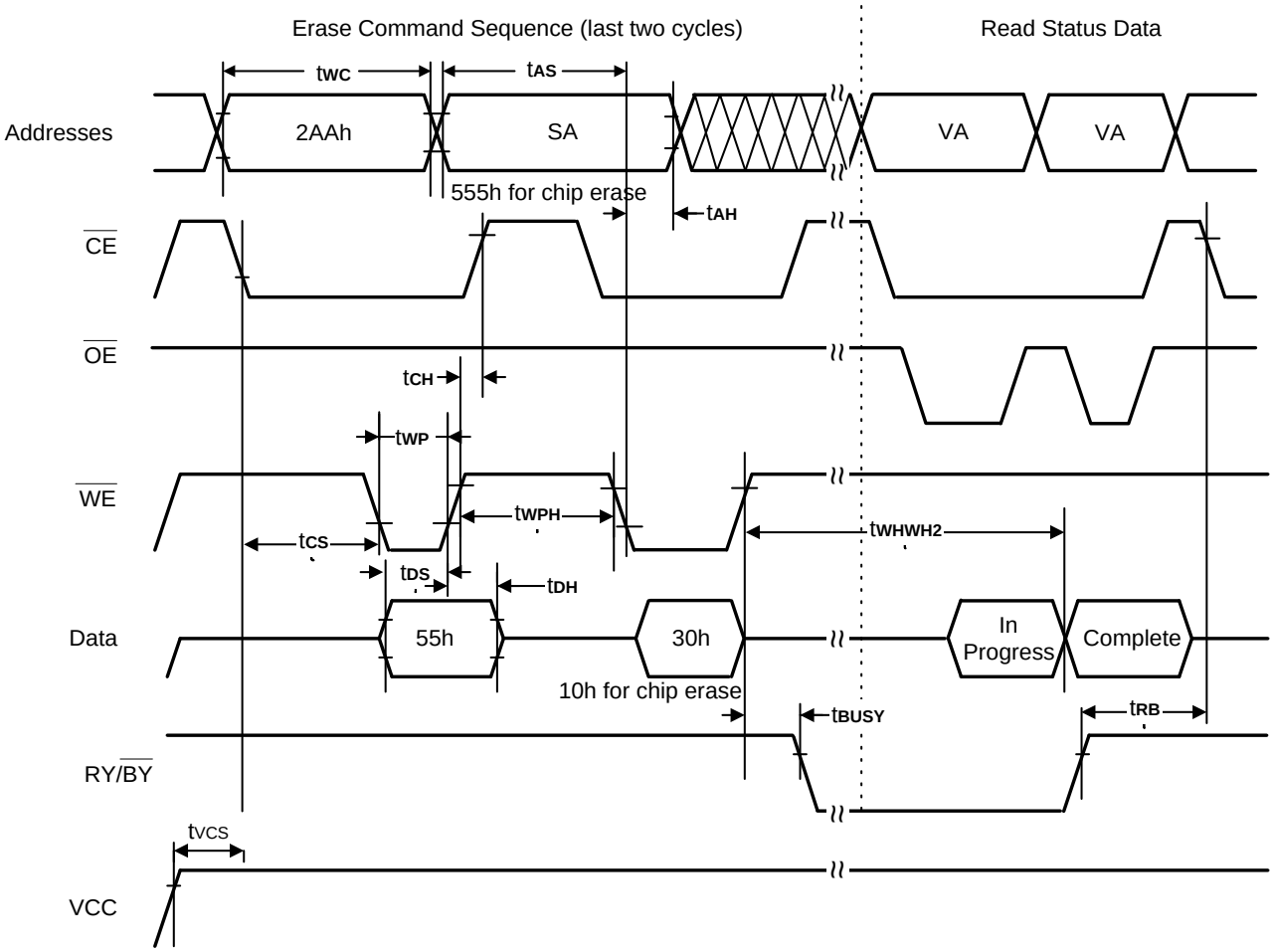
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Timing Waveforms for Program Operation



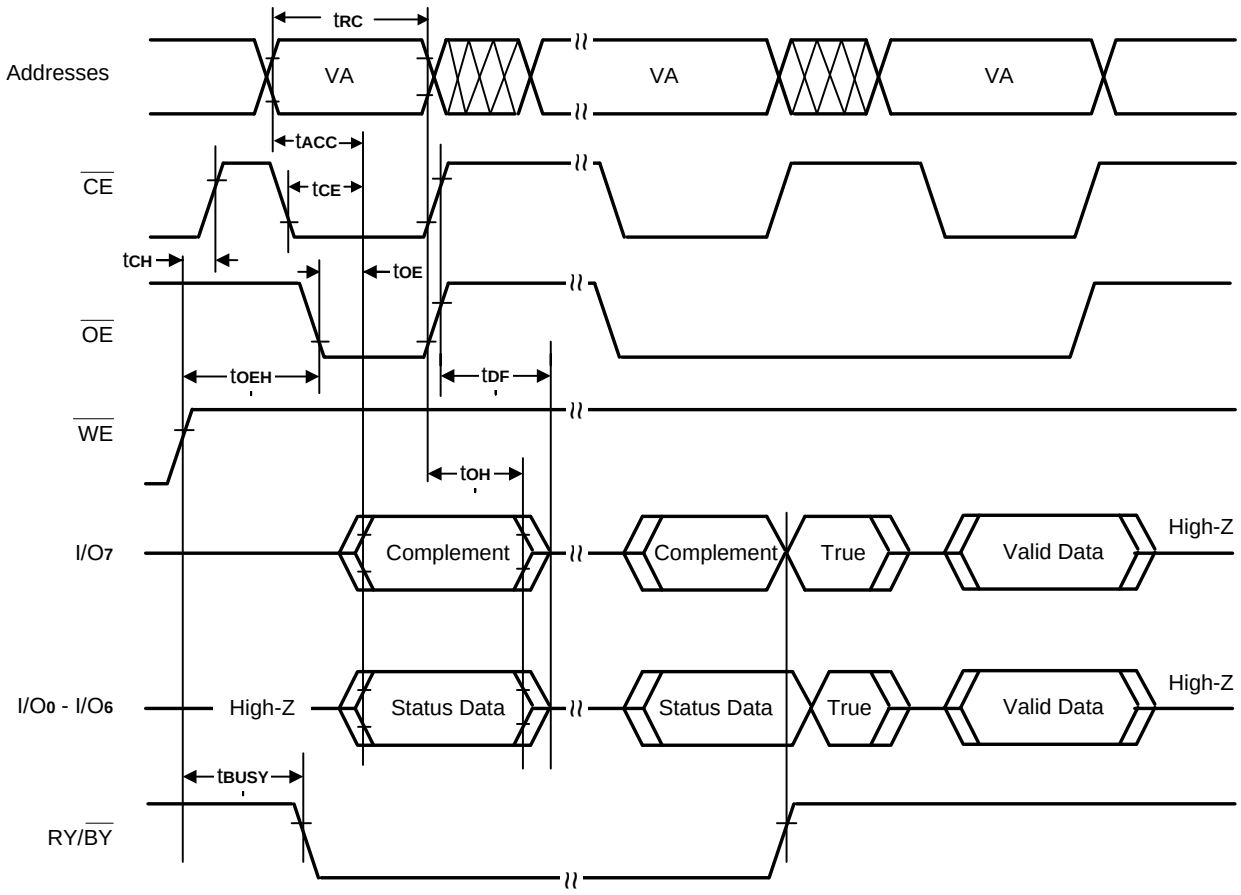
Note :
1. PA = program addrss, PD = program data, Dout is the true data at the program address.
2. Illustration shows device in word mode.

Timing Waveforms for Chip/Sector Erase Operation



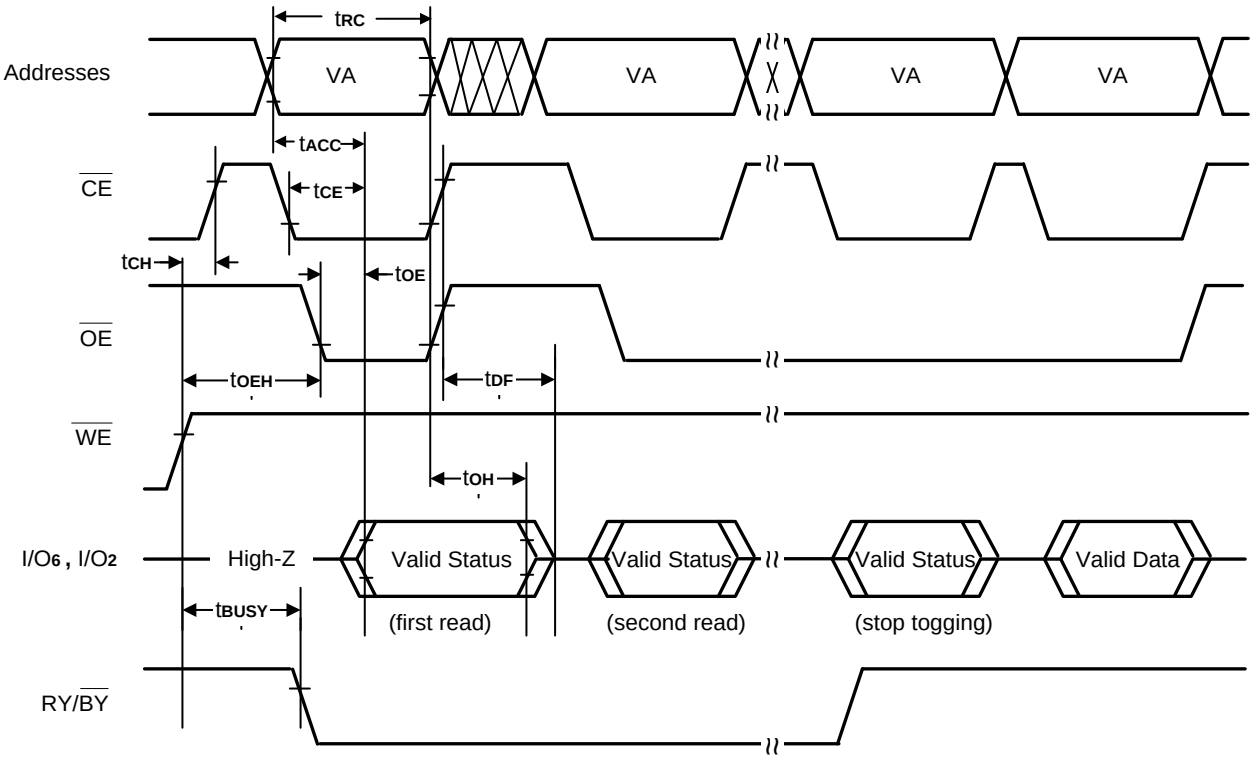
Note :
1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operaion Ststus").
2. Illustratin shows device in word mode.

Timing Waveforms for $\overline{\text{Data}}$ Polling (During Embedded Algorithms)



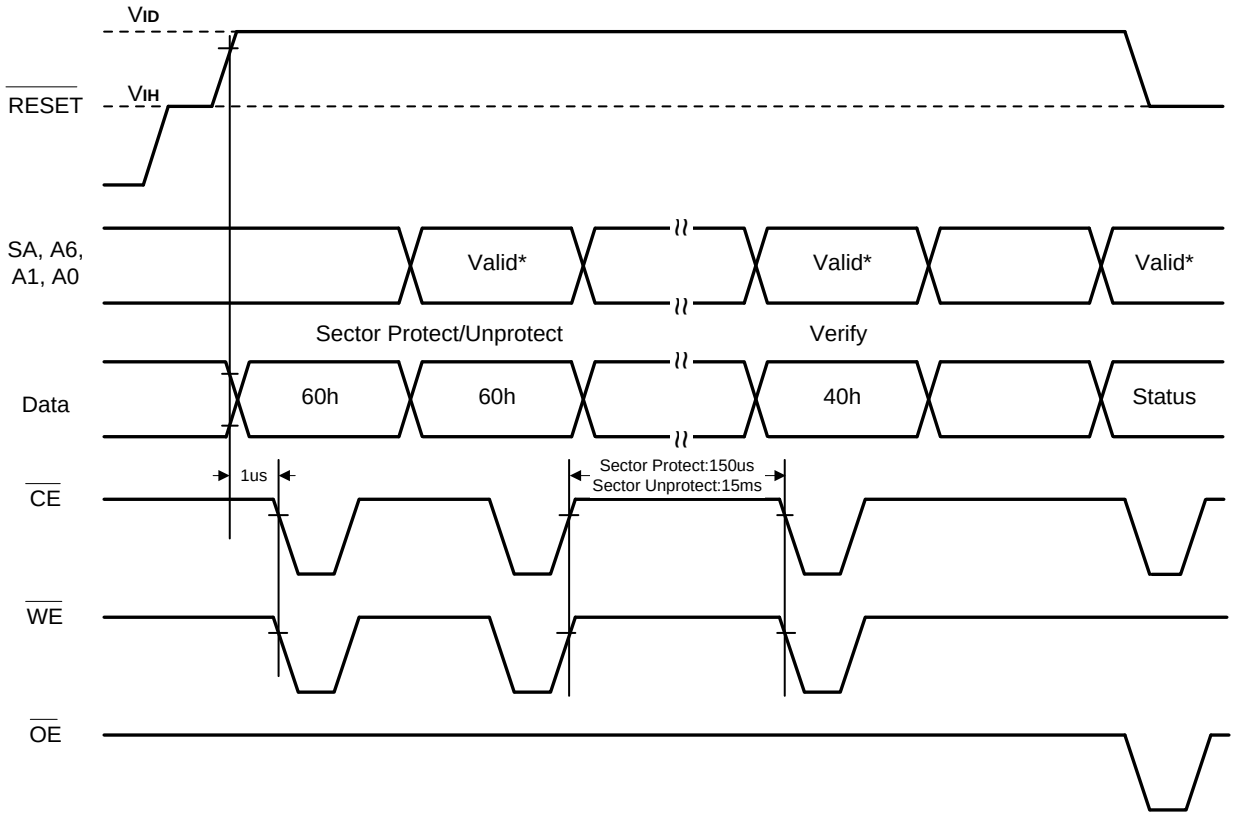
Note : VA = Valid Address. Illustation shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for Toggle Bit (During Embedded Algorithms)



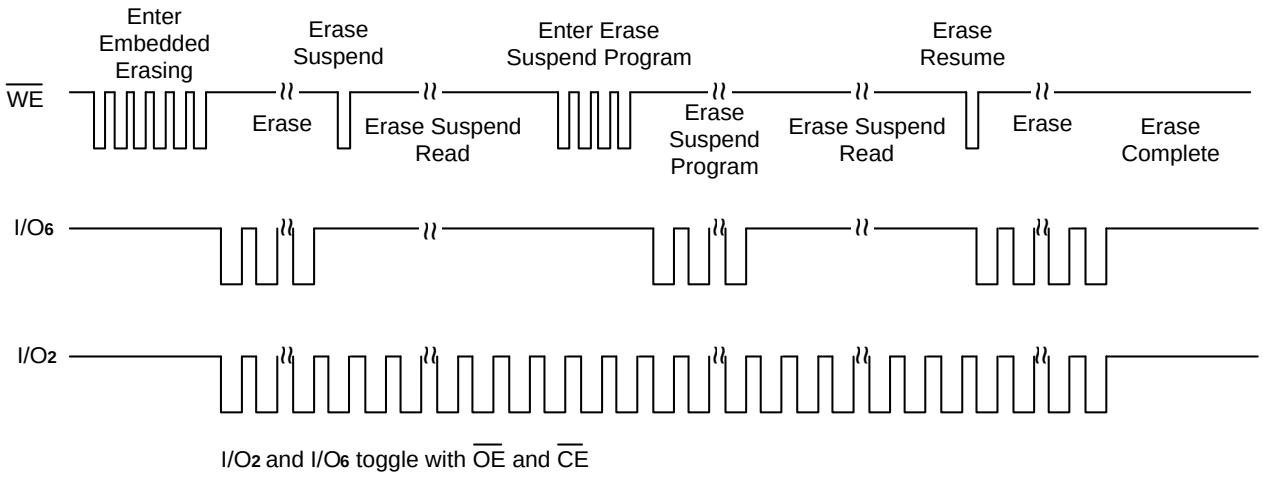
Note: VA = Valid Address; not required for I/O6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for Sector Protect/Unprotect



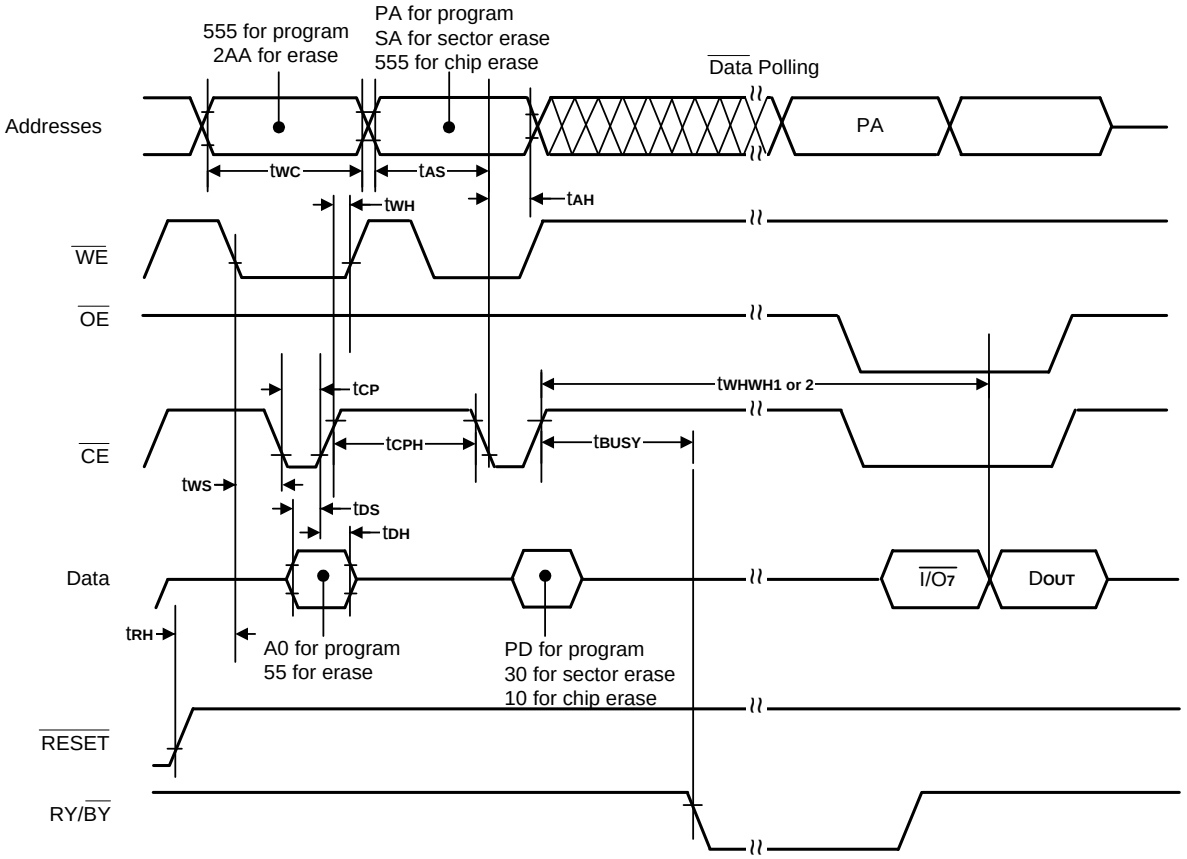
Note : For sector protect, A6=0, A1=1, A0=0. For sector unprotect, A6=1, A1=1, A0=0

Timing Waveforms for I/O2 vs. I/O6



Note : Both I/O6 and I/O2 toggle with $\overline{OE}$ or $\overline{CE}$. See the text on I/O6 and I/O2 in the section "Write Operation Status" for more information.

Timing Waveforms for Alternate $\overline{CE}$ Controlled Write Operation



Note :
1. PA = Program Address, PD = Program Data, SA = Sector Address, $\overline{I/O_7}$ = Complement of Data Input, D_{OUT} = Array Data.
2. Figure indicates the last two bus cycles of the command sequence.

Erase and Programming Performance

Parameter		Typ. (Note 1)	Unit	Comments
Sector Erase Time		0.7	sec	Excludes 00h programming prior to erasure
Chip Erase Time		45	sec	
Byte Programming Time		6	µs	Excludes system-level overhead (Note 4)
Word Programming Time		9	µs	
Chip Programming Time	Byte Mode	45	sec	
(Note 2)	Word Mode	40	sec	

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC, 10,000 cycles. Additionally, programming typically assumes checkerboard pattern..
2. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed. If the maximum byte program time given is exceeded, only then does the device set I/O_5 = 1. See the section on I/O_5 for further information.
3. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
4. System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 9 for further information on command definitions.
5. The device has a guaranteed minimum erase and program cycle endurance of 100,000 cycles.

Latch-up Characteristics

Description	Min.	Max.
Input Voltage with respect to VSS on all I/O pins	-1.0V	VCC+1.0V
VCC Current	-100 mA	+100 mA
Input voltage with respect to VSS on all pins except I/O pins (including A9, $\overline{OE}$ and $\overline{RESET}$)	-1.0V	12.5V

Includes all pins except VCC. Test conditions: VCC = 3.3V, one pin at time.

SOP/TSOP/TFBGA Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup		Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0	SOP/TSOP	6	7.5	pF
			TFBGA	4.2	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0	SOP/TSOP	8.5	12	pF
			TFBGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN}=0	SOP/TSOP	7.5	9	pF
			TFBGA	3.9	4.7	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0MHz

Data Retention

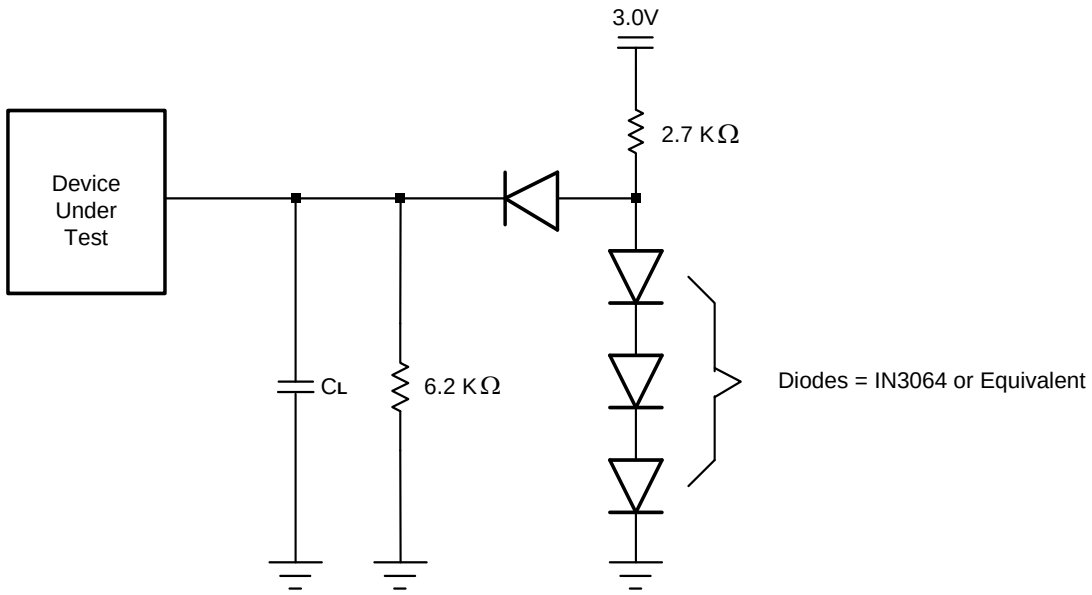
Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Test Conditions

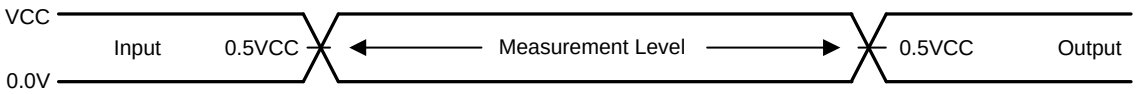
Test Specifications

Test Condition	-70	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L(including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0 – VCC	V
Input timing measurement reference levels	0.5VCC	V
Output timing measurement reference levels	0.5VCC	V

Test Setup



Input Waveforms and Measurement Levels



Ordering Information

Top Boot Sector Flash

Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A29L640TM-70F	70	10	20	0.5	44 Pin Pb-Free SOP
A29L640TM-70UF					44 Pin Pb-Free SOP
A29L640TM-70IF					44 Pin Pb-Free SOP
A29L640TV-70F	70	10	20	0.5	48 Pin Pb-Free TSOP
A29L640TV-70UF					48 Pin Pb-Free TSOP
A29L640TV-70IF					48 Pin Pb-Free TSOP
A29L640TG-70F	70	10	20	0.5	48 ball Pb-Free TFBGA
A29L640TG-70UF					48 ball Pb-Free TFBGA
A29L640TG-70IF					48 ball Pb-Free TFBGA

Note: -U is for industrial operating temperature range: -40°C to +85°C
-I is for industrial operating temperature range: -25°C to +85°C

Bottom Boot Sector Flash

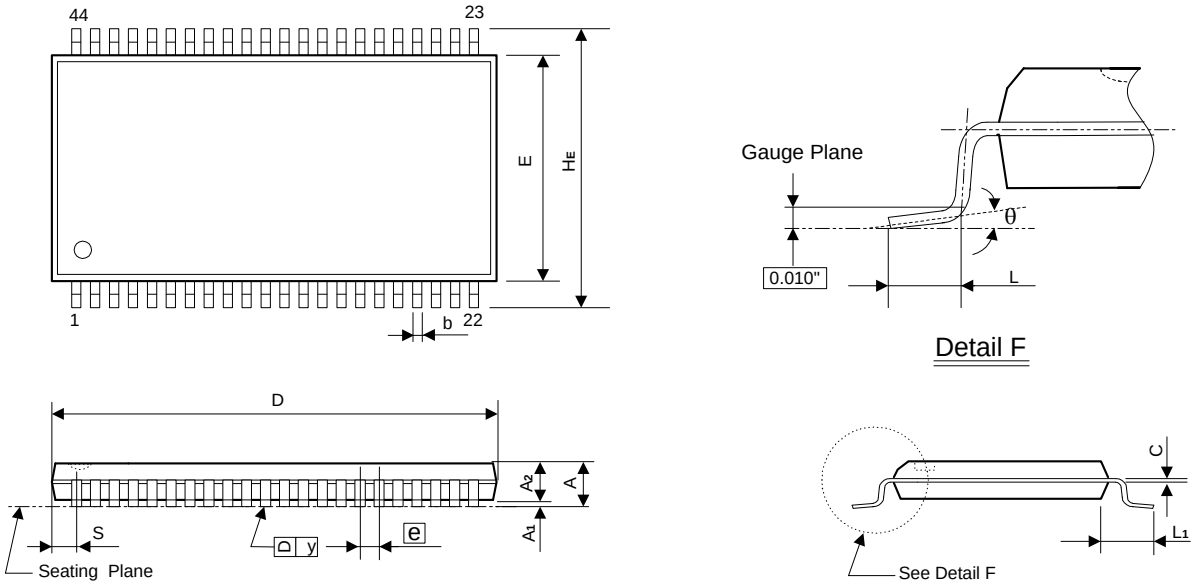
Part No.	Access Time (ns)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μA)	Package
A29L640UM-70F	70	10	20	0.5	44 Pin Pb-Free SOP
A29L640UM-70UF					44 Pin Pb-Free SOP
A29L640UM-70IF					44 Pin Pb-Free SOP
A29L640UV-70F	70	10	20	0.5	48 Pin Pb-Free TSOP
A29L640UV-70UF					48 Pin Pb-Free TSOP
A29L640UV-70IF					48 Pin Pb-Free TSOP
A29L640UG-70F	70	10	20	0.5	48 ball Pb-Free TFBGA
A29L640UG-70UF					48 ball Pb-Free TFBGA
A29L640UG-70IF					48 ball Pb-Free TFBGA

Note: -U is for industrial operating temperature range: -40°C to +85°C
-I is for industrial operating temperature range: -25°C to +85°C

Package Information

SOP 44L Outline Dimensions

unit: inches/mm



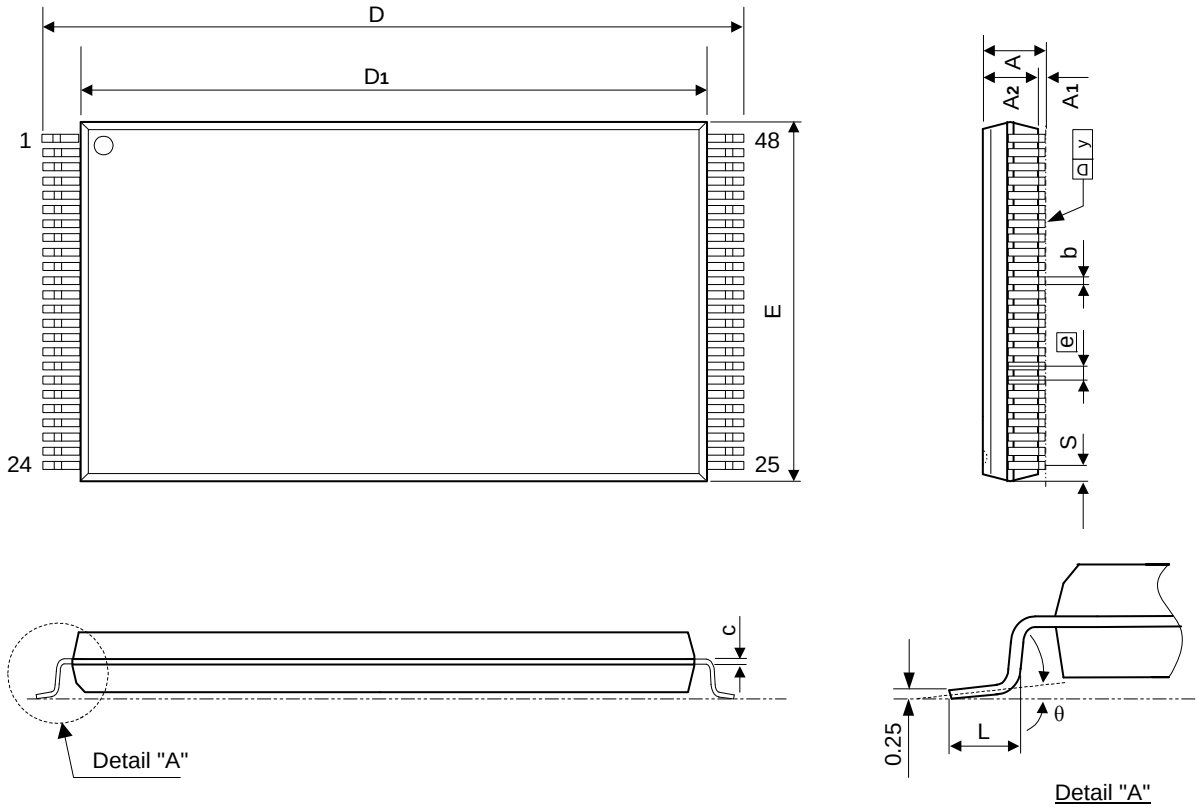
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A_1	0.004	-	-	0.10	-	-
A_2	0.103	0.106	0.109	2.62	2.69	2.77
b	0.013	0.016	0.020	0.33	0.40	0.50
C	0.007	0.008	0.010	0.18	0.20	0.25
D	-	1.122	1.130	-	28.50	28.70
E	0.490	0.496	0.500	12.45	12.60	12.70
e	-	0.050	-	-	1.27	-
H_E	0.620	0.631	0.643	15.75	16.03	16.33
L	0.024	0.032	0.040	0.61	0.80	1.02
L_1	-	0.0675	-	-	1.71	-
S	-	-	0.045	-	-	1.14
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

TSOP 48L (Type I) Outline Dimensions

unit: inches/mm



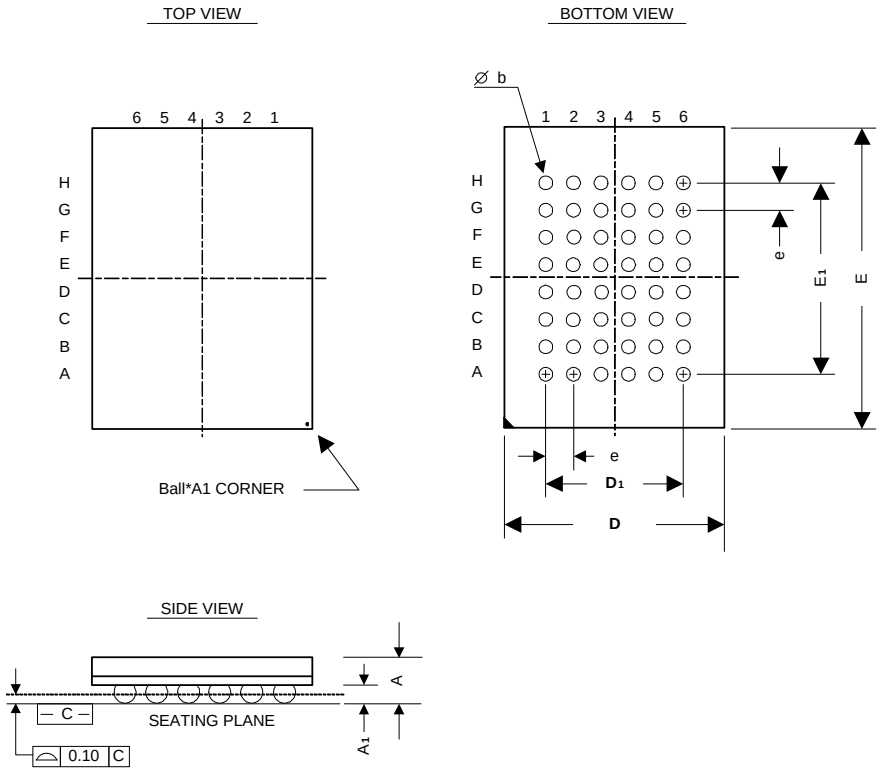
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.042	0.94	1.00	1.06
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.12	-	0.20
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.472	0.476	-	12.00	12.10
e	0.020 BASIC			0.50 BASIC		
L	0.016	0.020	0.024	0.40	0.50	0.60
S	0.011 Typ.			0.28 Typ.		
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

48LD CSP (6 x 8 mm) Outline Dimensions
(48TFBGA)

unit: mm



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	-	-	1.20
A_1	0.20	0.25	0.30
b	0.30	-	0.40
D	5.90	6.00	6.10
D_1	4.00 BSC		
e	-	0.80	-
E	7.90	8.00	8.10
E_1	5.60 BSC		