DRAM

1 MEG x 16 DRAM

3.3V FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single power supply: +3.3V ±0.3V
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and SELF
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 3mW standby; 225mW active, typical
- Optional SELF REFRESH mode, with Extended Refresh rate (8X)

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh Rate	
Standard and 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4LC1M16C3TG-7 S

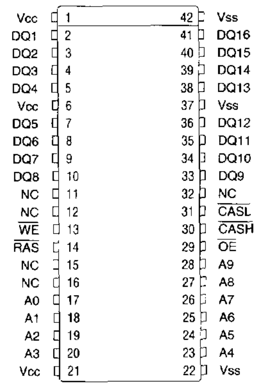
GENERAL DESCRIPTION

The MT4LC1M163(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The MT4LC1M16C3 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins ($\overline{CASL}$ and $\overline{CASH}$). These function in an identical manner to a single $\overline{CAS}$ of other DRAMs in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

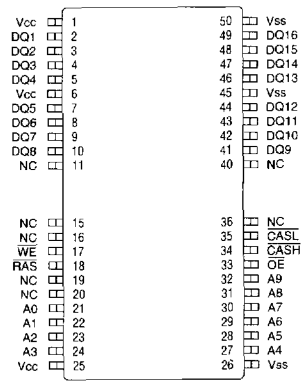
The MT4LC1M16C3 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last $\overline{CAS}$ to transition back HIGH. Use of only one of the two results in a BYTE access cycle. $\overline{CASL}$ transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

PIN ASSIGNMENT (Top View)

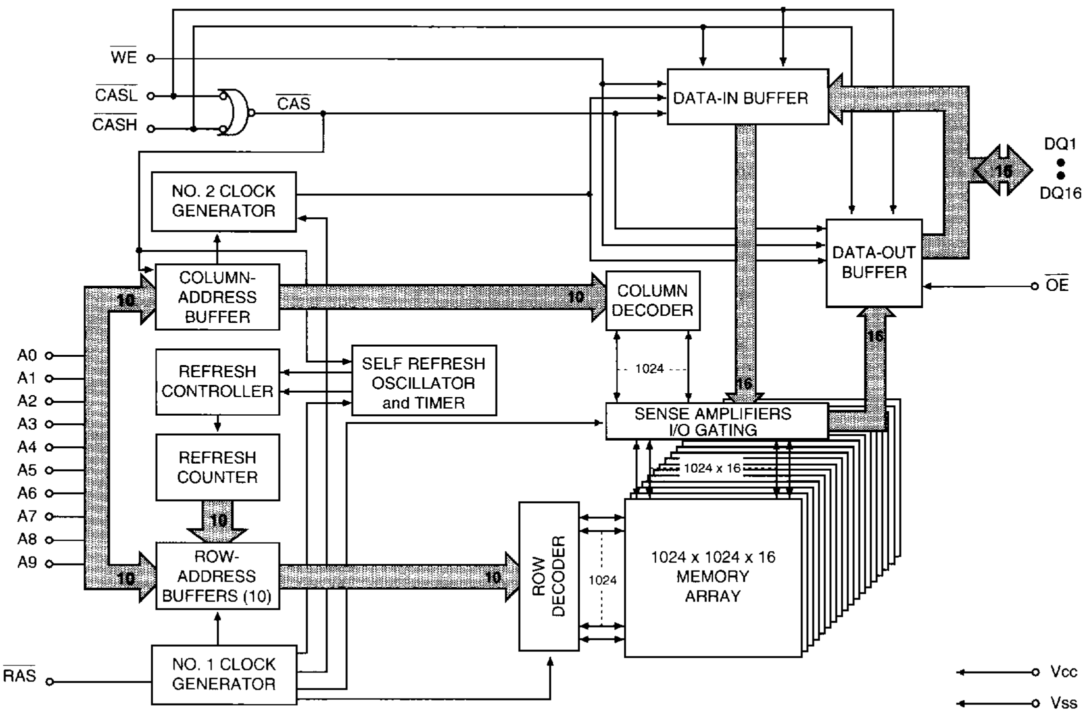
42-Pin SOJ (DC-7)



44/50-Pin TSOP (DD-6)



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered ten bits (A0-A9) at a time. RAS is used to latch the first ten bits and CAS the latter ten bits. The CAS function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The CAS function also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input of other DRAMs. The key difference is each CAS input (CASL and CASH) controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16. The two CAS controls give the MT4C1M16C3 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS REFRESH cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on S-version), regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE access (DQ1-DQ8). Enabling CASH will select an upper BYTE access (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4C1M16C3 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS inputs. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

SELF REFRESH

SELF REFRESH is similar to CBR except that the DRAM provides its own internal clocking during SLEEP mode. Thus, an external clock is not required. This results in additional power savings and design ease. The DRAM's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding both RAS and CAS LOW for a specified period. The industry standard for this value is 100µs minimum (^{t}RASS). The DRAM will remain in the SELF REFRESH mode while RAS and CAS remain LOW. Once CAS has been held LOW for ^{t}CHD, CAS is no longer required to remain LOW and becomes a "don't care." CAS is a "don't care" until ^{t}CHS, at which time CAS must be either HIGH or LOW.

The SELF REFRESH mode is terminated by taking RAS HIGH for the time minimum of an operation cycle, ^{t}RPS. Once the SELF REFRESH mode has been terminated, it is recommended that the user perform a refresh of all rows within the time of the external refresh rate prior to active use of the DRAM. The external refresh rate is typically 125µs per row-address. Once this burst has been completed, the DRAM may be used in the functional mode with distributed refreshes, such as CBR or RAS ONLY.

The alternative approach when exiting SELF REFRESH mode is to utilize distributed refreshes once ^{t}RPS has been met, provided CBR REFRESH cycles are employed. The first CBR pulse should occur within the time of the external refresh rate prior to active use of the DRAM and must be executed within three external refresh rate periods. This will ensure maximum data integrity.

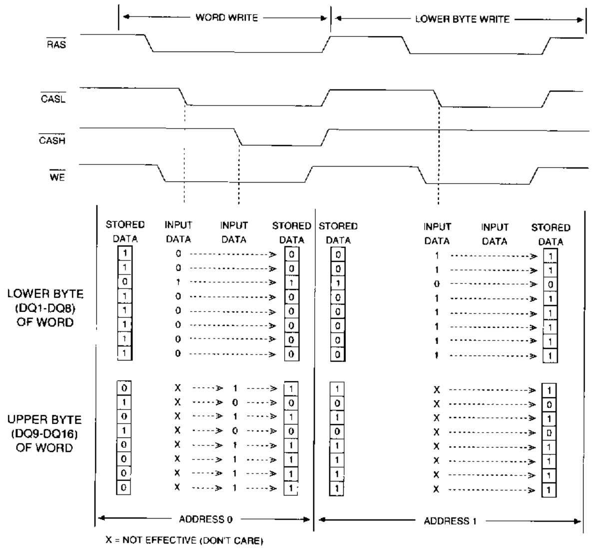


Figure 1
WORD AND BYTE WRITE EXAMPLE

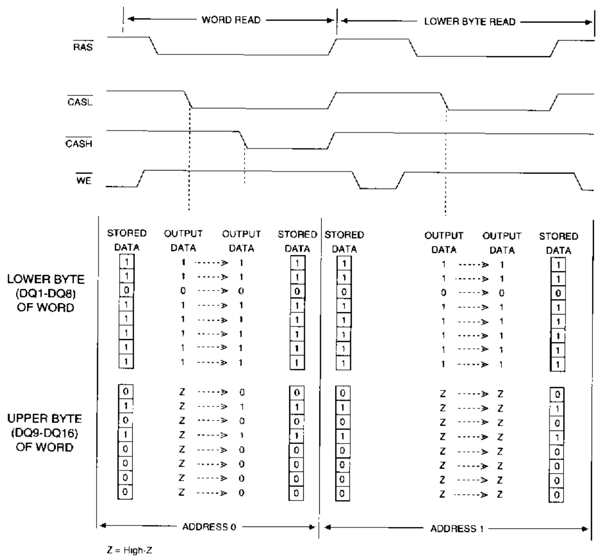


Figure 2
WORD AND BYTE READ EXAMPLE

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ${}^tR$	${}^tC$	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{RAS}$ ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4
SELF REFRESH		H→L	L	L	H	X	X	X	High-Z	

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. EARLY WRITE only.
4. Only one $\overline{CAS}$ must be active ($\overline{CASL}$ or $\overline{CASH}$).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS

(Notes: 1, 6, 7, 42) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.0mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2.0mA)	VOL		0.4	V	

ELECTRICAL CHARACTERISTICS AND DC OPERATING SPECIFICATIONS

(Notes: 1, 6, 7, 42) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	ICC3	150	140	130	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN]; ${}^tCP$, ${}^tASC$ = 10ns)	ICC4	80	70	60	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=VIH: ${}^tRC$ = ${}^tRC$ [MIN])	ICC5	150	140	130	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	ICC6	150	140	130	mA	3, 5
REFRESH CURRENT: Extended (S-only) Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ${}^tRAS$ (MIN); $\overline{WE}$, A0-A9 and DIN = Vcc - 0.2V (DIN may be left open); ${}^tRC$ = 125µs (1,024 rows at 125µs = 128ms)	ICC7	150	150	150	µA	3, 5
REFRESH CURRENT: SELF (S-only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ${}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	ICC8	150	150	150	µA	5, 27

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$,$\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	150		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 33
Output Enable	^tOE		15		15		15	ns	33
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	32
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	31
Column-address hold time	^tCAH	10		15		15		ns	31
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26, 32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	33, 30

NEW DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20, 30, 33
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21, 26, 31
Write command hold time	tWCH	10		15		15		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	26, 32
Data-in setup time	tDS	0		0		0		ns	22, 33
Data-in hold time	tDH	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	tAWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	40		45		45		ns	21, 31
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		16		16		16	ms	28
Refresh period - S option (1,024 cycles)	tREF		128		128		128	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	5		5		5		ns	5, 31
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	15		15		15		ns	5, 32
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		10		ns	26
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		10		ns	26
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Output disable	tOD	3	15	3	15	3	15	ns	29, 30, 41
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	15		15		15		ns	28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	tCLCH	10		10		10		ns	34
$\overline{RAS}$ pulse width during SELF REFRESH cycle	tRASS	100		100		100		µs	27
$\overline{RAS}$ precharge time during SELF REFRESH cycle	tRPS	110		130		150		ns	27
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	tCHD	15		15		15		ns	

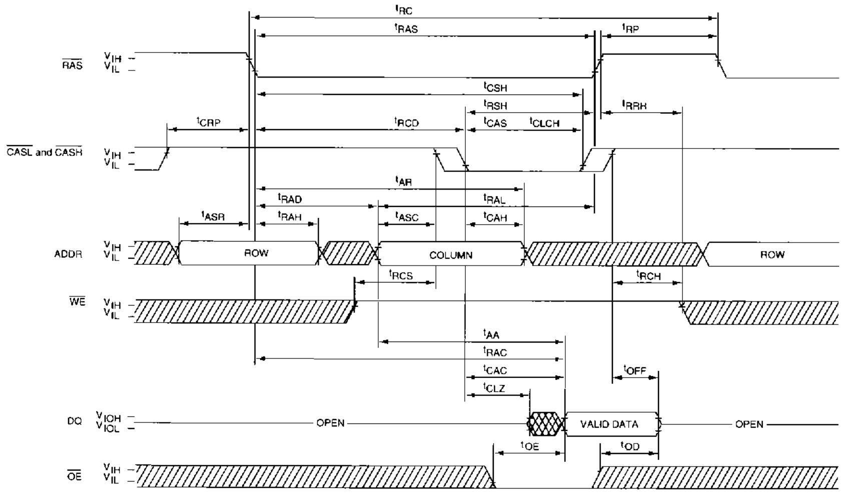
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V;f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate, 50pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at 0.2V or Vcc -0.2V.
26. Column-address changed once each cycle.
27. When exiting the SELF REFRESH mode, a complete set of row refreshes should be executed in order to ensure that the DRAM will be fully refreshed. Alternatively, distributed refreshes may be utilized, provided CBR refreshes are employed.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

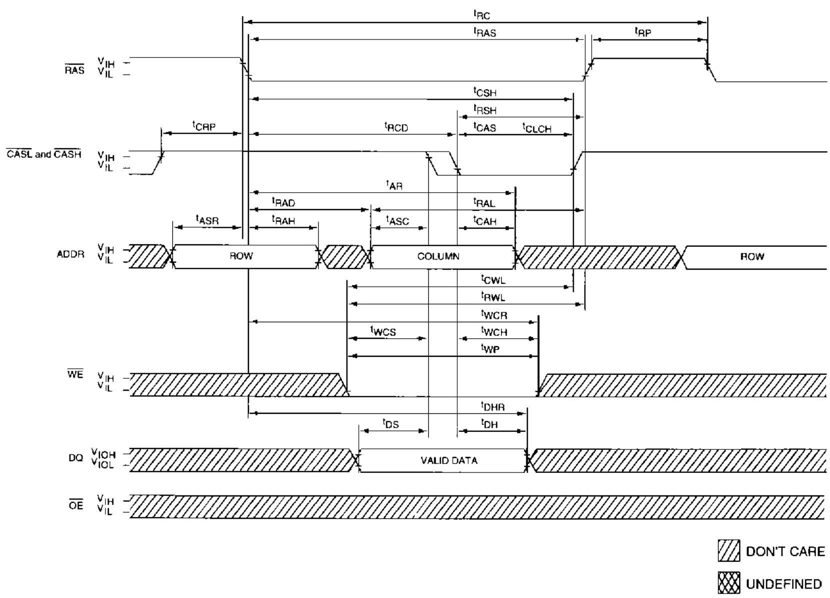
NOTES (continued)

30. The 3ns minimum is a parameter guaranteed by design.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.

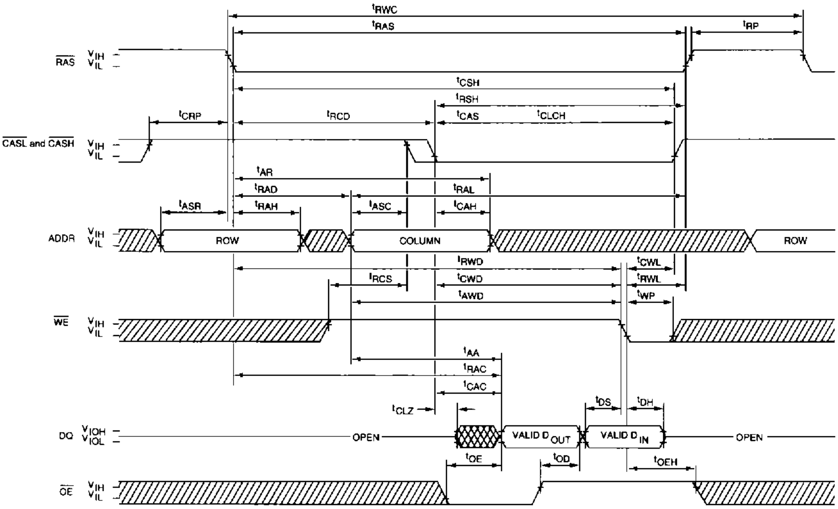
READ CYCLE



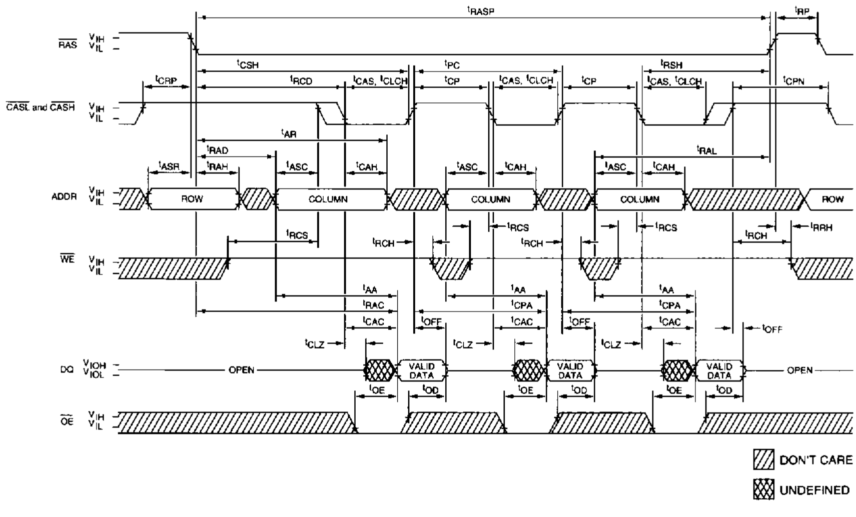
EARLY WRITE CYCLE



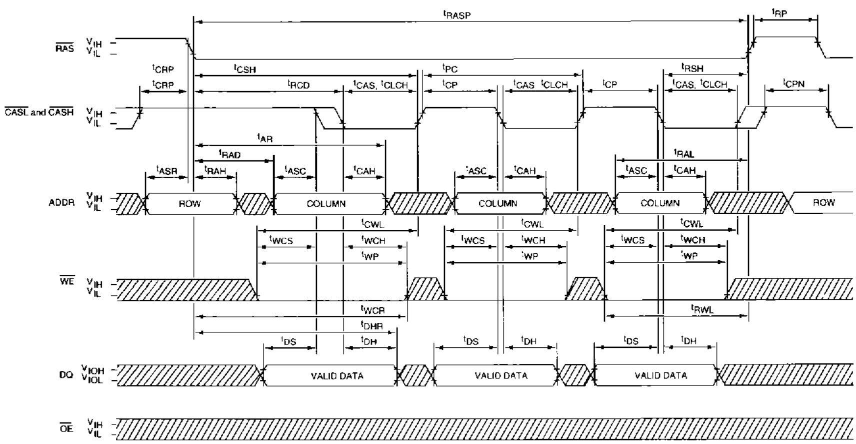
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



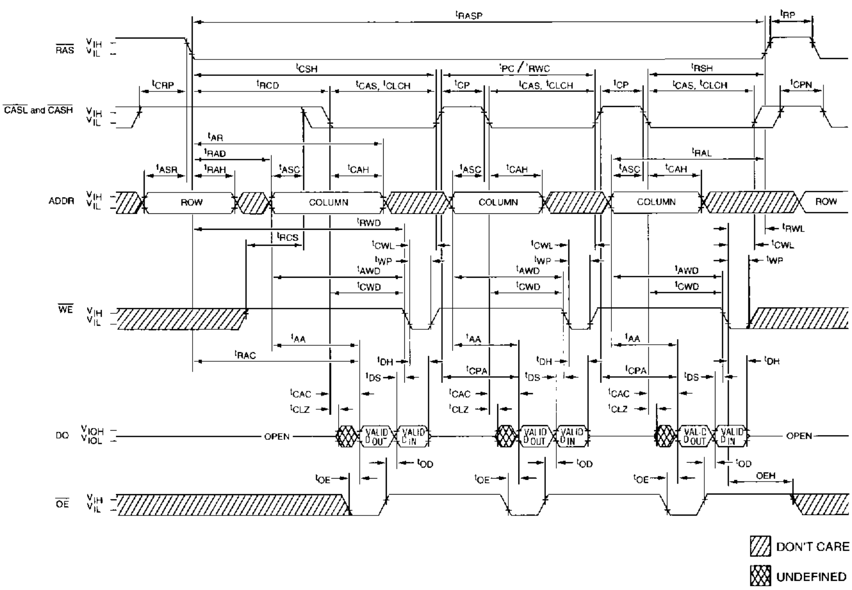
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

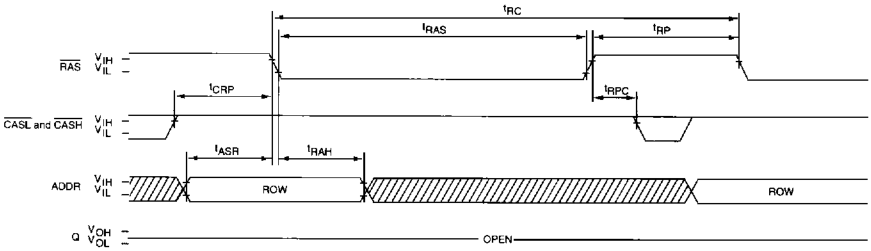


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



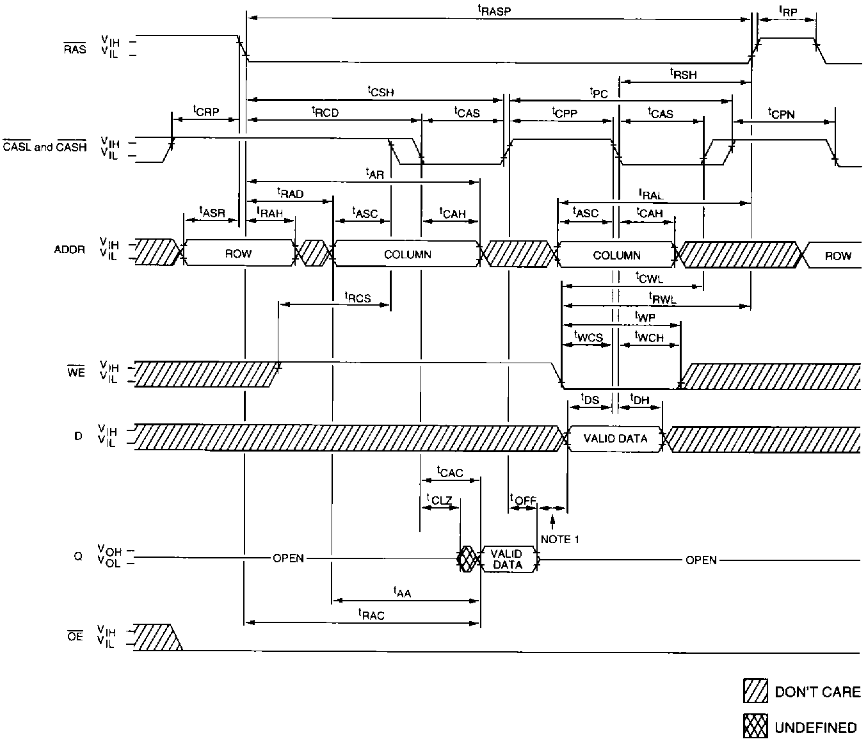
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

(ADDR = A0-A9, $\overline{\text{OE}}$; $\overline{\text{WE}}$ = DON'T CARE)



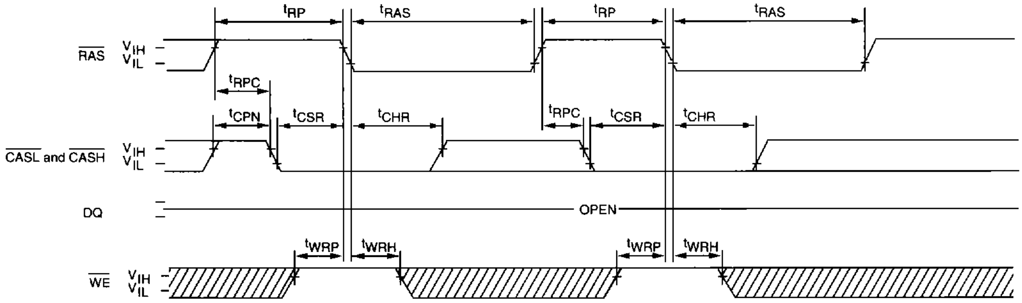
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)

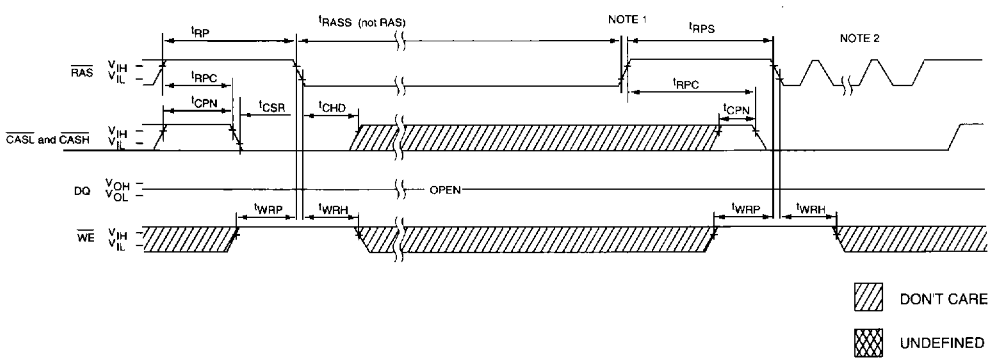


NOTE: 1. Do not drive data prior to High-Z; that is completion of ^{t}OFF. ^{t}CPP is equal to ^{t}OFF + ^{t}DS(MIN) + guardband between data-out and driving new data-in.

CBR REFRESH CYCLE
(A0-A9, $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A9, $\overline{OE}$ = DON'T CARE)



NOTE:
1. Once ^tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^tRPS is satisfied, a compete burst of all rows should be executed.

NEW DRAM

HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)