



**CYPRESS**

PRELIMINARY

**CY2272**

# Pentium™, 6x86, and K6 Clock Synthesizer/Driver for the Aladdin IV+ and 82430TX Chipsets for Portable PCs

## Features

- Mixed 2.5V and 3.3V operation
- Complete clock solution for Pentium™, Cyrix, and AMD processor-based motherboards
  - Four CPU clocks at 2.5V or 3.3V, up to 100 MHz
  - Six 3.3V SDRAM clocks, support three portable DIMMs, up to 100 MHz
  - Seven synchronous PCI clocks, one free-running, one early
  - One 3.3V 48 MHz USB clock
  - One 3.3V 24 MHz IO clock
  - Two high drive 3.3V Ref. clocks at 14.318 MHz
- 1 ns–4 ns delay between CPU and PCI clocks
- Three dedicated CPU frequency select inputs
- I<sup>2</sup>C™ Serial Configuration Interface
- Factory-EPROM programmable output drive and slew rate for optimal EMI control. Improved output drivers are designed for low EMI.
- Factory-EPROM programmable CPU clock frequencies for custom configurations
- Dedicated Power-down, CPU stop and PCI stop pins
- Low CPU clock jitter ≤ 250 ps cycle-cycle.
- Available in space-saving 48-pin SSOP package

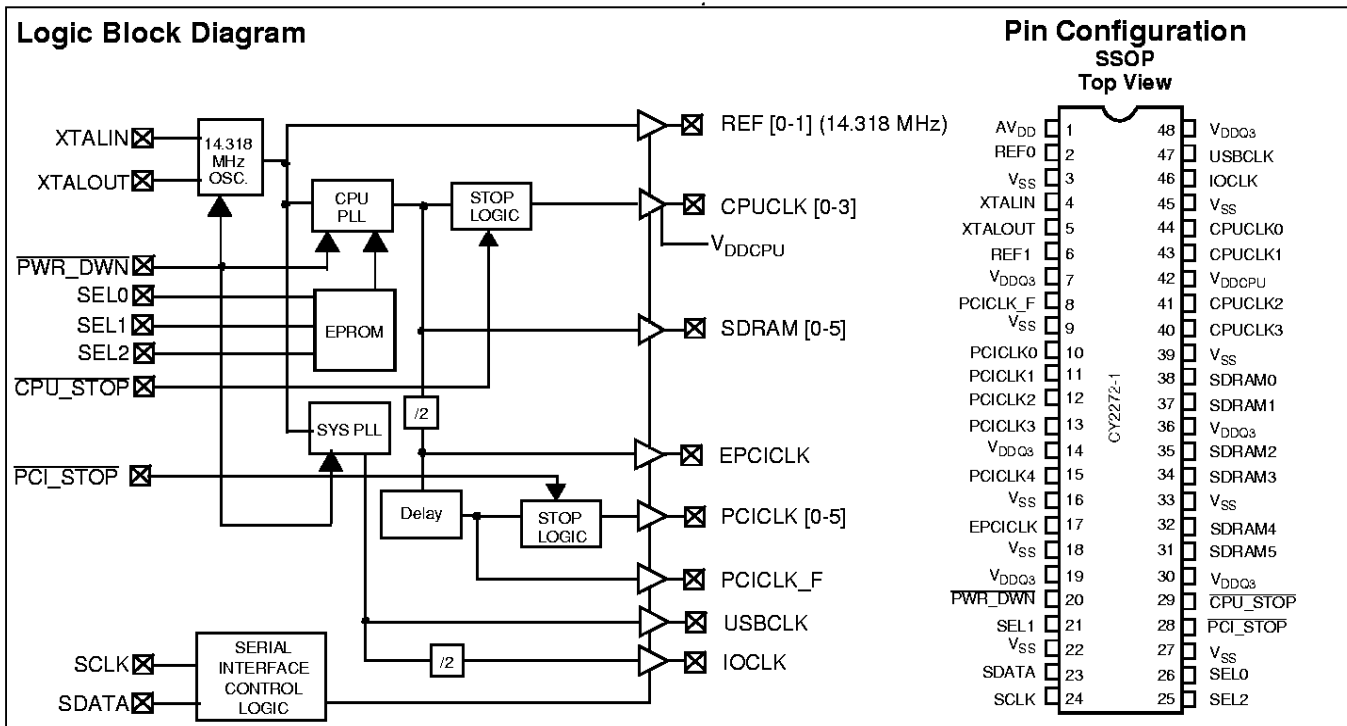
## Functional Description

The CY2272 is a clock synthesizer/driver for a Pentium, Cyrix, or AMD K6 processor-based portable PC using Intel's 82430TX, Aladdin IV+ or other similar chipsets.

The CY2272-1 outputs four CPU clocks at 2.5V or 3.3V. There are seven PCI clocks, running at one half the CPU clock frequency. One of the PCI clocks is free-running. Another leads the PCI clocks by 1 ns–4 ns. Additionally, the part outputs six 3.3V SDRAM clocks, one 3.3V USB clock at 48 MHz, one IO clock at 24 MHz, and two high-drive 3.3V reference clocks at 14.318 MHz. All output clocks meet Intel's and AMD's drive strength, rise/fall time, jitter, accuracy, and skew requirements.

The part possesses dedicated power-down, CPU stop, and PCI stop pins for power management control. When the CPU\_STOP input is asserted, the CPU clock outputs are driven LOW. When the PCI\_STOP input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the PWR\_DWN pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

The CY2272 clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2272 to have lower EMI than clock devices from other manufacturers. Additionally, factory-EPROM programmable output drive and slew-rate control enable optimal configurations.



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I<sup>2</sup>C is a trademark of Philips Corporation.



Pin Summary

Name	Pins (-1, -2)	Description
V <sub>DDQ3</sub>	7, 14, 19, 30, 36, 48	3.3V Digital voltage supply
V <sub>DDCPU</sub>	42	CPU Digital voltage supply, 2.5V or 3.3V
AV <sub>DD</sub>	1	Analog voltage supply, 3.3V
V <sub>SS</sub>	3, 9, 16, 18, 22, 27, 33, 39, 45	Ground
XTALIN <sup>[1]</sup>	4	Reference crystal input
XTALOUT <sup>[1]</sup>	5	Reference crystal feedback
PCI_STOP	28	Active LOW control input to stop PCI clocks (except free-running PCI clock)
CPU_STOP	29	Active LOW control input to stop CPU clocks
PWR_DWN	20	Active LOW control input to power down device
SDRAM[0-5]	38, 37, 35, 34, 32, 31	SDRAM clock outputs
SEL0	26	CPU frequency select input, bit 0 (See table below.)
SEL1	21	CPU frequency select input, bit 1 (See table below.)
SEL2	25	CPU frequency select input, bit 2 (See table below.)
CPUCLK[0:3]	44, 43, 41, 40	CPU clock outputs
PCICLK[0:4]	10, 11, 12, 13, 15	PCI clock outputs, at one-half the CPU frequency
PCICLK_F	8	Free-running PCI clock output
EPCICLK	17	Early PCI clock, leads PCI clocks by 1–4 ns
REF[0-1]	2, 6	3.3V Reference clock outputs, drive 45pF loads
USBCLK	47	USB Clock output (48 MHz)
IOCLK	46	IO Clock output (24 MHz)
SDATA	23	Serial data input for serial configuration port
SCLK	24	Serial clock input for serial configuration port

Function Table, EPROM Programmable<sup>[2]</sup>

I <sup>2</sup> C Bit 4	SEL0	SEL1	SEL2	CPU/PCI Ratio	CPUCLK[0:3] SDRAM[0:5]	PCICLK[0:4] PCICLK_F EPCICLK	REF[0-1]	USBCLK	IOCLK
0	0	0	0	2	15 MHz	7.5 MHz	14.318 MHz	48 MHz	24 MHz
0	0	0	1	2	16.67 MHz	8.33 MHz	14.318 MHz	48 MHz	24 MHz
0	0	1	0	2.5	18.75 MHz	7.5 MHz	14.318 MHz	48 MHz	24 MHz
0	0	1	1	2	13.75 MHz	6.875 MHz	14.318 MHz	48 MHz	24 MHz
0	1	0	0	2	60.0 MHz	30.0 MHz	14.318 MHz	48 MHz	24 MHz
0	1	0	1	2	66.67 MHz	33.33 MHz	14.318 MHz	48 MHz	24 MHz
0	1	1	0	2.5	75.0 MHz	30.0 MHz	14.318 MHz	48 MHz	24 MHz
0	1	1	1	2	55.0 MHz	27.5 MHz	14.318 MHz	48 MHz	24 MHz

Notes:

- For best accuracy, use a parallel-resonant crystal. C<sub>LOAD</sub> = 18 pF.
- CPU frequencies of 83.33 MHz and 100 MHz can also be supported. In this case, the CPU/PCI Divide ratio will be 2.5 and 3 respectively, thus enabling PCI clocks of 33.33 MHz. Please contact your local Cypress representative for more information.



**Actual Clock Frequency Values**

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	-195
CPUCLK	60.0	60.0	0
CPUCLK	75.0	75.0	0
USBCLK	48.0	48.008	167
IOCLK	24.0	24.004	167

**CPU and PCI Clock Driver Strengths**

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

**Power Management Logic**

CPU_STOP	PCI_STOP	PWR_DWN	CPUCLK	PCICLK EPCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Stopped	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	CPU PLL / 2	Running	Running	Running	Running
1	0	1	As per Func. Tbl.	Low	Running	Running	Running	Running
1	1	1	As per Func. Tbl.	As per Func. Tbl.	Running	Running	Running	Running

**Serial Configuration Map**

- The Serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0".
- I<sup>2</sup>C Address for the CY2273 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

**Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)**

Bit	Pin #	Description										
Bit 7	--	(Reserved) drive to '0'										
Bit 6	--	(Reserved) drive to '0'										
Bit 5	--	(Reserved) drive to '0'										
Bit 4	--	Frequency Select (Refer to Freq. Sel. Table)										
Bit 3	--	(Reserved) drive to '0'										
Bit 2	--	(Reserved) drive to '0'										
Bit 1 Bit 0	--	<table border="1"> <thead> <tr> <th>Bit 1</th> <th>Bit 0</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1 - Three-State</td> </tr> <tr> <td>1</td> <td>0 - N/A</td> </tr> <tr> <td>0</td> <td>1 - Testmode</td> </tr> <tr> <td>0</td> <td>0 - Normal Operation</td> </tr> </tbody> </table>	Bit 1	Bit 0	1	1 - Three-State	1	0 - N/A	0	1 - Testmode	0	0 - Normal Operation
Bit 1	Bit 0											
1	1 - Three-State											
1	0 - N/A											
0	1 - Testmode											
0	0 - Normal Operation											

**Select Functions based on Byte 0**

Functional Description	Outputs					
	CPU	PCI, PCI_F	SDRAM	Ref	USBCLK	IOCLK
Three-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode <sup>[4]</sup>	TCLK/2 <sup>[3]</sup>	TCLK/4	TCLK/2	TCLK	TCLK/2	TCLK/4

**Notes:**

3. TCLK supplied on the XTALIN pin in Test Mode.
4. Valid only for SEL2=1, SEL1=0, SEL0=1.



**Byte 1: CPU Active/Inactive Register**  
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	47	USBCLK (Active/Inactive)
Bit 6	46	IOCLK (Active/Inactive)
Bit 5	N/A	(Reserved) drive to '0'
Bit 4	N/A	Not used - drive to '0'
Bit 3	40	CPUCLK3 (Active/Inactive)
Bit 2	41	CPUCLK2 (Active/Inactive)
Bit 1	43	CPUCLK1 (Active/Inactive)
Bit 0	44	CPUCLK0 (Active/Inactive)

**Byte 2: PCI Active/Inactive Register**  
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	7	PCICLK_F (Active/Inactive)
Bit 5	15	EPCICLK (Active/Inactive)
Bit 4	14	PCICLK4 (Active/Inactive)
Bit 3	12	PCICLK3 (Active/Inactive)
Bit 2	11	PCICLK2 (Active/Inactive)
Bit 1	10	PCICLK1 (Active/Inactive)
Bit 0	8	PCICLK0 (Active/Inactive)

**Byte 3: SDRAM Active/Inactive Register**  
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	28	(Reserved) drive to '0'
Bit 6	29	(Reserved) drive to '0'
Bit 5	31	SDRAM5 (Active/Inactive)
Bit 4	32	SDRAM4 (Active/Inactive)
Bit 3	34	SDRAM3 (Active/Inactive)
Bit 2	35	SDRAM2 (Active/Inactive)
Bit 1	37	SDRAM1 (Active/Inactive)
Bit 0	38	SDRAM0 (Active/Inactive)

**Byte 4: SDRAM Active/Inactive Register**  
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	N/A	Not used - drive to '0'
Bit 6	N/A	Not used - drive to '0'
Bit 5	N/A	Not used - drive to '0'
Bit 4	N/A	Not used - drive to '0'
Bit 3	17	Not used - drive to '0'
Bit 2	18	Not used - drive to '0'
Bit 1	20	Not used - drive to '0'
Bit 0	21	Not used - drive to '0'

**Byte 5: Peripheral Active/Inactive Register**  
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	N/A	(Reserved) drive to '0'
Bit 6	N/A	(Reserved) drive to '0'
Bit 5	N/A	(Reserved) drive to '0'
Bit 4	N/A	(Reserved) drive to '0'
Bit 3	N/A	(Reserved) drive to '0'
Bit 2	N/A	(Reserved) drive to '0'
Bit 1	6	REF1 (Active/Inactive)
Bit 0	2	REF0 (Active/Inactive)

**Byte 6: Reserved, for future use**



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... -0.5 to +7.0V  
 Input Voltage ..... -0.5V to  $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C  
 Max. Soldering Temperature (10 sec) ..... +260°C  
 Junction Temperature ..... +150°C  
 Package Power Dissipation ..... 1W  
 Static Discharge Voltage ..... >2000V  
 (per MIL-STD-883, Method 3015)

**Operating Conditions<sup>[5]</sup>**

Parameter	Description	Min.	Max.	Unit
$AV_{DD}, V_{DDQ3}$	Analog and Digital Supply Voltage	3.135	3.465	V
$V_{DDCPU}$	CPU Supply Voltage	2.375 3.135	2.9 3.465	V
$T_A$	Operating Temperature, Ambient	0	70	°C
$C_L$	Max. Capacitive Load on CPUCLK, USBCLK, IOCLK EPCICK, PCICK SDRAM REF [0,1]	10 30 20 20	20 30 30 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
$V_{IH}$	High-level Input Voltage	Except Crystal Inputs	2.0		V
$V_{IL}$	Low-level Input Voltage	Except Crystal Inputs		0.8	V
$V_{OH}$	High-level Output Voltage	$V_{DDCPU} = V_{DDQ2} = 2.375V$ $I_{OH} = 16\text{ mA}$ CPUCLK	2.0		V
$V_{OL}$	Low-level Output Voltage	$V_{DDCPU} = V_{DDQ2} = 2.375V$ $I_{OL} = 27\text{ mA}$ CPUCLK		0.4	V
$V_{OH}$	High-level Output Voltage	$V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V$ $I_{OH} = 16\text{ mA}$ CPUCLK $I_{OH} = 36\text{ mA}$ SDRAM $I_{OH} = 32\text{ mA}$ PCICK $I_{OH} = 26\text{ mA}$ USBCLK IOCLK $I_{OH} = 36\text{ mA}$ REF[0-1]	2.4		V
$V_{OL}$	Low-level Output Voltage	$V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V$ $I_{OL} = 27\text{ mA}$ CPUCLK $I_{OL} = 29\text{ mA}$ SDRAM $I_{OL} = 26\text{ mA}$ PCICK $I_{OL} = 21\text{ mA}$ USBCLK IOCLK $I_{OL} = 29\text{ mA}$ REF[0-1]		0.4	V
$I_{IH}$	Input High Current	$V_{IH} = V_{DD}$	-10	+10	μA
$I_{IL}$	Input Low Current	$V_{IL} = 0V$		10	μA
$I_{OZ}$	Output Leakage Current	Three-state	-10	+10	μA
$I_{DD}$	Power Supply Current <sup>[6]</sup>	$V_{DD} = 3.465V, V_{IN} = 0$ or $V_{DD}$ , Loaded Outputs, CPU clocks = 66.67 MHz		300	mA
$I_{DD}$	Power Supply Current <sup>[6]</sup>	$V_{DD} = 3.465V, V_{IN} = 0$ or $V_{DD}$ , Unloaded Outputs		120	mA
$I_{DDS}$	Power-down Current	Current draw in power-down state		50	μA

**Notes:**

- Electrical parameters are guaranteed with these operating conditions.
- Power supply current will vary with number of outputs which are running. Therefore, power supply current can be calculated with the following formula: TBD



Switching Characteristics<sup>[7]</sup>

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	All	Output Duty Cycle <sup>[8]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>2</sub>	CPUCLK	CPU Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	1.0		4.0	V/ns
t <sub>2</sub>	PCICLK, EPCICLK, REF[0-1]	PCI, EPCI, REF Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t <sub>2</sub>	SDRAM	SDRAM Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t <sub>3</sub>	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V <sub>DDCPU</sub> = 2.5V Between 0.4V and 2.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		1.6 2.0	ns
t <sub>4</sub>	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V <sub>DDCPU</sub> = 2.5V Between 2.4V and 0.4V, V <sub>DDCPU</sub> = 3.3V	0.4 0.5		1.6 2.0	ns
t <sub>5</sub>	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V <sub>DDCPU</sub> = 2.5V Measured at 1.5V, V <sub>DDCPU</sub> = 3.3V		100	250	ps
t <sub>6</sub>	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.0	4.0	ns
t <sub>7</sub>	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			500	ps
t <sub>8</sub>	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			250	ps
t <sub>9</sub>	EPCICLK, PCICLK	EPCI-PCI Clock Skew	Measured at 1.5V for 3.3V clocks	1.0	2.0	4.0	ns
t <sub>10</sub>	CPUCLK, SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			250	ps
t <sub>11</sub>	PCICLK, EPCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t <sub>12</sub>	CPUCLK, PCICLK, EPCI, SDRAM	Power-up Time	CPU, PCI, EPCI, and SDRAM clock stabilization from power-up			3	ms
t <sub>13</sub>	CPUCLK, PCICLK, SDRAM	/4 Frequency Slew Time	Time for CPU, EPCI, PCI, and SDRAM clock frequency to change from F to F/4 after select input change		10	25	cycles

Notes:

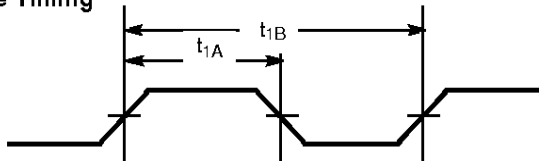
- 7. All parameters specified with loaded outputs.
- 8. Duty cycle is measured at 1.5V when V<sub>DD</sub> = 3.3V. When V<sub>DDCPU</sub> = 2.5V, CPUCLK duty cycle is measured at 1.25V.

### Timing Requirement for the I<sup>2</sup>C Bus

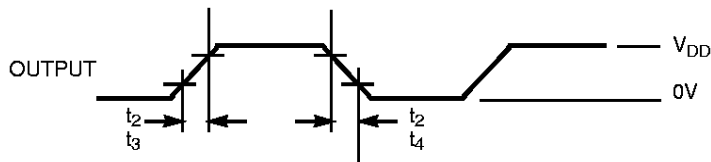
Parameter	Description	Min.	Max.	Unit
t <sub>12</sub>	SCLK Clock Frequency	0	100	kHz
t <sub>13</sub>	Time the bus must be free before a new transmission can start	4.7		μs
t <sub>14</sub>	Hold time start condition. After this period the first clock pulse is generated.	4		μs
t <sub>15</sub>	The LOW period of the clock.	4.7		μs
t <sub>16</sub>	The HIGH period of the clock.	4		μs
t <sub>17</sub>	Set-up time for start condition. (Only relevant for a repeated start condition.)	4.7		μs
t <sub>18</sub>	Hold time DATA for CBUS compatible masters. for I <sup>2</sup> C devices	5 0		μs
t <sub>19</sub>	DATA input set-up time	250		ns
t <sub>20</sub>	Rise time of both SDATA and SCLK inputs		1	μs
t <sub>21</sub>	Fall time of both SDATA and SCLK inputs		300	ns
t <sub>22</sub>	Set-up time for stop condition	4.0		μs

### Switching Waveforms

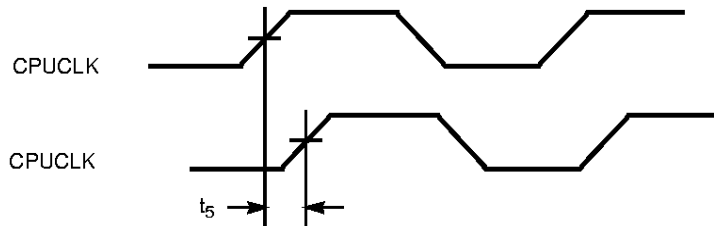
#### Duty Cycle Timing

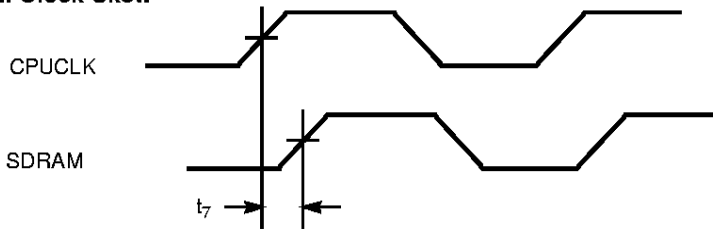
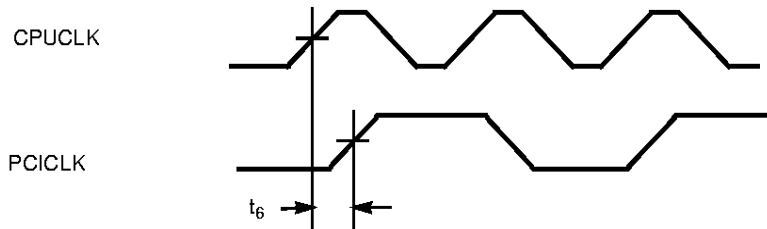
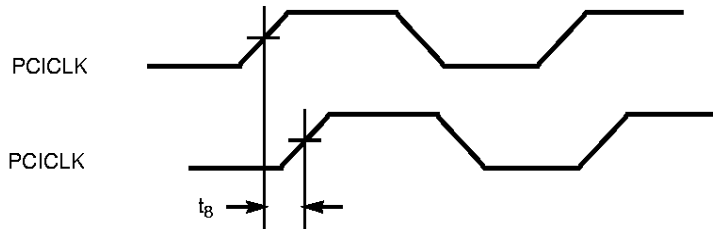
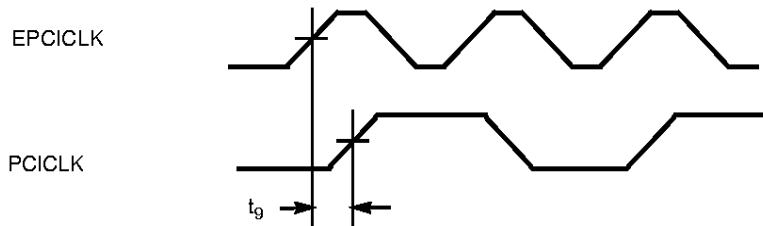
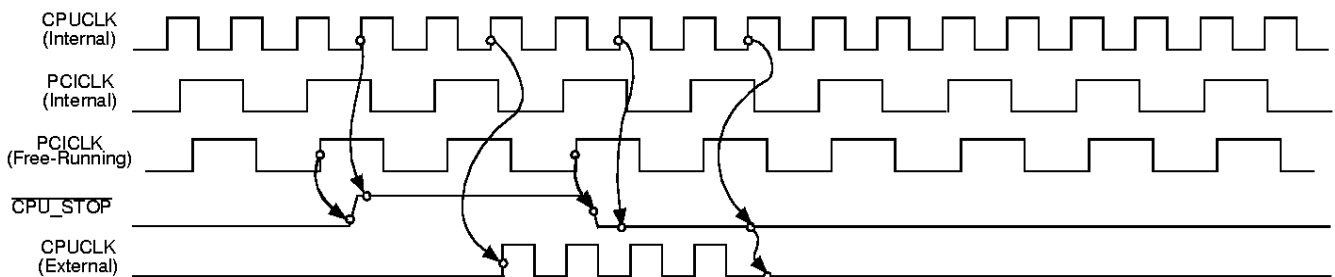


#### All Outputs Rise/Fall Time



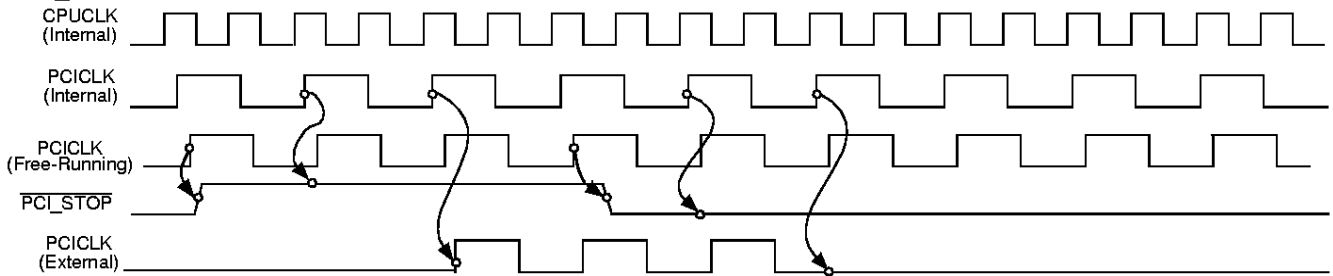
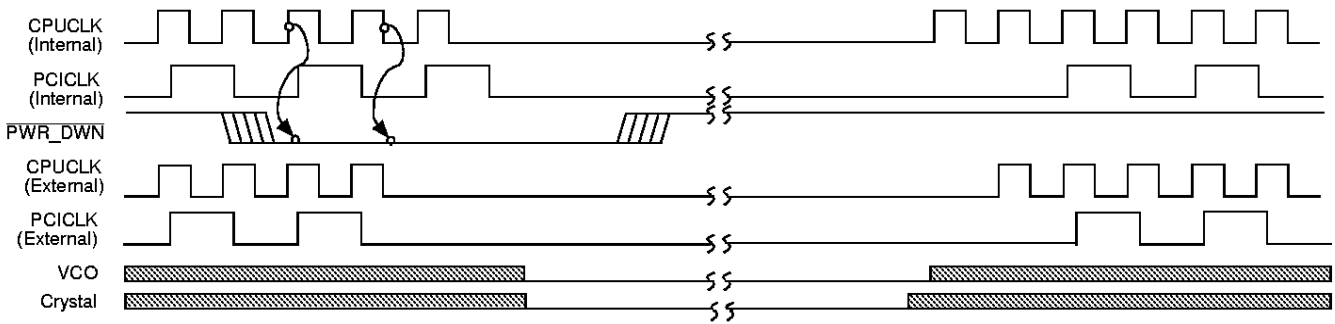
#### CPU-CPU Clock Skew



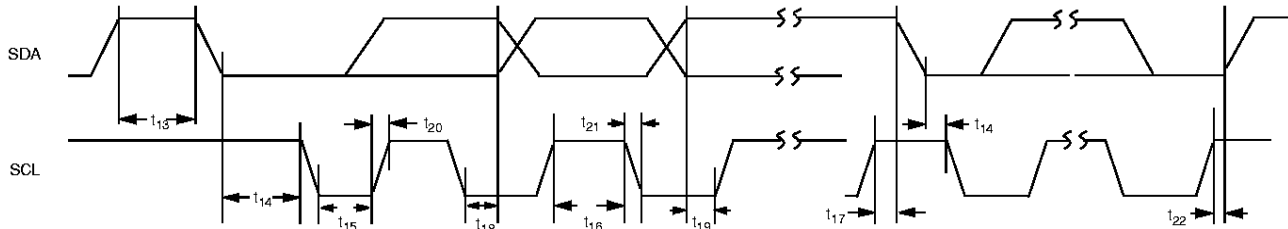
**Switching Waveforms (continued)**
**CPU-SDRAM Clock Skew**

**CPU-PCI Clock Skew**

**PCI-PCI Clock Skew**

**EPCI-PCI Clock Skew**

**CPU\_STOP<sup>[9, 10]</sup>**

**Notes:**

9. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
10. CPU\_STOP may be applied asynchronously. It is synchronized internally.



**Switching Waveforms (continued)**
**PCI\_STOP<sup>[11, 12]</sup>**

**PWR\_DOWN**


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

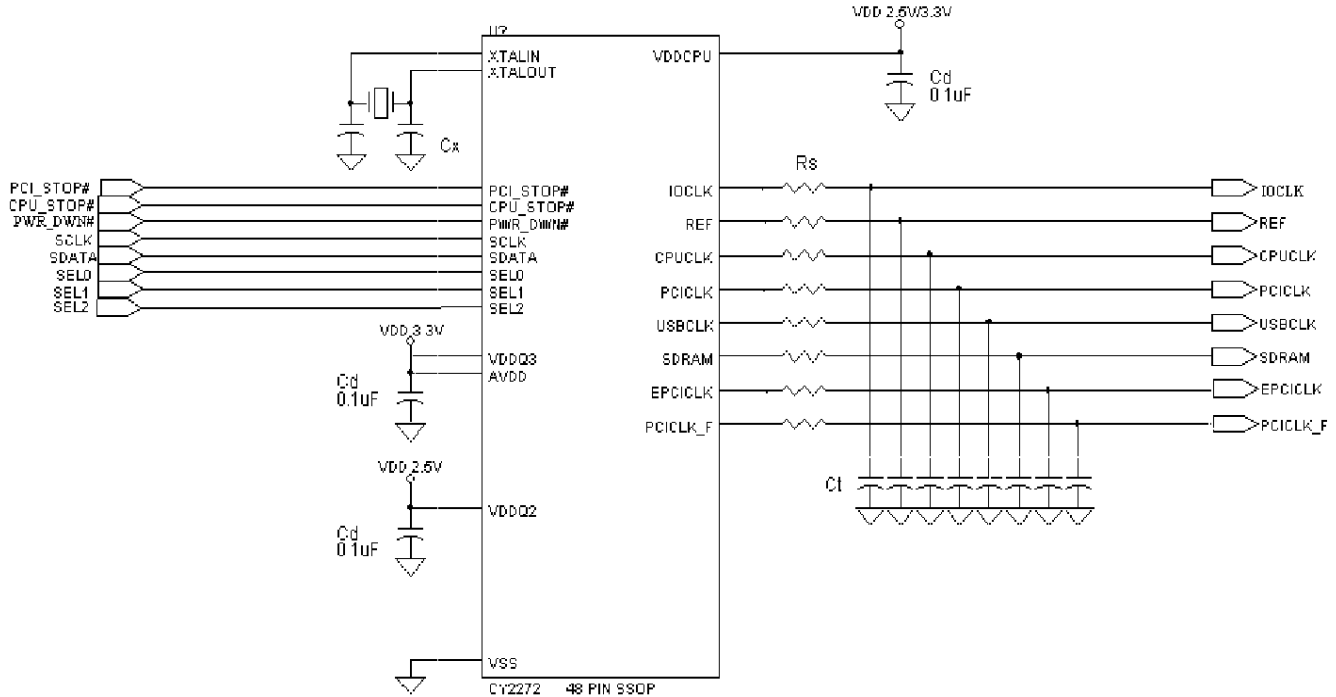
**Timing Requirements for the I<sup>2</sup>C Bus**

**Notes:**

11. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
12. PCI\_STOP may be applied asynchronously. It is synchronized internally.

## Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

## Application Circuit



Cd = DECOUPLING CAPACITORS

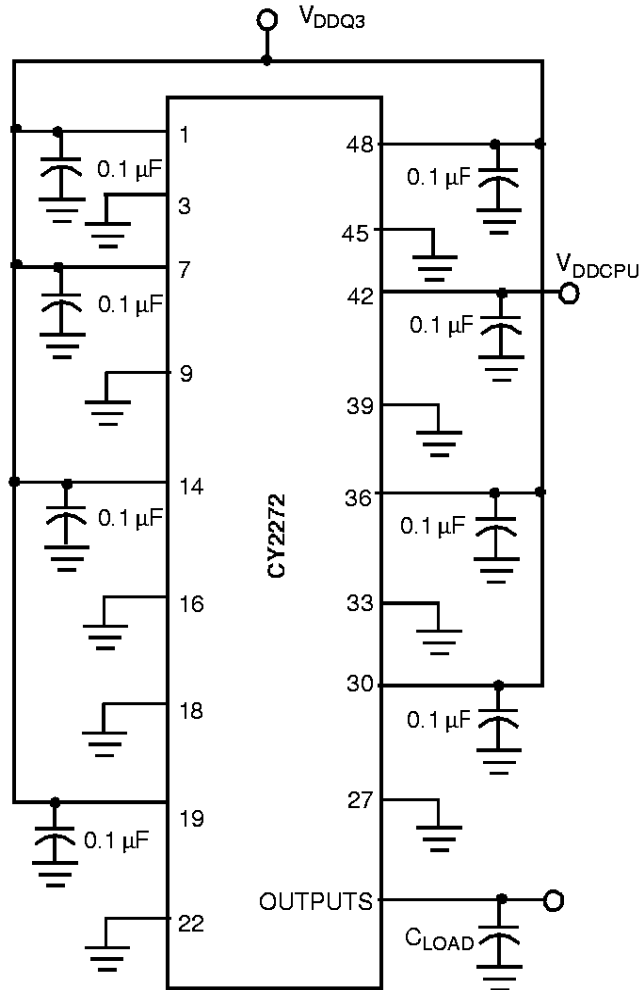
Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rs = SERIES TERMINATING RESISTORS

## Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and  $C_{LOAD}$  of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different  $C_{LOAD}$  is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1  $\mu$ F. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where  $R_{trace}$  is the loaded characteristic impedance of the trace,  $R_{out}$  is the output impedance of the clock generator (specified in the data sheet), and  $R_{series}$  is the series terminating resistor.
 
$$R_{series} \geq R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board  $V_{DD}$  from the clock generator  $V_{DD}$  island. Ensure that the Ferrite Bead offers greater than 50 $\Omega$  impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10  $\mu$ F–22  $\mu$ F tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

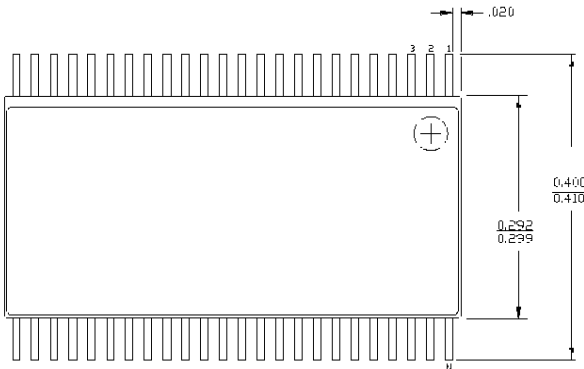
**Test Circuit**


Note: All Capacitors must be placed as close to the pins as is possible

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY2272PVC-1	O48	48-Pin SSOP	Commercial

Document #: 38-00607

**Package Diagram**
**48-Lead Shrink Small Outline Package O48**

 DIMENSIONS IN INCHES MIN.  
MAX.
