

OBJECTIVE SPECIFICATIONS

Dual 4-Bit Binary Counters

Features

- *Function, pin-out, speed and drive compatibility with 54/74ALS logic family*
- *Low power consumption characteristic of CMOS*
- *High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$*
- *Inputs and outputs interface directly with TTL, NMOS and CMOS devices*
- *Wide operating voltage range: 4.5V to 5.5V*
- *Characterized for operation over industrial and military temperature ranges:*

74AHCT: -40°C to $+85^{\circ}\text{C}$

54AHCT: -55°C to $+125^{\circ}\text{C}$

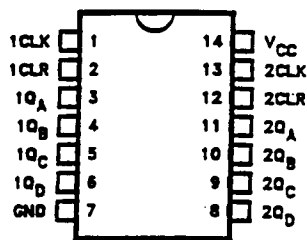
Description

The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. Parallel outputs from each counter stage provide any submultiple of the input count frequency for system timing signals.

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

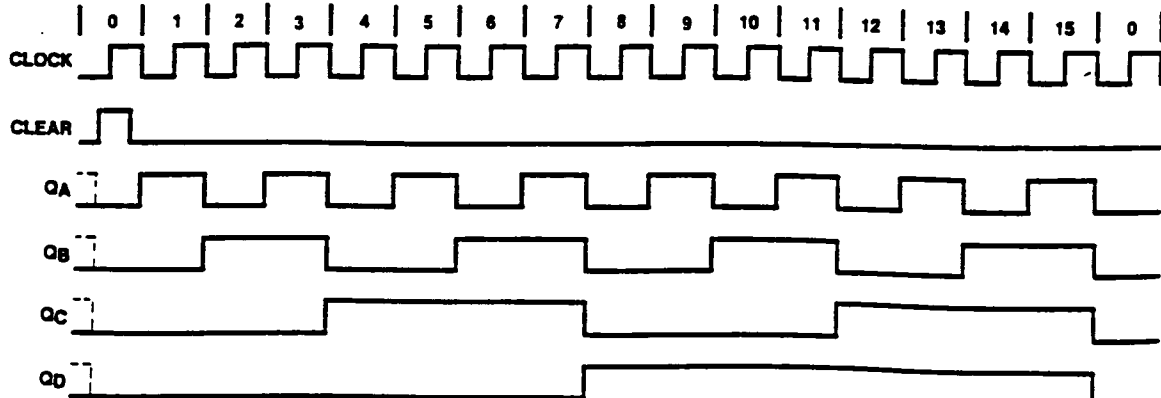
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration



0046-1

Logic Timing Waveforms



0046-1

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{STG} .. -65°C to +150°C
 Power Dissipation Per Package, P_D † 500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): -12 mW/°C from 65°C to 85°C
 Ceramic Package (J): -12 mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}
 Operating Temperature
 Range
 74AHCT: -40°C to +85°C
 54AHCT: -55°C to +125°C
 Input Rise & Fall Times, t_r , t_f Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ C$		74AHCT	54AHCT	Unit
			Typ	Guaranteed Limits			
				$T_A = -40^\circ C$ to $+85^\circ C$	$T_A = -55^\circ C$ to $+125^\circ C$		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20 \mu A$ $I_O = -4 mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20 \mu A$ $I_O = 4 mA$ $I_O = 8 mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		8.0	80.0	160.0	μA

AC Electrical Characteristics (Input $t_r, t_f \leq 2$ ns), AHCT393

Symbol	Parameter		Conditions†	$T_A = 25^\circ\text{C}$	74AHCT	54AHCT	Unit
				$V_{CC} = 5.0\text{V}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
				Typ	Guaranteed Limits		
f_{max}	Maximum Operating Frequency		$C_L = 50$ pF	50	30	25	MHz
t_{PLH}	Maximum Propagation Delay, A to Q_A			8	13	16	ns
t_{PHL}				8	13	16	
t_{PLH}	Maximum Propagation Delay, A to Q_B			14	23	28	ns
t_{PHL}				14	23	28	
t_{PLH}	Maximum Propagation Delay, A to Q_C			17	28	34	ns
t_{PHL}				17	28	34	
t_{PLH}	Maximum Propagation Delay, A to Q_D			23	38	46	ns
t_{PHL}				23	38	46	
t_{PHL}	Maximum Propagation Delay, CLR to any Q			15	25	30	ns
t_w	Minimum Pulse Width	A Input High or Low		7	12	15	ns
		CLR High		7	12	15	
t_{su}	Minimum Setup Time, CLR Inactive before A			5	8	10	ns
C_{IN}	Maximum Input Capacitance			5			pF
C_{PD}	Power Dissipation Capacitance*		(per counter)	40			pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
†For AC switching test circuits and timing waveforms see section 2.