54F113
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop Without Reset

Product Specification

DESCRIPTION

The 54F113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set ($\overline{S}_D$) input, when Low, forces the outputs to the steady state levels as shown in the Funcion Table regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of $\overline{CP}$.

ORDERING INFORMATION

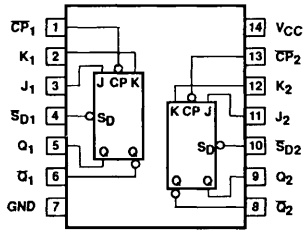
DESCRIPTION	ORDER CODE
Ceramic DIP	54F113/BCA
Ceramic Flat Pack	54F113/BDA
Ceramic LLCC	54F113/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, K_1, K_2	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock pulse inputs (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct set inputs (active Low)	1.0/5	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

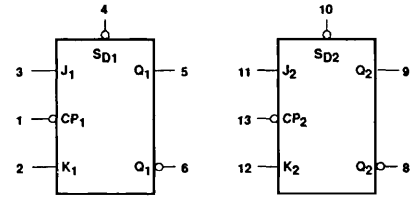
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments see JEDEC Standard No. 2

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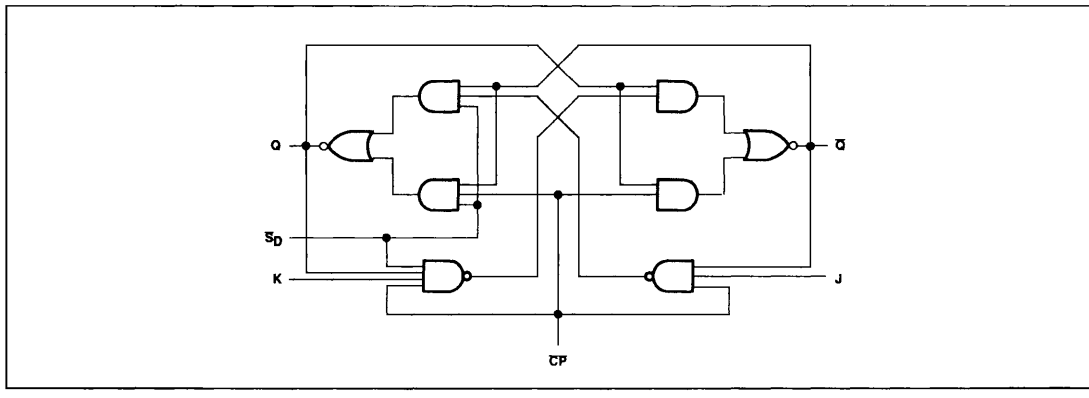
LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = High voltage level steady state.
h = High voltage level one setup time prior to the High-to-Low Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the High-to-Low Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low Clock transition.
X = Don't Care.
↓ = High-to-Low Clock transition.
Asynchronous input:
Low input to $\overline{S}_D$ set Q to High level
Set is independent of clock.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS *(Over recommended operating free-air temperature range unless otherwise noted.)*

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	J_n, K_n	V_{CC} = Max, V_I = 7.0V			100	µA
		$\overline{S}_{Dn}$				100	µA
		$\overline{CP}_n$				100	µA
I_{IH1}	High-level input current	J_n, K_n	V_{CC} = Max, V_I = 2.7V			20	µA
		$\overline{S}_{Dn}$				20	µA
		$\overline{CP}_n$				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = Max, V_I = 0.5V			-0.6	mA
		$\overline{S}_{Dn}$				-3.0	mA
		$\overline{CP}_n$				-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		15	21	mA

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.5			6.0 5.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns ns
t_w(H) t_w(L)	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns ns
t_w(L)	SD_n pulse width	Waveform 2	4.5			5.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ to $\overline{CP}_n$	Waveform 2	4.5			6.0		ns

AC ELECTRICAL CHARACTERISTICS

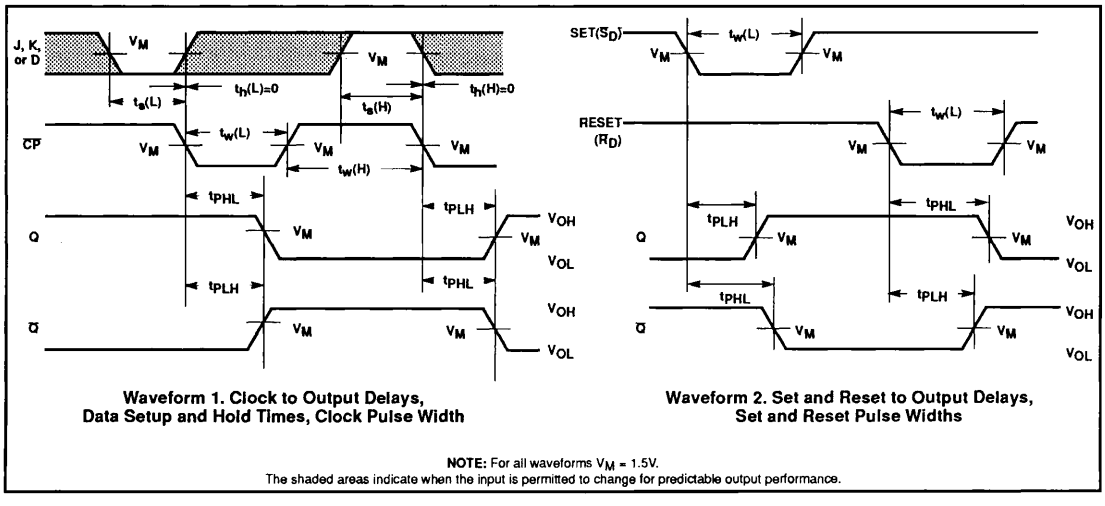
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	85	100		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Qn, $\overline{Q}$n	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	8.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ to Q_n, $\overline{Q}_n$	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	8.5 8.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS

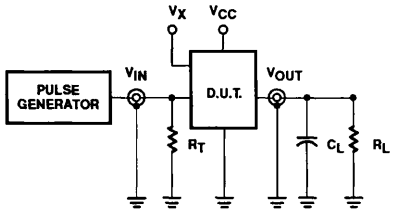


Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width

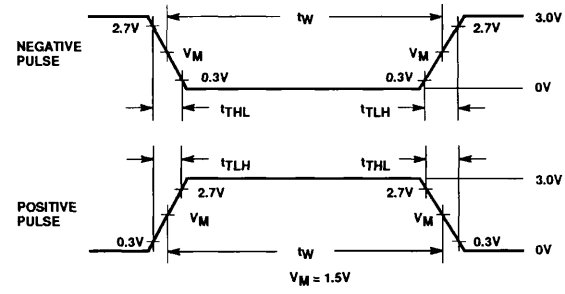
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

NOTE: For all waveforms V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns