

MITSUBISHI <DIGITAL ASSP>
M74HC373-1P/FP

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

DESCRIPTION

The M74HC373-1 is an integrated circuit chip consisting of eight 3-state output D-type latches with common-enable input and output-enable input.

FEATURES

- High-fanout 3-state output : ($I_{OL}=24\text{mA}$, $I_{OH}=-24\text{mA}$)
- High-speed : 9ns typ. ($C_L=50\text{pF}$, $V_{CC}=5\text{V}$)
- Low power dissipation : $25\mu\text{W}/\text{package}$, max
($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, quiescent state)
- High noise margin : 30% of V_{CC} , min ($V_{CC}=4.5, 6\text{V}$)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : $V_{CC}=2\sim 6\text{V}$
- Wide operating temperature range : $T_a=-40\sim +85^\circ\text{C}$

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

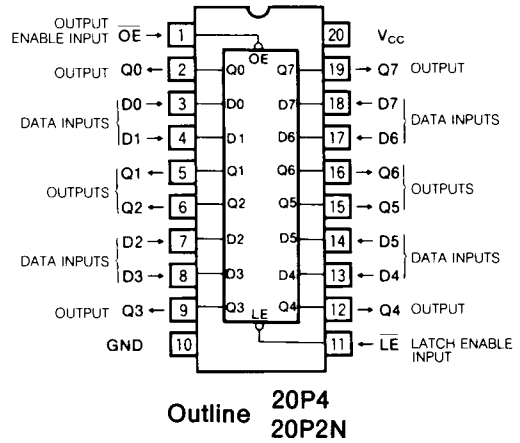
FUNCTION

Use of silicon gate technology allows the M74HC373-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS373. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. The M74HC373-1 consists of eight D-type latches with latch-enable input $\overline{\text{LE}}$ and output-enable input $\overline{\text{OE}}$ common to all circuits.

When $\overline{\text{LE}}$ is high-level, the data input D appears at output Q through the latch and the Q state follows changes in the D state. When $\overline{\text{LE}}$ changes from high to low-level, the data immediately prior to the change at D will be stored in the latch.

Even if other inputs are changed when $\overline{\text{LE}}$ is low-level, the contents stored in the latch will not be affected.

PIN CONFIGURATION (TOP VIEW)



When $\overline{\text{OE}}$ is high-level, all outputs Q will become high-impedance states.

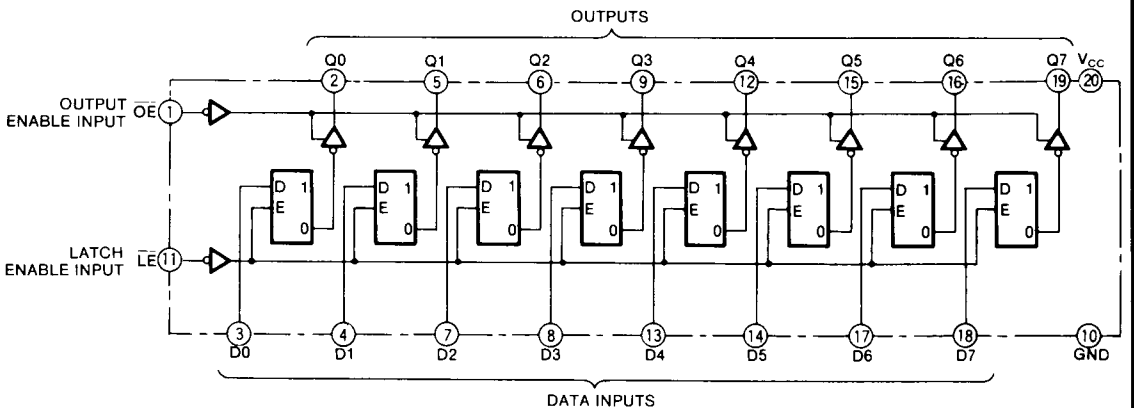
A version of the M74HC373-1 with the same pin connection and an inverted output, the M74HC533-1, is also available.

FUNCTION TABLE (Note 1)

Inputs			Output
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ⁰
H	X	X	Z

Note 1 : Q⁰ : Output state Q before $\overline{\text{LE}}$ changed.
 Z : High impedance
 X : Irrelevant

LOGICAL DIAGRAM



OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC} + 0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC} + 0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_D	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature		$-65 \sim +150$	$^\circ\text{C}$

Note 2 : M74HC373-1FP : $T_a = -40 \sim +75^\circ\text{C}$ and $T_a = 75 \sim 85^\circ\text{C}$ are derated at $-7\text{mW}/^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	-40		+85	$^\circ\text{C}$
t_r, t_f	Input rise time, fall time	$V_{CC} = 2.0V$	0	500	ns/V
		$V_{CC} = 4.5V$	0	50	
		$V_{CC} = 6.0V$	0	30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits					Unit
			25 $^\circ\text{C}$					
			$V_{CC}(V)$	Min	Typ	Max	Max	
V_{IH}	High-level input voltage	$V_O = 0.1V, V_{CC} = 0.1V$ $I_O = 20\mu A$	2.0	1.5			1.5	V
			4.5	3.15			3.15	
			6.0	4.2			4.2	
V_{IL}	Low-level input voltage	$V_O = 0.1V, V_{CC} = 0.1V$ $I_O = 20\mu A$	2.0			0.5	0.5	V
			4.5			1.35	1.35	
			6.0			1.8	1.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}, V_{IH}$	$I_{OH} = -20\mu A$	2.0	1.9		1.9	V
			$I_{OH} = -20\mu A$	4.5	4.4		4.4	
			$I_{OH} = -20\mu A$	6.0	5.9		5.9	
			$I_{OH} = -24mA$	4.5	3.83		3.70	
V_{OL}	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20\mu A$	2.0		0.1	0.1	V
			$I_{OL} = 20\mu A$	4.5		0.1	0.1	
			$I_{OL} = 20\mu A$	6.0		0.1	0.1	
			$I_{OL} = 24mA$	4.5		0.44	0.53	
I_{IH}	High-level input current	$V_I = 6V$	6.0		0.1	1.0	μA	
I_{IL}	Low-level input current	$V_I = 0V$	6.0		-0.1	-1.0	μA	
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}, V_{IL}, V_O = V_{CC}$	6.0		0.5	5.0	μA	
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}, V_{IL}, V_O = \text{GND}$	6.0		-0.5	-5.0	μA	
I_{CC}	Quiescent supply current	$V_I = V_{CC}, \text{GND}, I_O = 0\mu A$	6.0		5.0	50.0	μA	

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	$C_L = 50pF$ (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D - Q)				17	ns
t_{PHL}					17	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (LE - Q)				20	ns
t_{PHL}					20	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE} - Q$)	$C_L = 5 pF$ (Note 4)			18	ns
t_{PHZ}					18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE} - Q$)	$C_L = 50pF$ (Note 4)			20	ns
t_{PZH}					20	ns

SWITCHING CHARACTERISTICS ($V_{CC} = 2\sim 6V$, $T_a = -40\sim +85^\circ C$)

Symbol	Parameter	Test conditions	Limits					Unit	
			$V_{CC}(V)$	25°C			-40~+85°C		
				Min	Typ	Max	Min		Max
t_{TLH}	Low-to high-level and high-to low-level output transition time	$C_L = 50pF$ (Note 4)	2.0	12	60		75	ns	
			4.5	5	12		15		
			6.0	4	10		13		
t_{THL}			2.0	18	60		75	ns	
			4.5	5	12		15		
			6.0	4	10		13		
t_{PLH}	Low-to high-level and high-to low-level output propagation time (D - Q)		2.0	36	90		115	ns	
			4.5	9	18		23		
			6.0	7	15		20		
t_{PHL}			2.0	28	90		115	ns	
			4.5	10	18		23		
			6.0	9	15		20		
t_{PLH}	Low-to high-level and high-to low-level output propagation time ($\overline{LE} - Q$)	2.0	32	105		130	ns		
		4.5	11	21		26			
		6.0	9	18		22			
t_{PHL}		2.0	33	105		130	ns		
		4.5	11	21		26			
		6.0	9	18		22			
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE} - Q$)	2.0	15	105		130	ns		
		4.5	7	21		26			
		6.0	7	18		22			
t_{PHZ}		2.0	16	105		130	ns		
		4.5	10	21		26			
		6.0	9	18		22			
t_{PZL}	Low-level and high-level output enable time ($\overline{OE} - Q$)	2.0	22	105		130	ns		
		4.5	8	21		26			
		6.0	6	18		22			
t_{PZH}		2.0	24	105		130	ns		
		4.5	9	21		26			
		6.0	7	18		22			
C_I	Input capacitance			10		10	pF		
C_O	Off-state output capacitance	$OE = V_{CC}$			15		15	pF	
C_{PD}	Power dissipation capacitance (Note 3)		44.5					pF	

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per latch). The power dissipated during operation under no-load condition is calculated using the following formula :

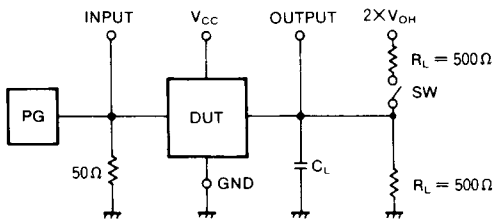
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_t + I_{CC} \cdot V_{CC}$$

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

TIMING REQUIREMENTS ($V_{CC} = 2\sim 6V$, $T_a = -40\sim +85^\circ C$)

Symbol	Parameter	Test conditions	Limits						Unit
			25°C			-40~+85°C			
			$V_{CC}(V)$	Min	Typ	Max	Min	Max	
t_w	Latch-enable pulse width		2.0	60	8		75		ns
			4.5	12	3		15		
			6.0	10	2		13		
t_{su}	D setup time with respect to \overline{LE}		2.0	50	3		65		ns
			4.5	10	1		13		
			6.0	9	1		11		
t_h	D hold time with respect to \overline{LE}		2.0	25	-2		30		ns
			4.5	5	0		6		
			6.0	5	0		6		

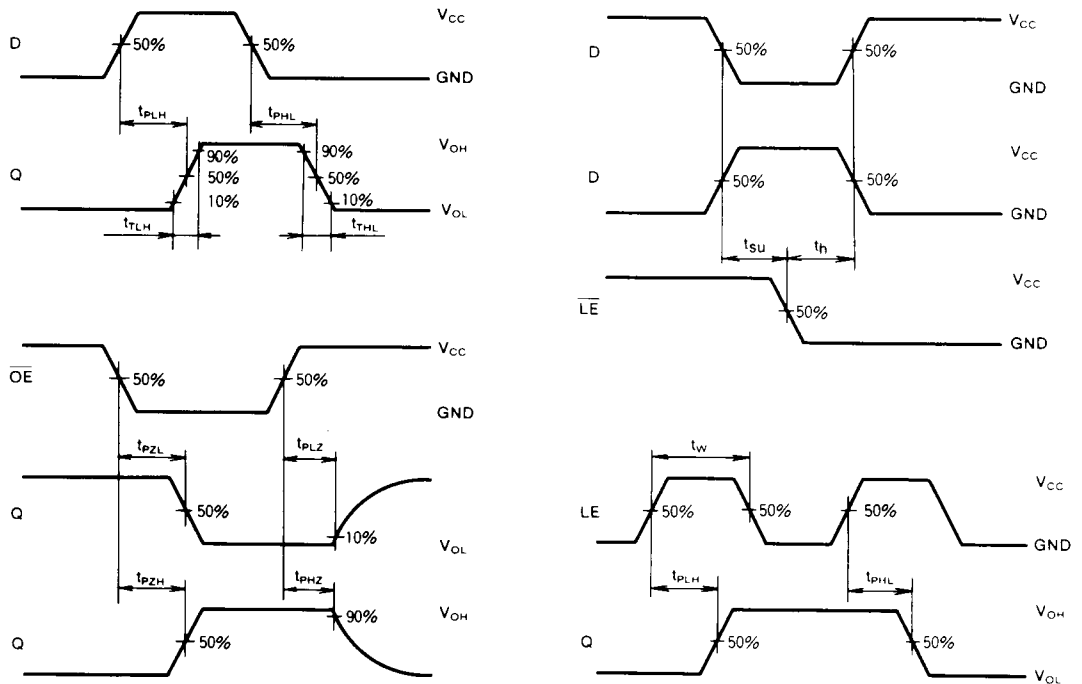
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}	Open
t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%) : $t_r=3ns$, $t_f=3ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

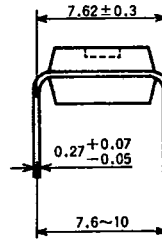
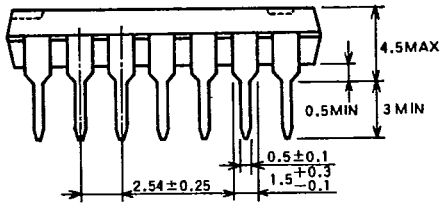
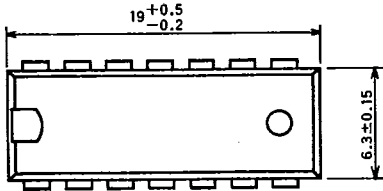
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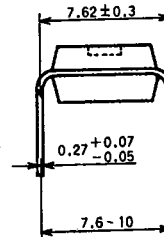
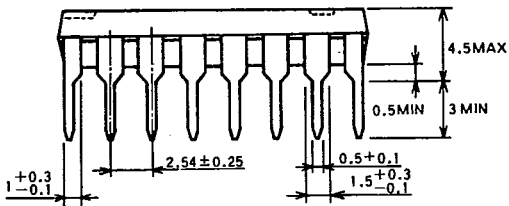
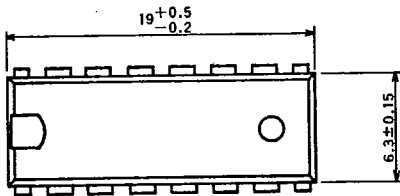
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

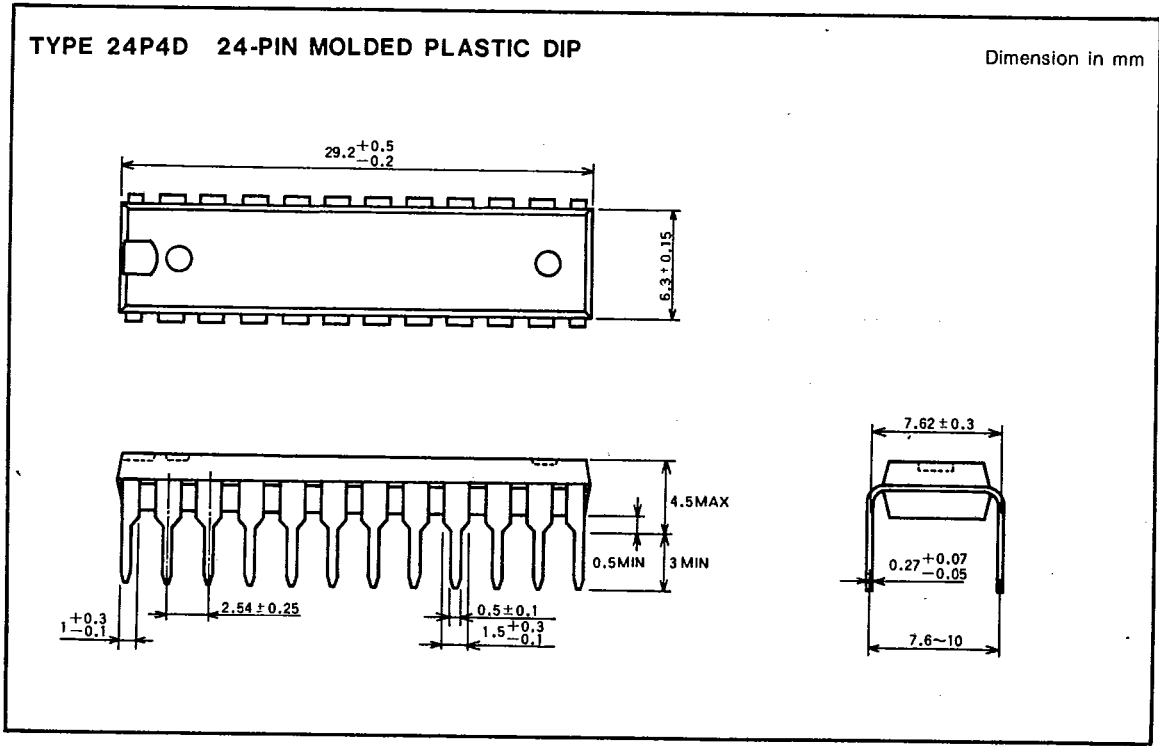
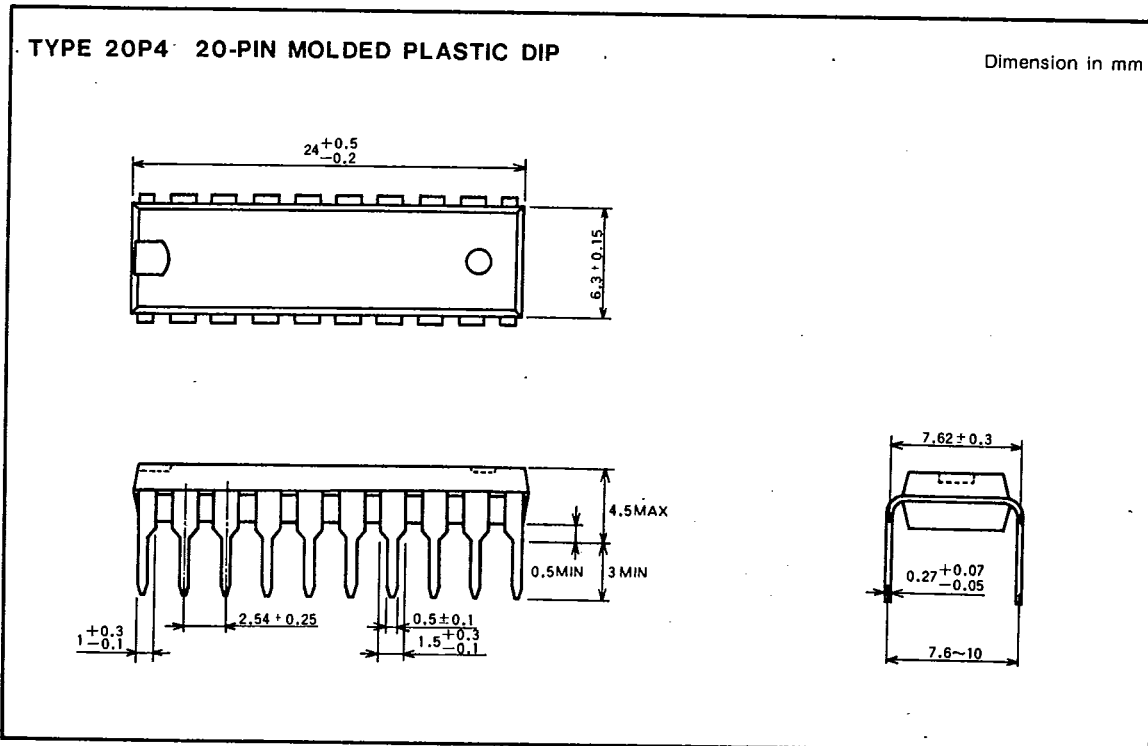
Dimension in mm



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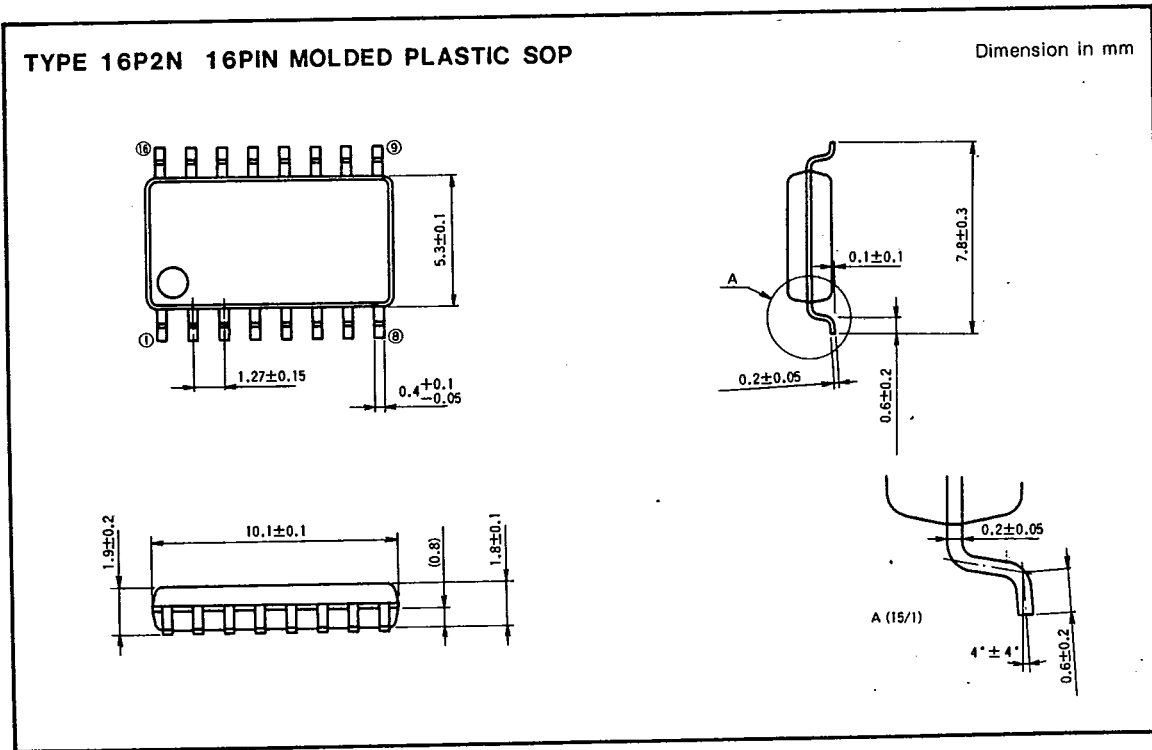
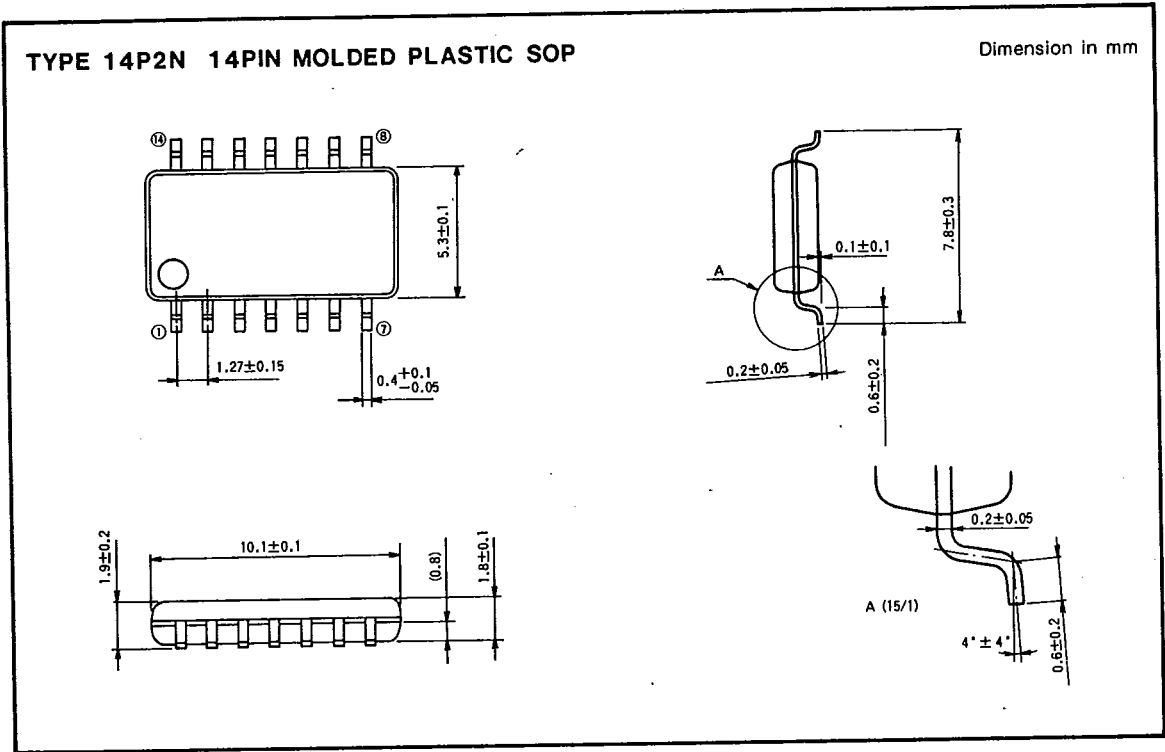


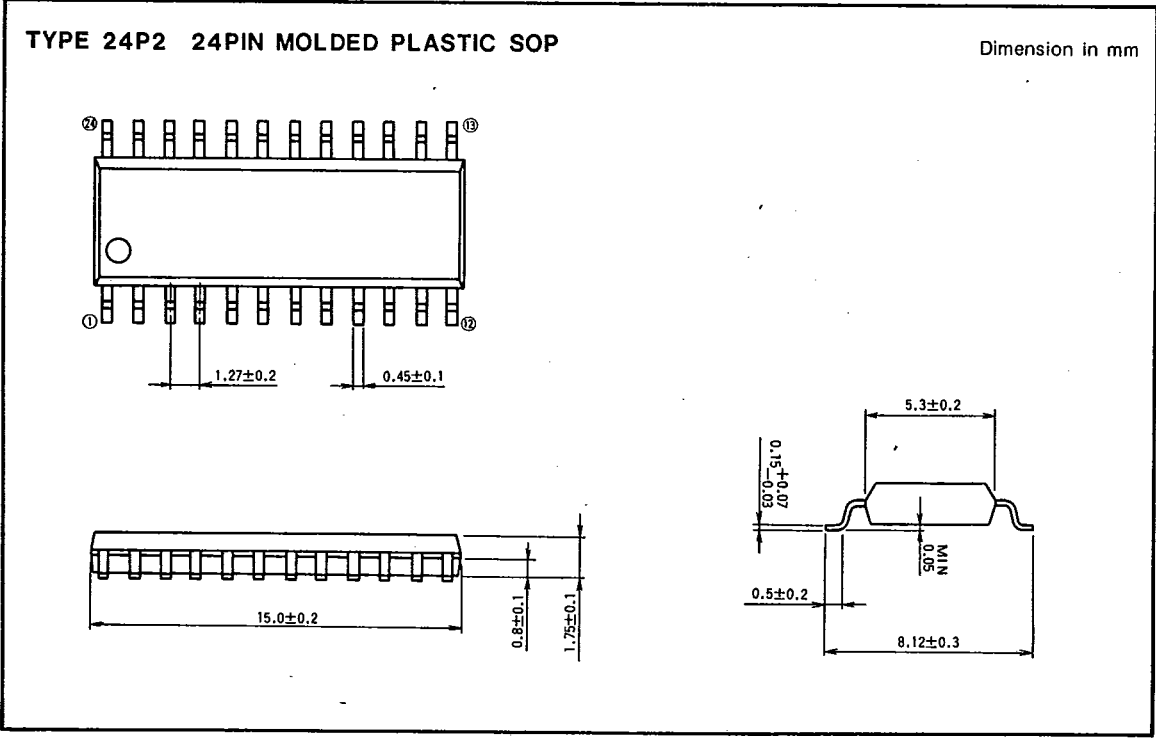
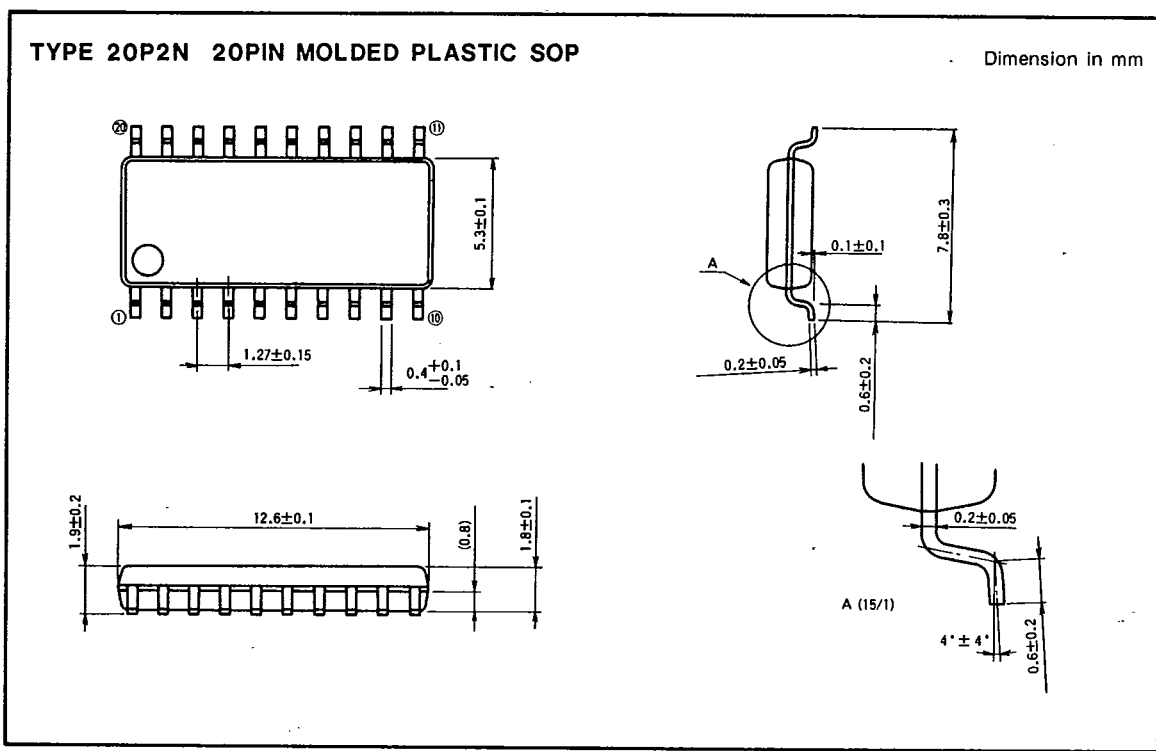
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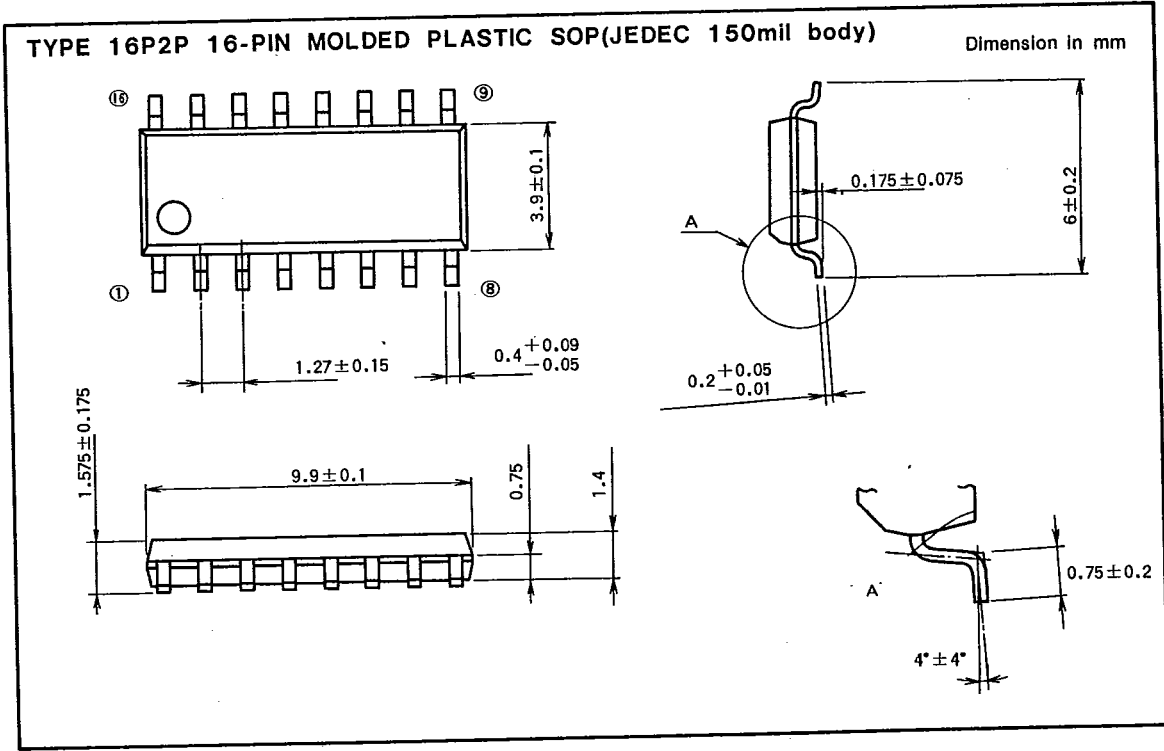
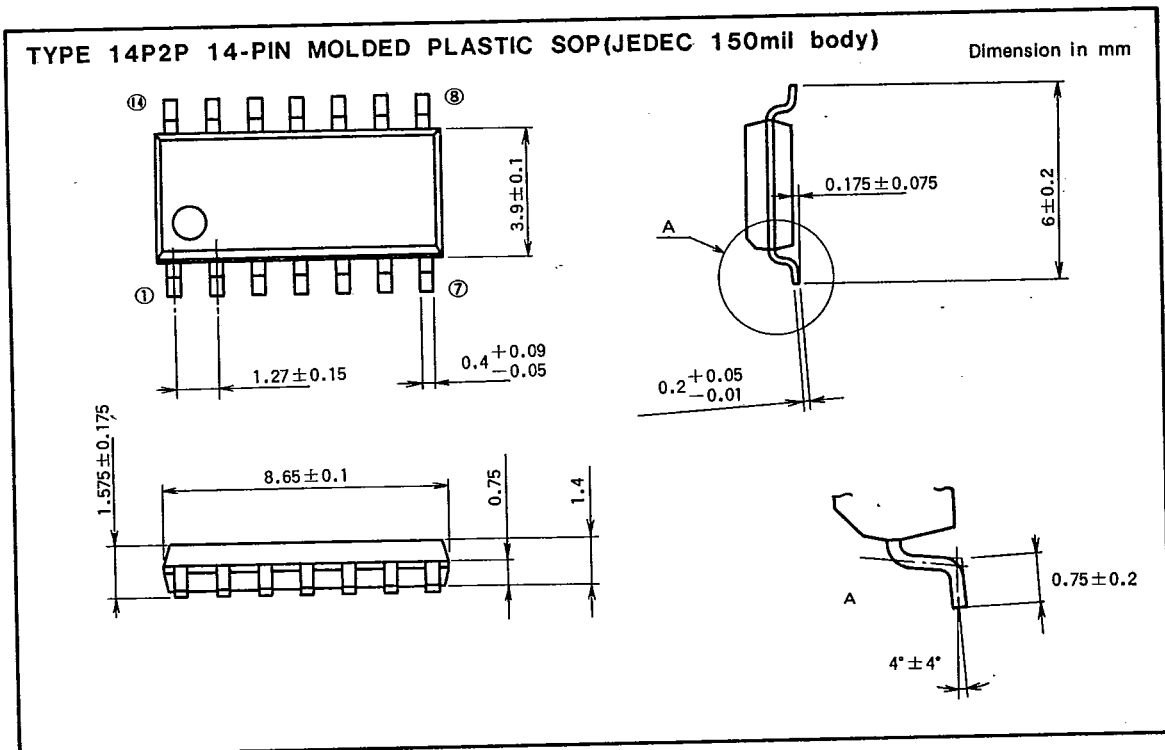
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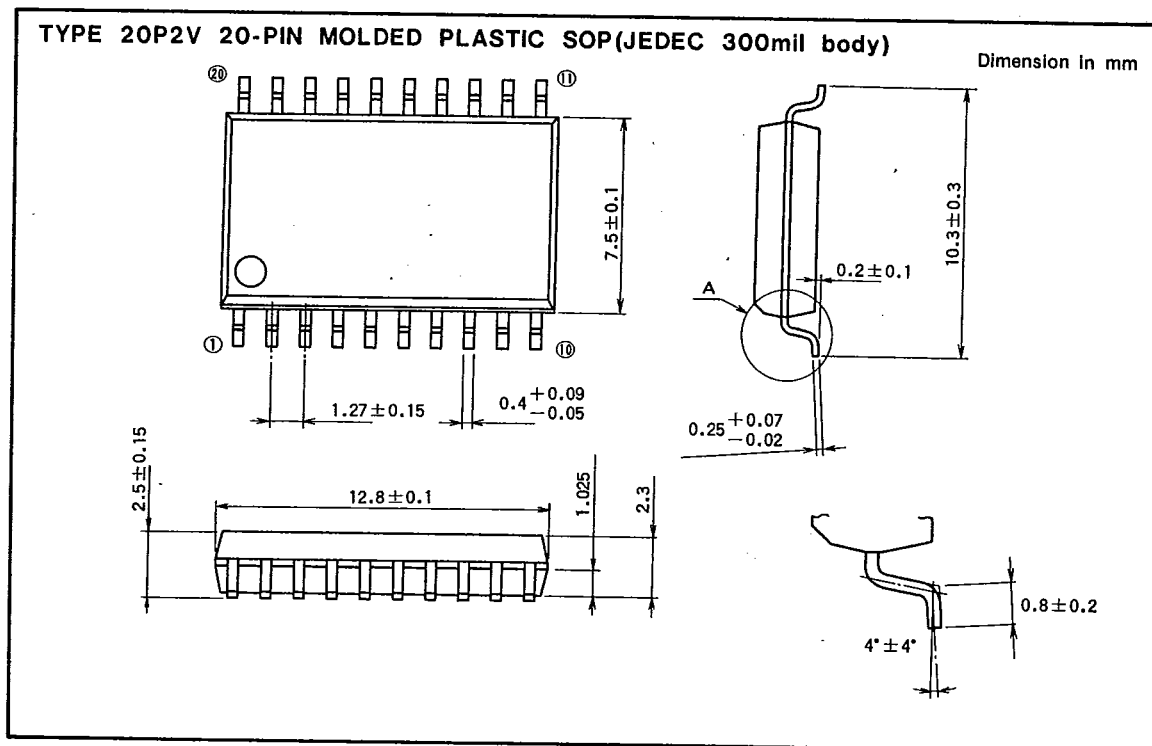




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