National Semiconductor

March 1993

# 74ACT841
# 10-Bit Transparent Latch with TRI-STATE® Outputs

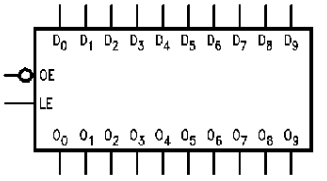
## General Description

The 'ACT841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'ACT373.

## Features

- 'ACT841 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Non-inverting TRI-STATE outputs

## Logic Symbols

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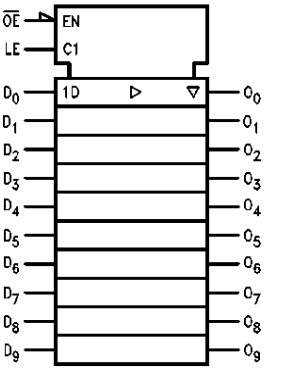
IEEE/IEC

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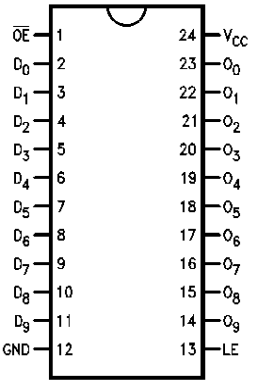
## Connection Diagram

Pin Assignment for DIP and SOIC

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| Pin Names | Description |
|---|---|
| $D_0$–$D_9$ | Data Inputs |
| $O_0$–$O_9$ | TRI-STATE Outputs |
| $\overline{OE}$ | Output Enable |
| LE | Latch Enable |

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## Functional Description

The ACT841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

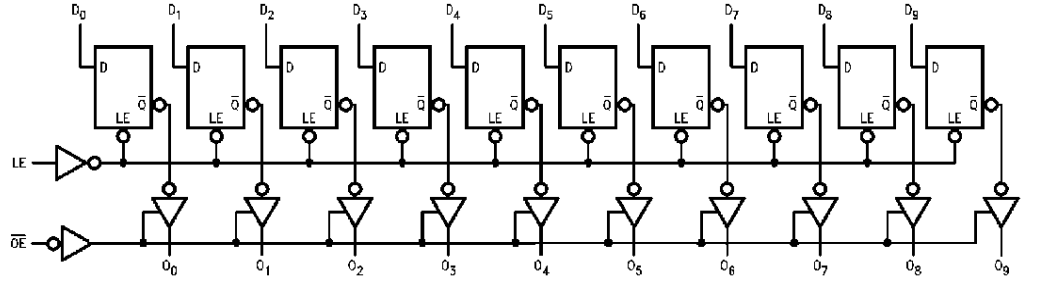
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

**Function Table**

| Inputs | | | Internal | Output | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | LE | D | Q | O | |
| X | X | X | X | Z | High Z |
| H | H | L | L | Z | High Z |
| H | H | H | H | Z | High Z |
| H | L | X | NC | Z | Latched |
| L | H | L | L | L | Transparent |
| L | H | H | H | H | Transparent |
| L | L | X | NC | NC | Latched |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| 'ACT | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| 74ACT | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| 'ACT Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

## DC Characteristics for 'ACT Family Devices

| Symbol | Parameter | $V_{CC}$ (V) | 74ACT $T_A$ = +25°C | | 74ACT $T_A$ = −40°C to +85°C | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 2.0<br>2.0 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1V<br>or $V_{CC}$ − 0.1V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 0.8<br>0.8 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1V<br>or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.4<br>5.4 | 4.4<br>5.4 | V | $I_{OUT}$ = −50 μA |
| | | 4.5<br>5.5 | | 3.86<br>4.86 | 3.76<br>4.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OH}$ −24 mA<br>$I_{OH}$ −24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1 | 0.1<br>0.1 | V | $I_{OUT}$ = 50 μA |
| | | 4.5<br>5.5 | | 0.36<br>0.36 | 0.44<br>0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OL}$ 24 mA<br>$I_{OL}$ 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±5.0 | μA | $V_I$ = $V_{IL}$, $V_{IH}$<br>$V_O$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | μA | $V_I$ = $V_{CC}$ − 2.1V |

*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics for 'ACT Family Devices (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | 74ACT $T_A = +25°C$ | | 74ACT $T_A = -40°C$ to $+85°C$ | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80.0 | μA | $V_{IN} = V_{CC}$ or GND |

†Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A = +25°C$, $C_L = 50$ pF | | | 74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay $D_n$ to $O_n$ | 5.0 | 2.0 | 5.5 | 9.5 | 2.0 | 10.0 | ns |
| $t_{PHL}$ | Propagation Delay $D_n$ to $O_n$ | 5.0 | 2.0 | 5.5 | 9.5 | 2.0 | 10.0 | ns |
| $t_{PLH}$ | Propagation Delay LE to $O_n$ | 5.0 | 2.0 | 5.5 | 9.0 | 2.0 | 10.0 | ns |
| $t_{PHL}$ | Propagation Delay LE to $O_n$ | 5.0 | 2.0 | 5.5 | 9.0 | 2.0 | 10.0 | ns |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.0 | 5.5 | 9.5 | 2.0 | 10.5 | ns |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.0 | 5.5 | 9.5 | 2.0 | 10.5 | ns |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.0 | 6.0 | 10.5 | 2.0 | 11.0 | ns |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.0 | 6.0 | 10.5 | 2.0 | 11.0 | ns |

*Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A = +25°C$, $C_L = 50$ pF | | 74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_s$ | Setup Time, HIGH or LOW $D_n$ to LE | 5.0 | −0.5 | 0.5 | 1.0 | ns |
| $t_h$ | Hold Time, HIGH or LOW $D_n$ to LE | 5.0 | 0.5 | 2.0 | 2.0 | ns |
| $t_w$ | LE Pulse Width, HIGH | 5.0 | 2.0 | 3.5 | 3.5 | ns |

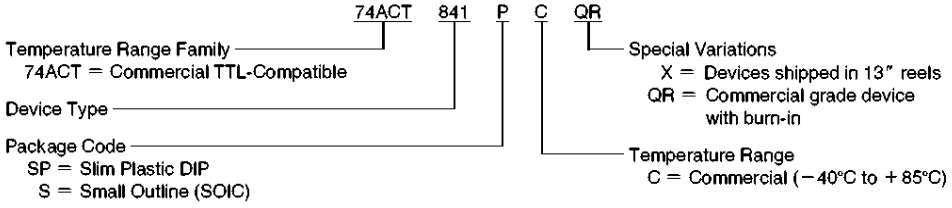
*Voltage Range 5.0 is 5.0V ±0.5V

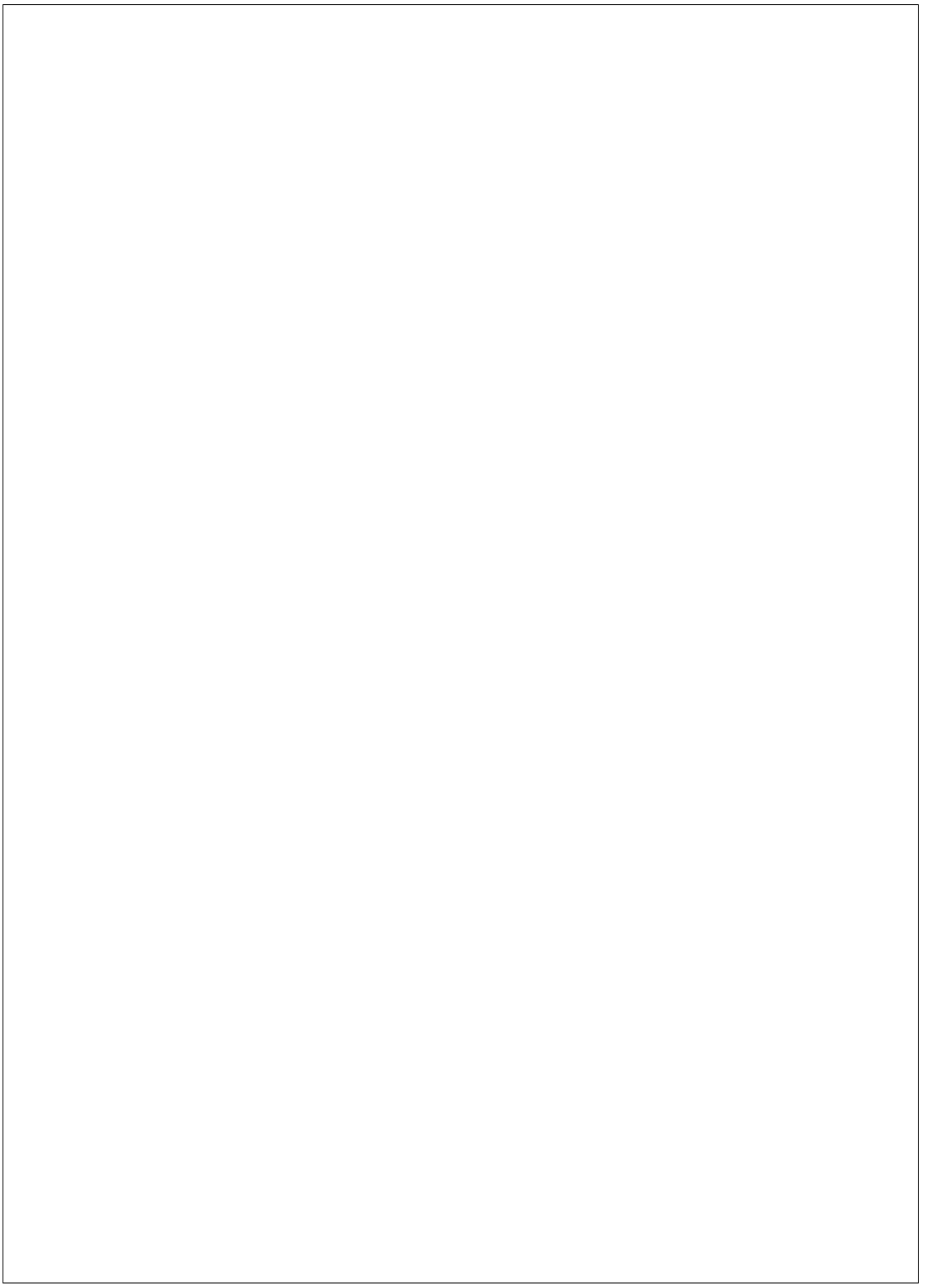
## Capacitance

| Symbol | Parameter | AC/ACT Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 44 | pF | $V_{CC}$ = 5.0V |

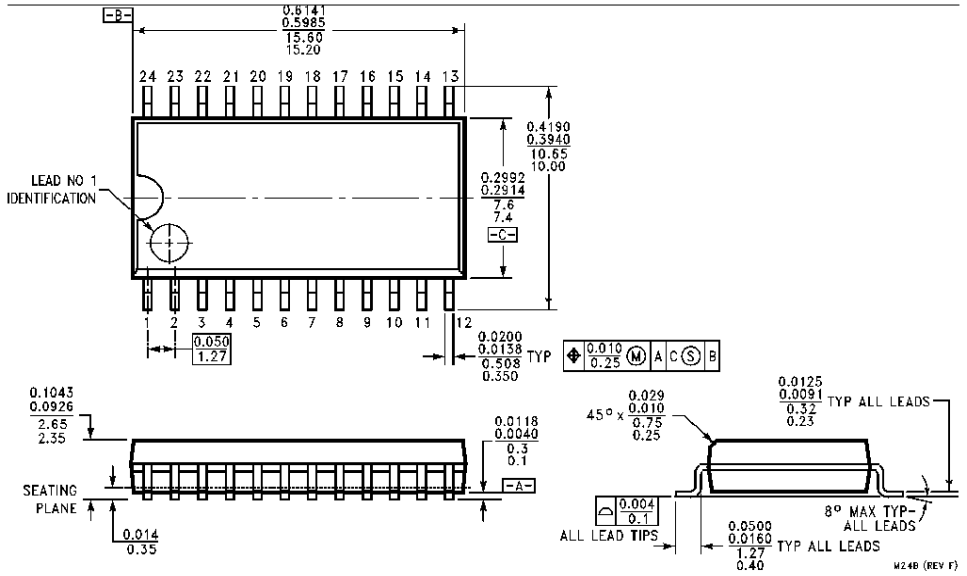
## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:





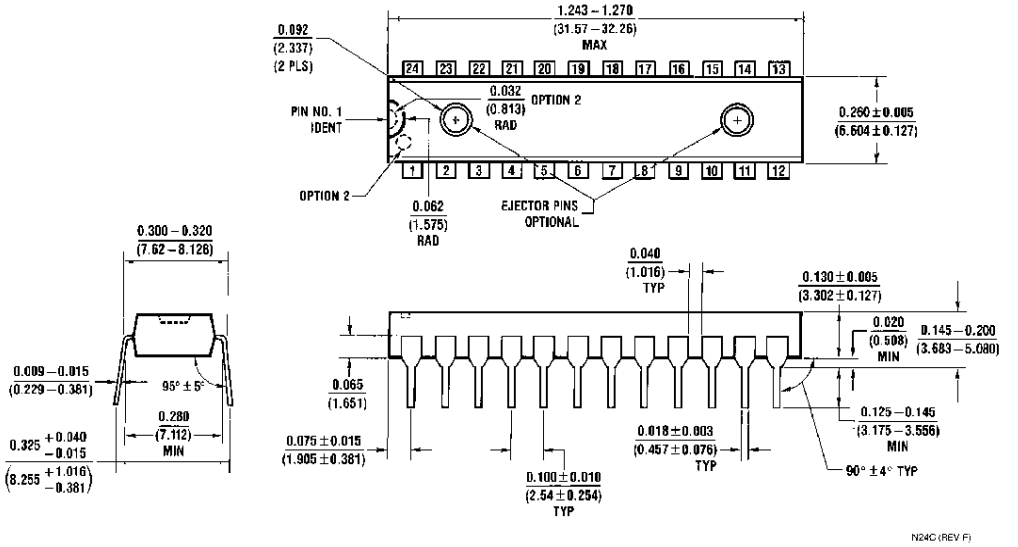
## Physical Dimensions inches (millimeters)




**24 Lead Small Outline Integrated Circuit (S)**
**NS Package Number M24B**

## Physical Dimensions inches (millimeters) (Continued)

Lit. # 114850




**24 Lead Slim (0.300" Wide) Plastic Dual-In-Line Package (SP)**
**NS Package Number N24C**

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