

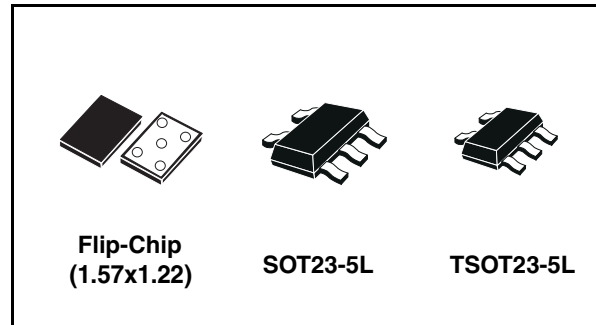


LD3985 series

Ultra low drop-low noise bicmos voltage regulators low ESR capacitors compatible

Feature summary

- Input voltage from 2.5V to 6V
- Stable with low ESR ceramic capacitors
- Ultra low dropout voltage (100mV typ. at 150mA load, 0.4mV typ. at 1mA load)
- Very low quiescent current (85µA typ. at no load, 170µA typ. at 150mA load; max 1.5µA in OFF mode)
- Guaranteed output current up to 150mA
- Wide range of output voltage: 1.2V; 1.22V; 1.25V; 1.35V; 1.5V; 1.8V; 2V; 2.1V; 2.2V; 2.4V; 2.5V; 2.6V; 2.7V; 2.8V; 2.85V; 2.9V; 3V; 3.1V; 3.2V; 3.3V; 4.4V; 4.7V; 4.8V; 4.9V; 5V
- Fast turn-on time: typ. 200µs [$C_O=1\mu F$, $C_{BYP}=10nF$ and $I_O=1mA$]
- Logic-controlled electronic shutdown
- Internal current and thermal limit
- Output low noise voltage $30\mu V_{RMS}$ over 10Hz to 100KHz
- S.V.R. of 60dB at 1KHz, 50dB at 10KHz
- Temperature range: $-40^\circ C$ to $125^\circ C$



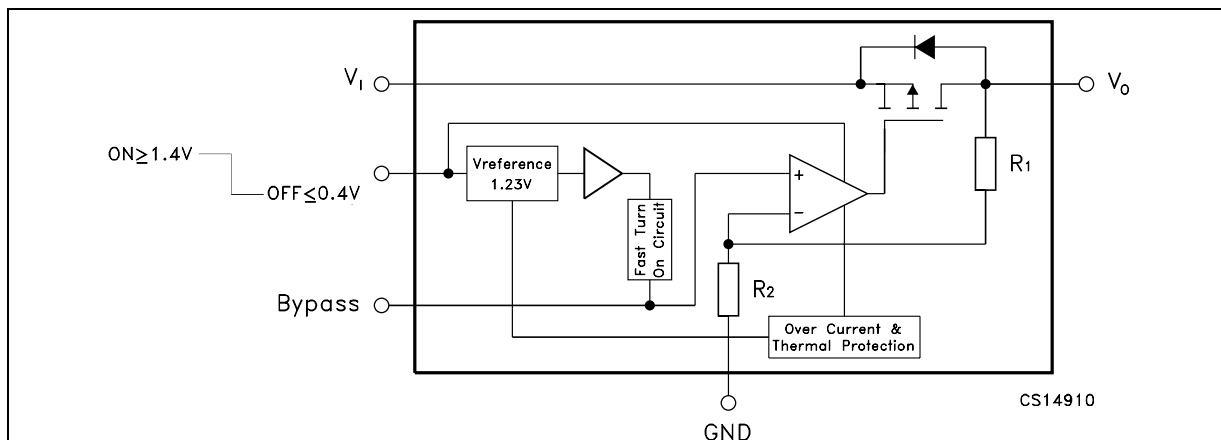
6V input voltage.

The ultra low drop-voltage, low quiescent current and low noise make it suitable for low power applications and in battery powered systems. Regulator ground current increases only slightly in dropout, further prolonging the battery life. Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10KHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits. Shutdown Logic Control function is available, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The LD3985 is designed to work with low ESR ceramic capacitors. Typical applications are in mobile phone and similar battery powered wireless systems.

Description

The LD3985 provides up to 150mA, from 2.5V to

Schematic diagram



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1 Pin configuration

Figure 1. Pin connections (top view for SOT and TSOT, top through view for DFN6)

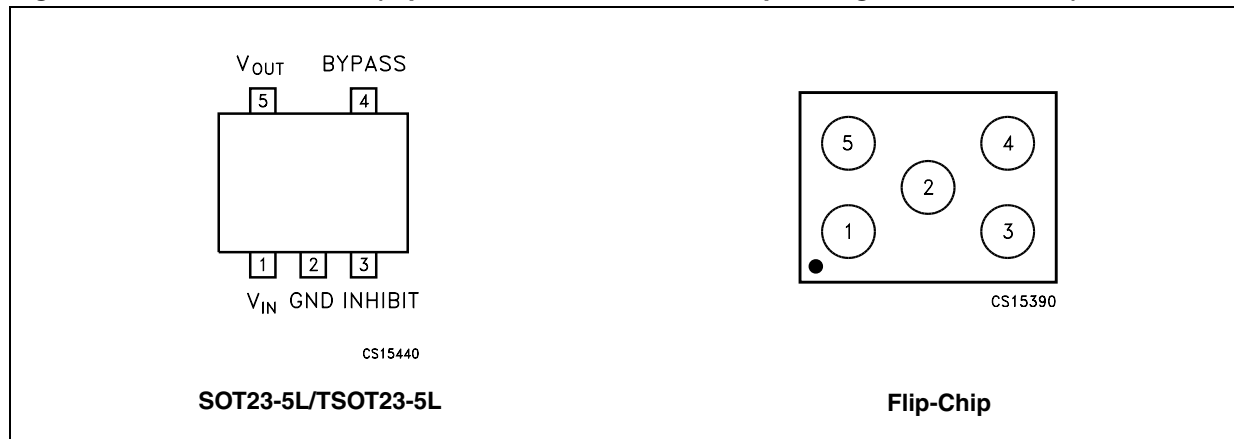
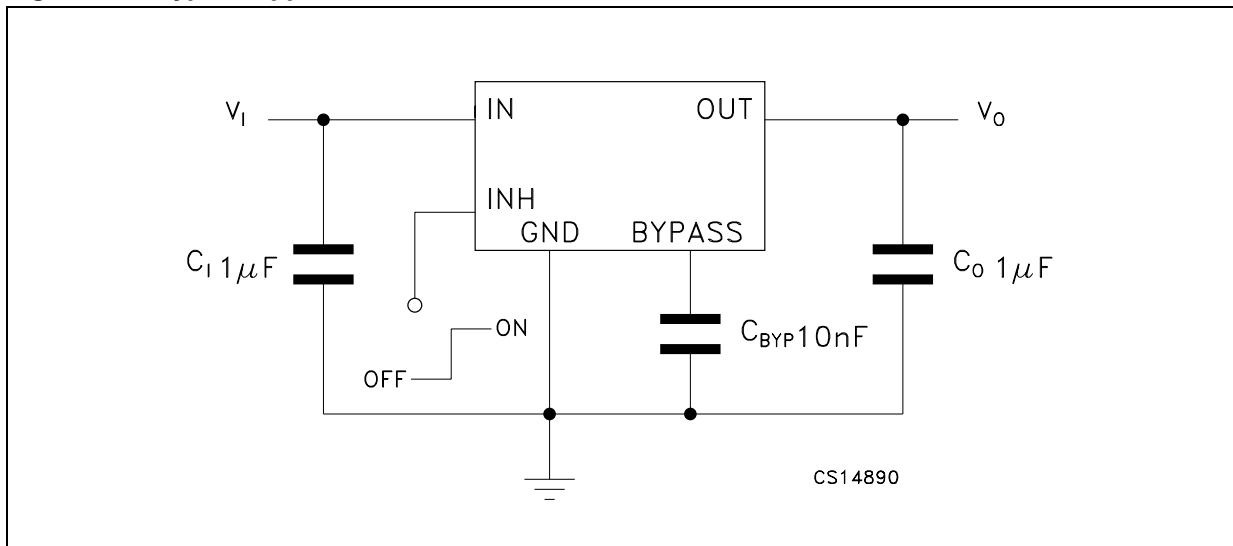


Table 1. Pin description

Pin N° for SOT23-5L/TSOT23-5L	Pin N° for Flip-Chip	Symbol	Name and function
1	1	V_I	Input Voltage of the LDO
2	5	GND	Common Ground
3	6	V_{INH}	Inhibit Input Voltage: ON MODE when $V_{INH} \geq 1.2V$, OFF MODE when $V_{INH} \leq 0.4V$ (Do not leave floating, not internally pulled down/up)
4	4	BYPASS	Bypass Pin: Connect an external capacitor (usually 10nF) to minimize noise voltage
5	3	V_O	Output Voltage of the LDO

2 Typical application

Figure 2. Typical application circuit



3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC Input voltage	-0.3 to 6 ⁽¹⁾	V
V_O	DC Output voltage	-0.3 to $V_I+0.3$	V
V_{INH}	INHIBIT Input voltage	-0.3 to $V_I+0.3$	V
I_O	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-65 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

1. The input pin is able to withstand non repetitive spike of 6.5V for 200ms.

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 3. Thermal data

Symbol	Parameter	SOT23-5L/ TSOT23	Flip-Chip	Unit
R_{thJC}	Thermal resistance junction-case	81		°C/W
R_{thJA}	Thermal resistance junction-ambient	255	170	°C/W

4 Electrical characteristics

Table 4. Electrical characteristics for LD3985 ($T_J = 25^\circ\text{C}$, $V_I = V_{O(NOM)} + 0.5\text{V}$, $C_I = 1\mu\text{F}$, $C_{BYP} = 10\text{nF}$, $I_O = 1\text{mA}$, $V_{INH} = 1.4\text{V}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage		2.5		6	V
V_O	Output voltage < 2.5V	$I_O = 1\text{mA}$	-50		50	mV
		$T_J = -40\text{ to }125^\circ\text{C}$	-75		75	
V_O	Output voltage $\geq 2.5\text{V}$	$I_O = 1\text{mA}$	-2		2	% of $V_{O(NOM)}$
		$T_J = -40\text{ to }125^\circ\text{C}$	-3		3	
ΔV_O	Line regulation (<i>Note: 1</i>)	$V_I = V_{O(NOM)} + 0.5\text{ to }6\text{V}$ $T_J = -40\text{ to }125^\circ\text{C}$	-0.1		0.1	%/ V
		$V_O = 4.7\text{ to }5\text{V}$	-0.19		0.19	
ΔV_O	Load regulation	$I_O = 1\text{mA to }150\text{mA}$, $V_O < 2.5\text{V}$ $T_J = -40\text{ to }125^\circ\text{C}$		0.002	0.008	%/ mA
ΔV_O	Load regulation	$I_O = 1\text{mA to }150\text{mA}$, $V_O \geq 2.5\text{V}$ $T_J = -40\text{ to }125^\circ\text{C}$ (for Flip-Chip)		0.0004	0.002	%/ mA
		$I_O = 1\text{mA to }150\text{mA}$, $T_J = -40\text{ to }125^\circ\text{C}$ (for SOT23-5L/TSOT23-5L), $V_O \geq 2.5\text{V}$		0.0025	0.005	
ΔV_O	Output AC Line regulation	$V_I = V_{O(NOM)} + 1\text{V}$, $I_O = 150\text{mA}$, $t_R = t_F = 30\mu\text{s}$		1.5		mV_{PP}
I_Q	Quiescent current ON MODE: $V_{INH} = 1.2\text{V}$	$I_O = 0$		85		μA
		$I_O = 0$, $T_J = -40\text{ to }125^\circ\text{C}$			150	
		$I_O = 0\text{ to }150\text{mA}$		170		
		$I_O = 0\text{ to }150\text{mA}$, $T_J = -40\text{ to }125^\circ\text{C}$			250	
	OFF MODE: $V_{INH} = 0.4\text{V}$			0.003		
		$T_J = -40\text{ to }125^\circ\text{C}$			1.5	
V_{DROP}	Dropout voltage (<i>Note: 1</i>)	$I_O = 1\text{mA}$		0.4		mV
		$I_O = 1\text{mA}$, $T_J = -40\text{ to }125^\circ\text{C}$			2	
		$I_O = 50\text{mA}$		20		
		$I_O = 50\text{mA}$, $T_J = -40\text{ to }125^\circ\text{C}$			35	
		$I_O = 100\text{mA}$		45		
		$I_O = 100\text{mA}$, $T_J = -40\text{ to }125^\circ\text{C}$			70	
		$I_O = 150\text{mA}$		60		
		$I_O = 150\text{mA}$, $T_J = -40\text{ to }125^\circ\text{C}$			100	
I_{SC}	Short circuit current	$R_L = 0$		600		mA
SVR	Supply voltage rejection	$V_I = V_{O(NOM)} + 0.25\text{V} \pm V_{RIPPLE} = 0.1\text{V}$, $I_O = 50\text{mA}$ $V_{O(NOM)} < 2.5\text{V}$, $V_I = 2.55\text{V}$	$f = 1\text{KHz}$	60		dB
			$f = 10\text{KHz}$	50		
$I_{O(PK)}$	Peak output current	$V_O \geq V_{O(NOM)} - 5\%$	300	550		mA

Table 4. Electrical characteristics for LD3985 ($T_J = 25^\circ\text{C}$, $V_I = V_{O(NOM)} + 0.5\text{V}$, $C_I = 1\mu\text{F}$, $C_{BYP} = 10\text{nF}$, $I_O = 1\text{mA}$, $V_{INH} = 1.4\text{V}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{INH}	Inhibit input logic low	$V_I = 2.5\text{V to } 6\text{V}$, $T_J = -40 \text{ to } 125^\circ\text{C}$			0.4	V
	Inhibit input logic high		1.2			
I_{INH}	Inhibit input current	$V_{INH} = 0.4\text{V}$, $V_I = 6\text{V}$		± 1		nA
eN	Output noise voltage	$B_W = 10 \text{ Hz to } 100 \text{ KHz}$, $C_O = 1\mu\text{F}$		30		μV_{RMS}
t_{ON}	Turn On time (<i>Note 4</i>)	$C_{BYP} = 10 \text{ nF}$		100	250	μs
T_{SHDN}	Thermal shutdown	<i>Note 5</i>		160		$^\circ\text{C}$
C_O	Output capacitor	Capacitance (<i>Note 6</i>)	1		22	μF
		ESR	5		5000	$\text{m}\Omega$

- Note:
- 1 For $V_{O(NOM)} < 2\text{V}$, $V_I = 2.5\text{V}$
 - 2 For $V_{O(NOM)} = 1.25\text{V}$, $V_I = 2.5\text{V}$
 - 3 Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.
 - 4 Turn-on time is time measured between the enable input just exceeding V_{INH} High Value and the output voltage just reaching 95% of its nominal value
 - 5 Typical thermal protection hysteresis is 20°C
 - 6 The minimum capacitor value is $1\mu\text{F}$, anyway the LD3985 is still stable if the compensation capacitor has a 30% tolerance in all temperature range.

5 Typical performance characteristics

($T_J = 25^\circ\text{C}$, $V_I = V_{O(\text{NOM})} + 0.5\text{V}$, $C_I = C_O = 1\mu\text{F}$, $C_{\text{BYP}} = 10\text{nF}$, $I_O = 1\text{mA}$, $V_{\text{INH}} = 1.4\text{V}$, unless otherwise specified)

Figure 3. Output voltage vs temperature

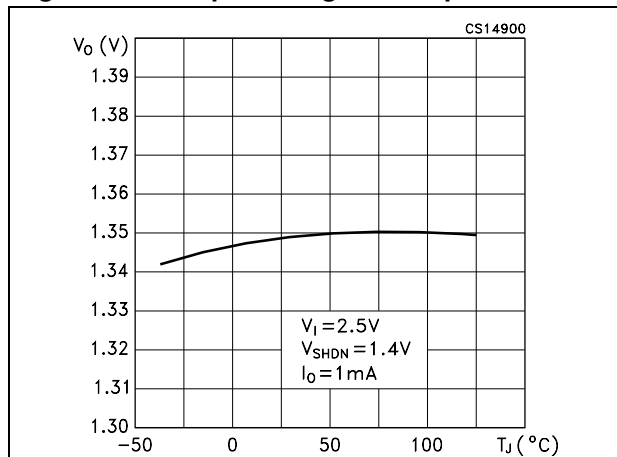


Figure 4. Output voltage vs temperature

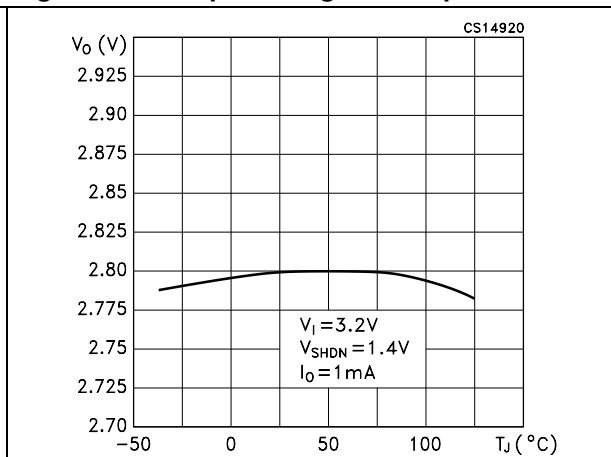


Figure 5. Output voltage vs temperature

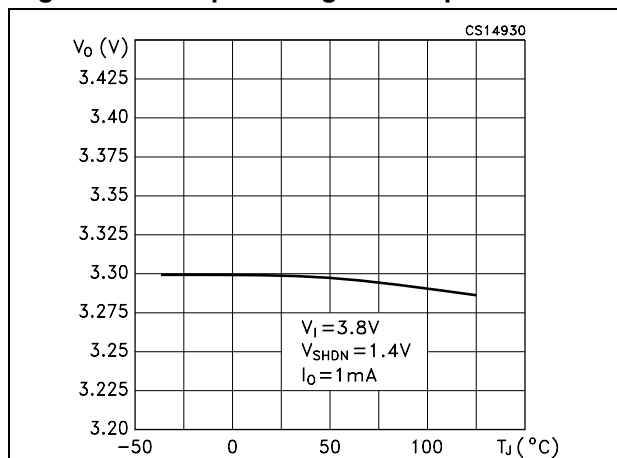


Figure 6. Shutdown voltage vs temperature

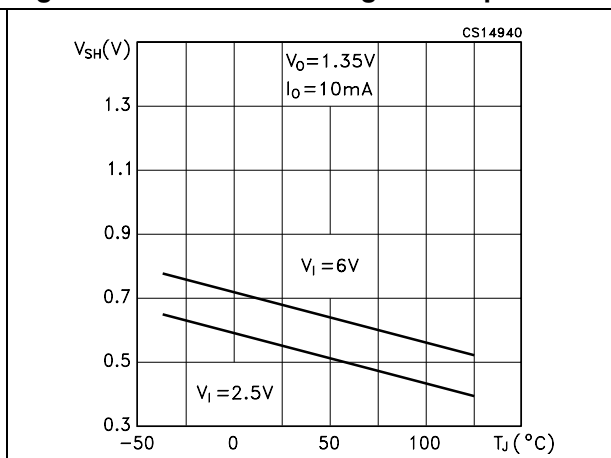


Figure 7. Shutdown voltage vs temperature

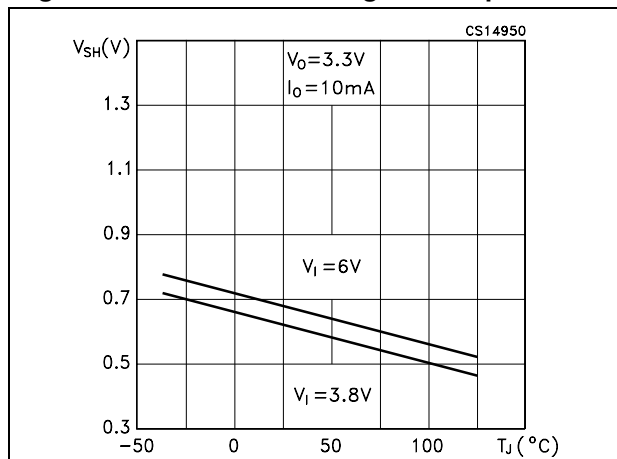


Figure 8. Line regulation vs temperature

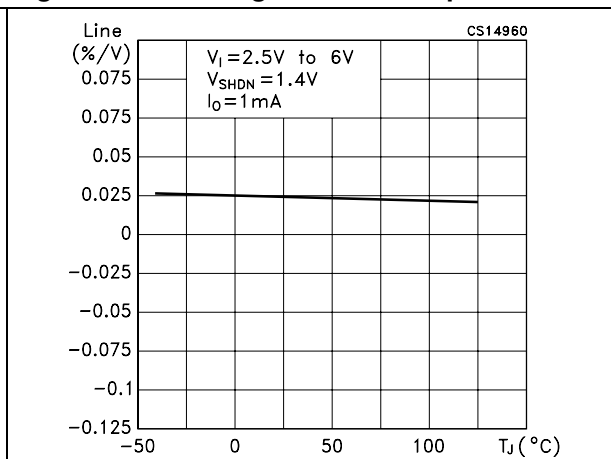


Figure 9. Line regulation vs temperature

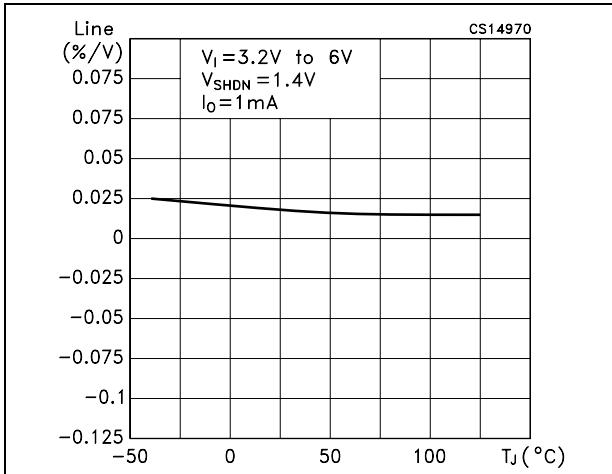


Figure 10. Line regulation vs temperature

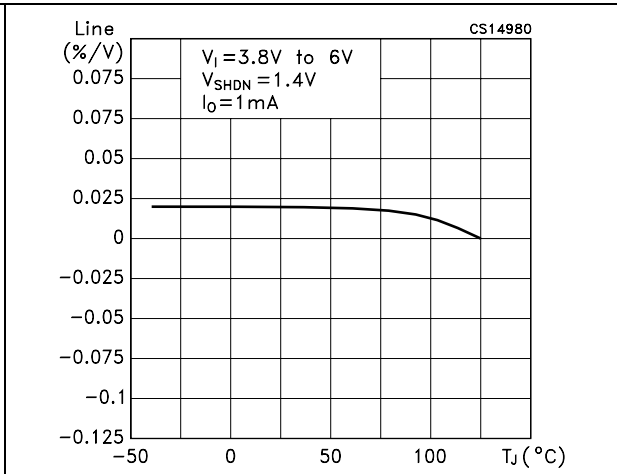


Figure 11. Load regulation vs temperature

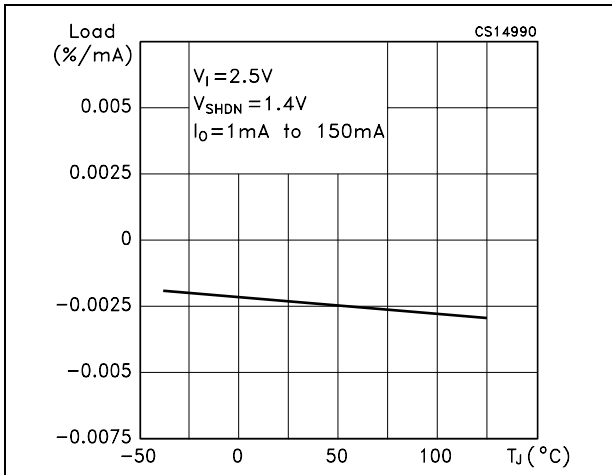


Figure 12. Load regulation vs temperature

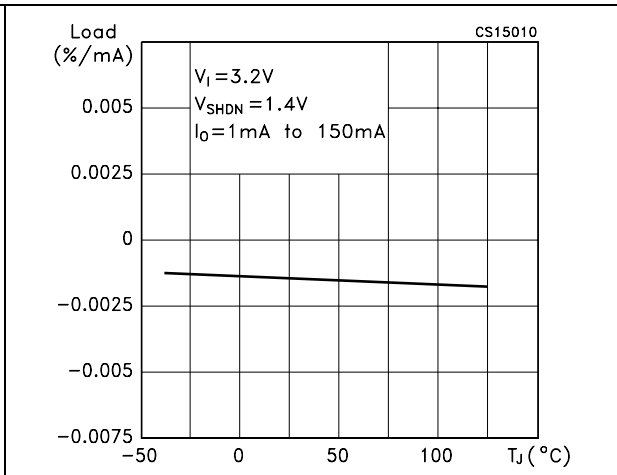


Figure 13. Load regulation vs temperature

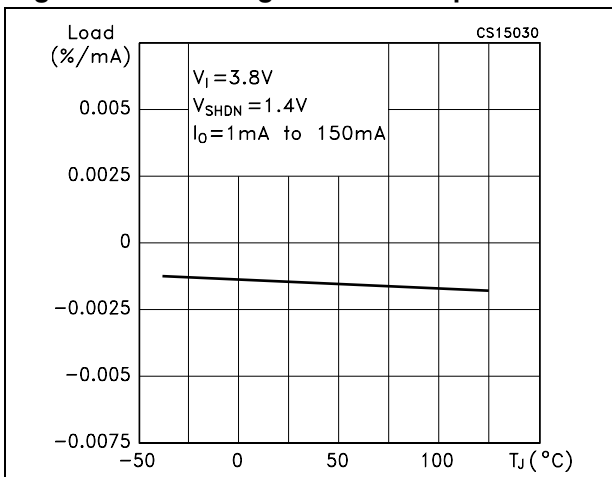


Figure 14. Quiescent current vs temperature

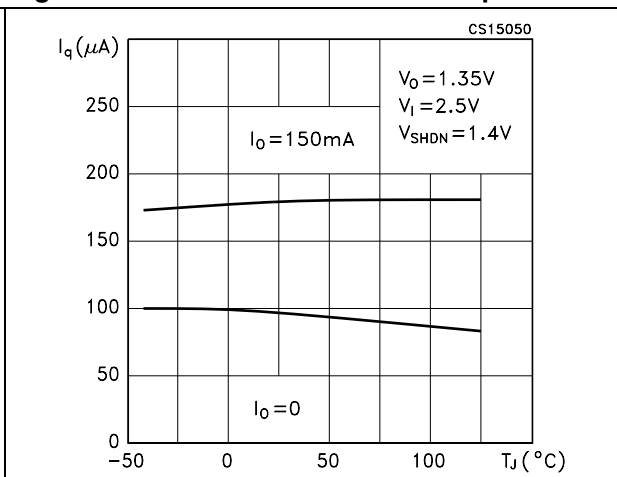


Figure 15. Quiescent current vs temperature

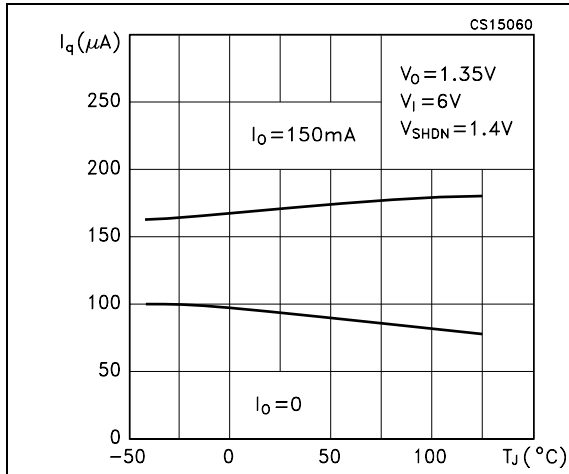


Figure 16. Quiescent current vs temperature

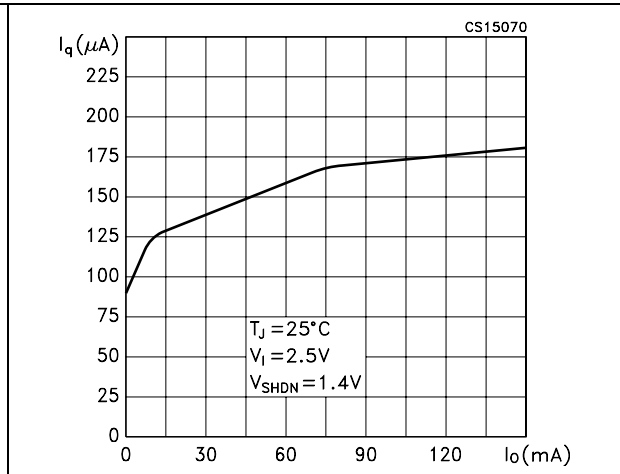


Figure 17. Supply voltage rejection vs frequency

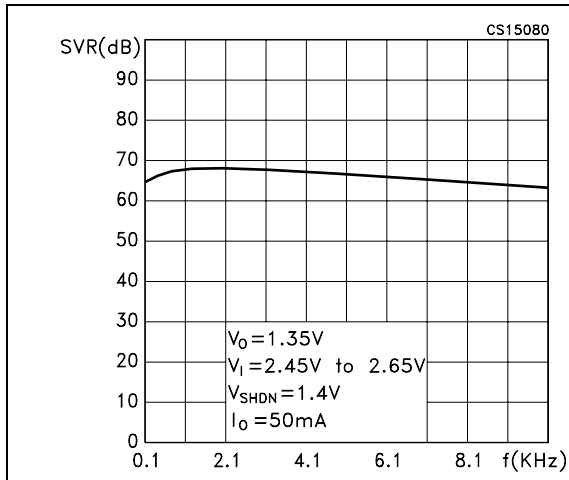


Figure 18. Load transient response

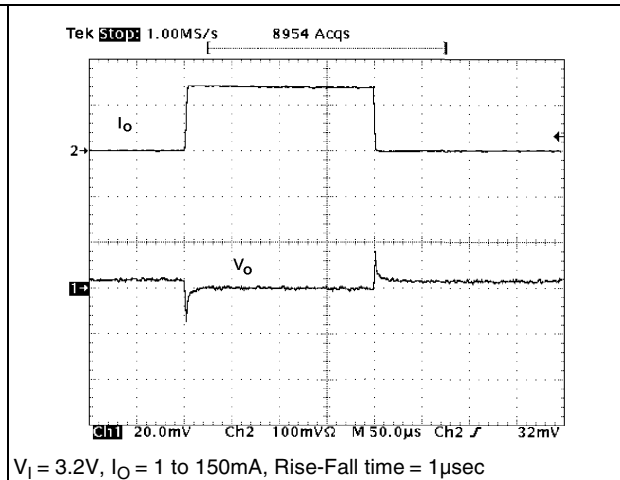


Figure 19. Line transient response

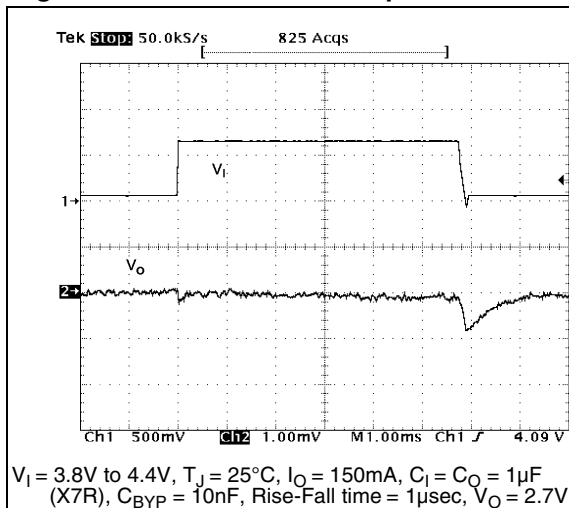


Figure 20. Start-Up

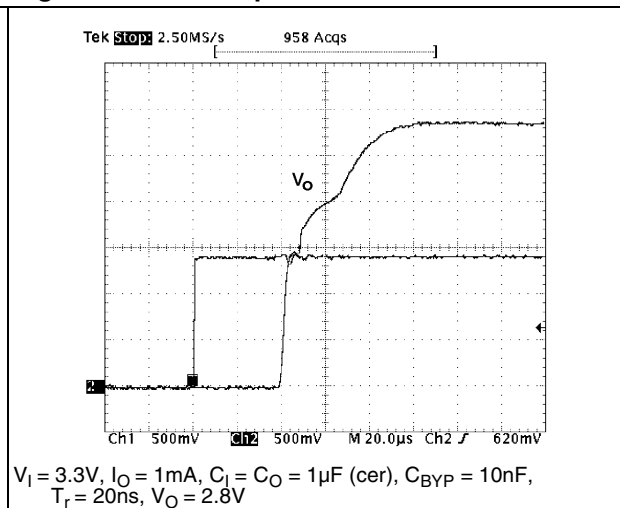
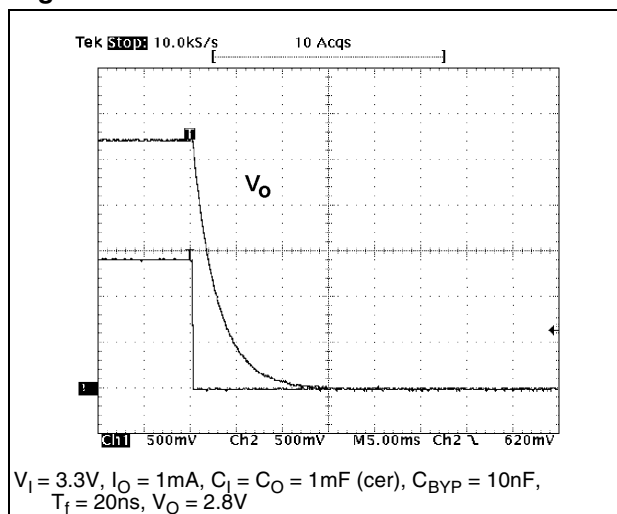


Figure 21. Turn-Off

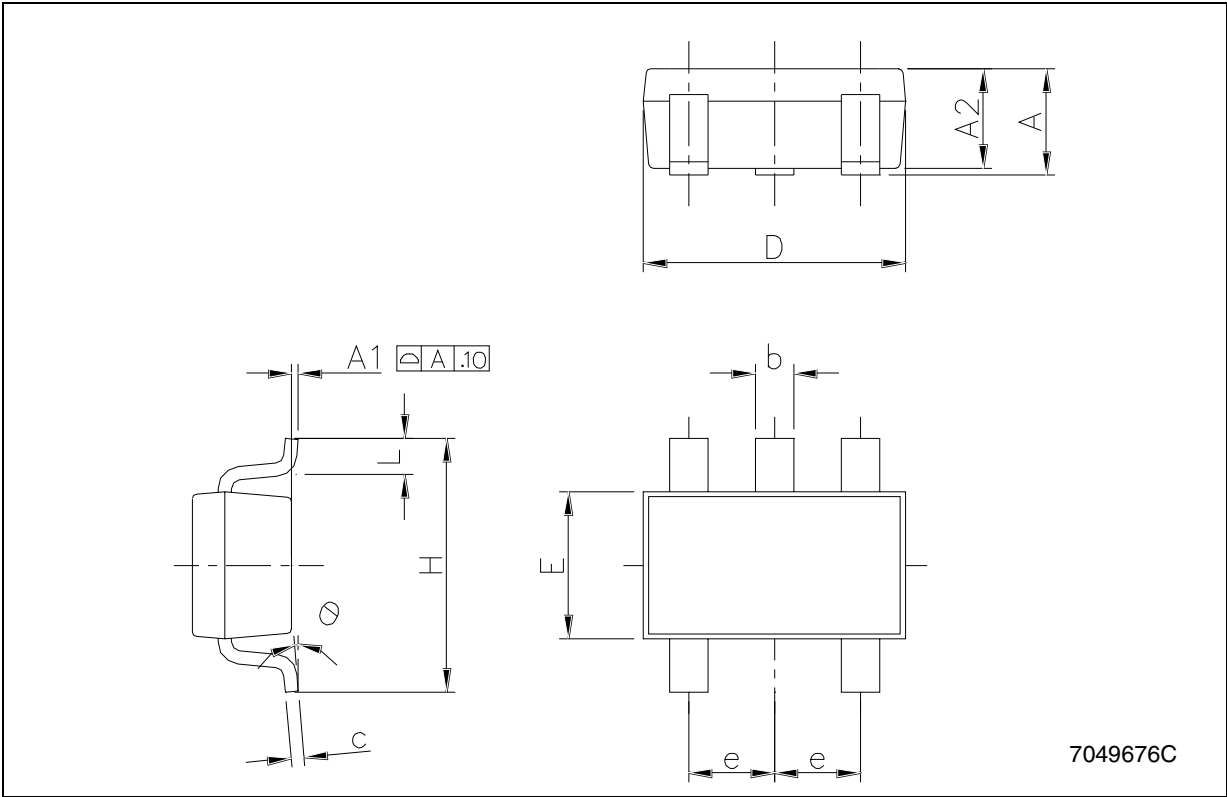


6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

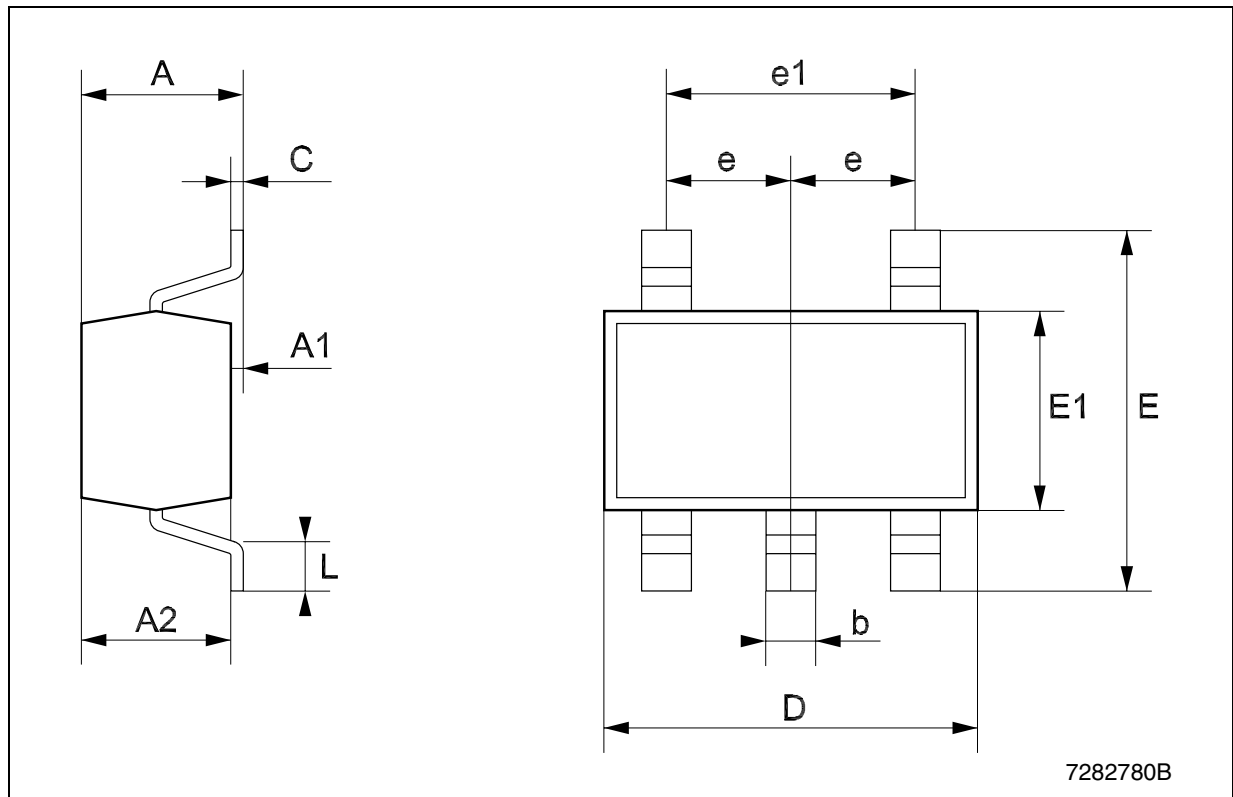
SOT23-5L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



TSOT23-5L MECHANICAL DATA

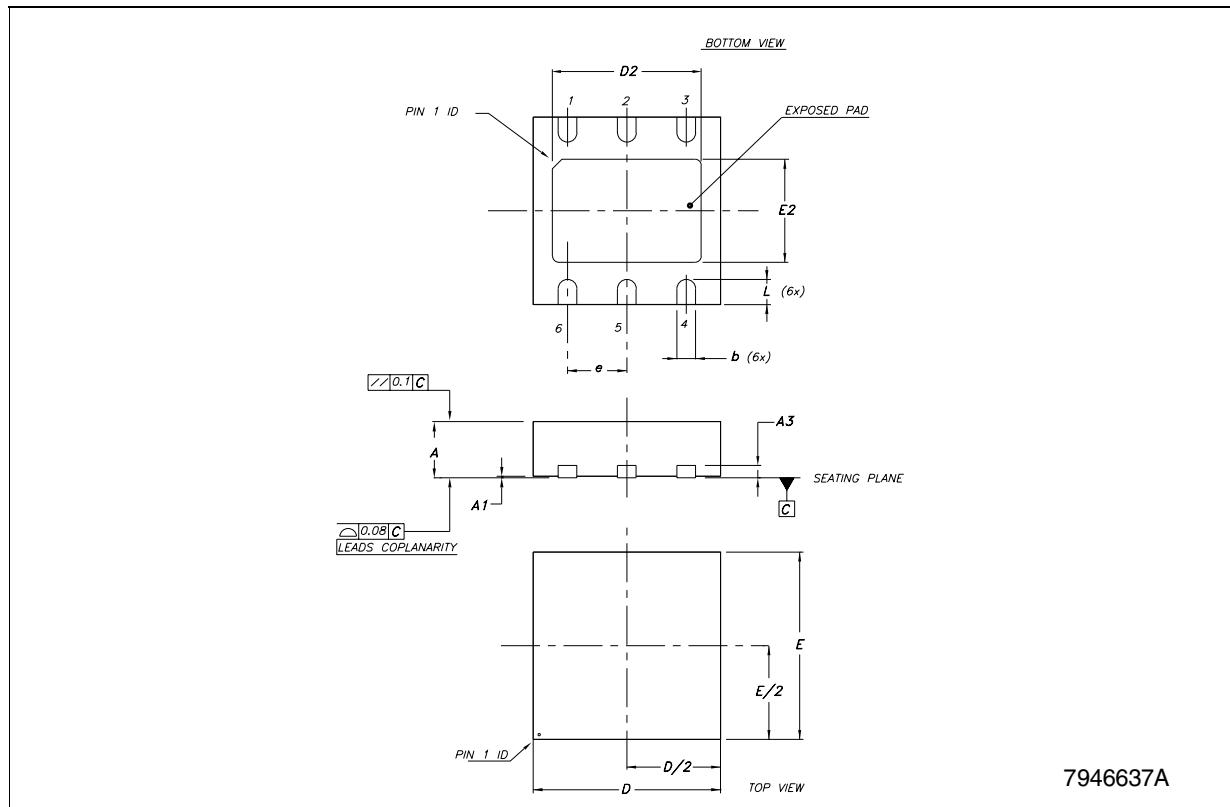
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			43.3
A1	0		0.1			3.9
A2	0.7		1.0	27.6		39.4
b	0.3		0.5	11.8		19.7
C	0.08		0.2	3.1		7.9
D		2.9			114.2	
E		2.8			110.2	
E1		1.6			63.0	
e		0.95			37.4	
e1		1.9			74.8	
L	0.3		0.6	11.8		23.6



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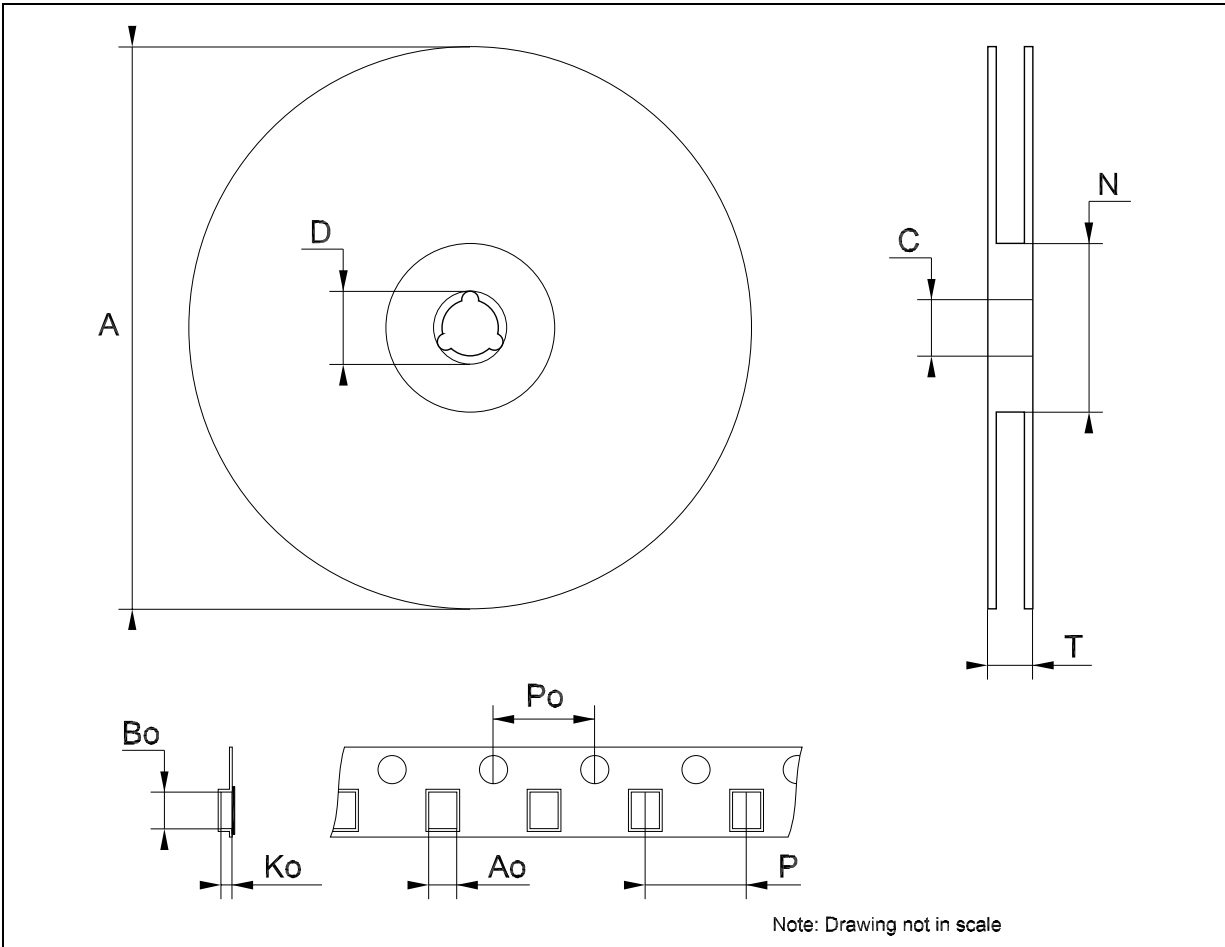
DFN6 (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23	0.30	0.38	0.009	0.012	0.015
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23	2.38	2.48	0.088	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50	1.65	1.75	0.059	0.065	0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020



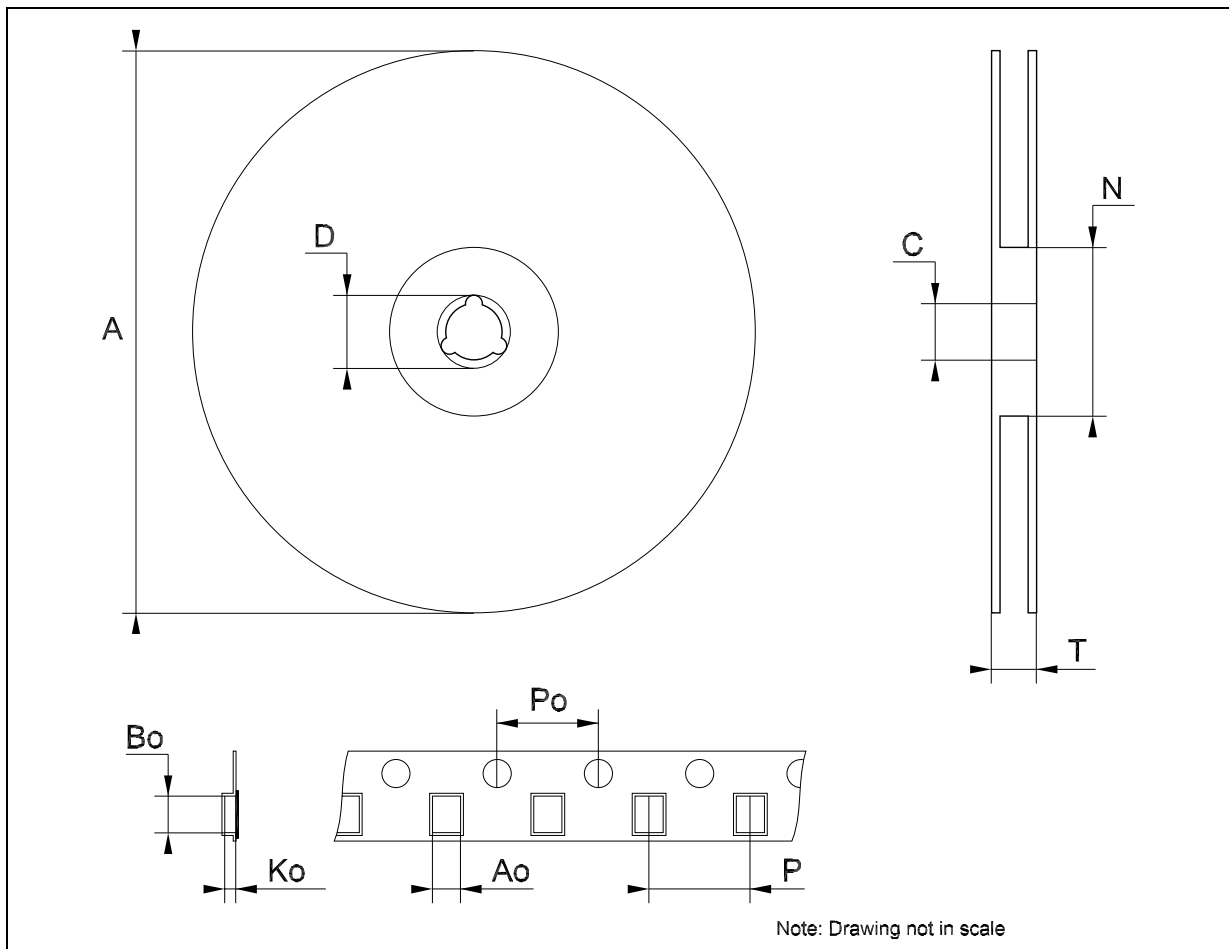
Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Tape & Reel QFNxx/DFNxx (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



7 Order codes

Table 5. Order codes

Part number			
SOT23-5L	TSOT23-5L	Flip-Chip	Output voltage
LD3985M12R ⁽¹⁾	LD3985G12R ⁽¹⁾	LD3985J12R ⁽¹⁾	1.20 V
LD3985M122R	LD3985G122R ⁽¹⁾	LD3985J122R	1.22 V
LD3985M125R ⁽¹⁾	LD3985G125R ⁽¹⁾	LD3985J125R	1.25 V
LD3985M135R ⁽¹⁾	LD3985G135R ⁽¹⁾	LD3985J135R	1.35 V
LD3985M15R	LD3985G15R ⁽¹⁾	LD3985J15R ⁽¹⁾	1.5 V
LD3985M18R	LD3985G18R	LD3985J18R	1.8 V
LD3985M20R ⁽¹⁾	LD3985G20R ⁽¹⁾	LD3985J20R ⁽¹⁾	2.0 V
LD3985M21R ⁽¹⁾	LD3985G21R ⁽¹⁾	LD3985J21R ⁽¹⁾	2.1 V
LD3985M22R ⁽¹⁾	LD3985G22R ⁽¹⁾	LD3985J22R ⁽¹⁾	2.2 V
LD3985M24R ⁽¹⁾	LD3985G24R ⁽¹⁾	LD3985J24R	2.4 V
LD3985M25R	LD3985G25R	LD3985J25R	2.5 V
LD3985M26R ⁽¹⁾	LD3985G26R ⁽¹⁾	LD3985J26R	2.6 V
LD3985M27R	LD3985G27R	LD3985J27R	2.7 V
LD3985M28R ⁽¹⁾	LD3985G28R ⁽¹⁾	LD3985J28R	2.8 V
LD3985M285R ⁽¹⁾	LD3985G285R ⁽¹⁾	LD3985J285R ⁽¹⁾	2.85 V
LD3985M29R	LD3985G29R	LD3985J29R	2.9 V
LD3985M30R ⁽¹⁾	LD3985G30R ⁽¹⁾	LD3985J30R	3.0 V
	LD3985G31R ⁽¹⁾	LD3985J31R	3.1 V
LD3985M32R ⁽¹⁾	LD3985G32R ⁽¹⁾	LD3985J32R (*)	3.2 V
LD3985M33R	LD3985G33R ⁽¹⁾	LD3985J33R	3.3 V
LD3985M44R ⁽¹⁾	LD3985G44R ⁽¹⁾	LD3985J44R ⁽¹⁾	4.4 V
LD3985M47R	LD3985G47R ⁽¹⁾	LD3985J47R	4.7 V
LD3985M48R ⁽¹⁾	LD3985G48R ⁽¹⁾	LD3985J48R	4.8 V
LD3985M49R ⁽¹⁾	LD3985G49R ⁽¹⁾	LD3985J49R ⁽¹⁾	4.9 V
LD3985M50R ⁽¹⁾	LD3985G50R ⁽¹⁾	LD3985J50R ⁽¹⁾	5.0 V

1. Available on request.

8 Revision history

Table 6. Revision history

Date	Revision	Changes
07-May-2004	6	Part number status changed on table 3.
05-Oct-2004	7	t_{ON} values are changed on table 5.
27-Oct-2004	8	Order codes changed - Table 3.
17-Mar-2005	9	Improved drawing quality for figures 19-20-21-22.
10-Apr-2007	10	Order codes has been updated and the document has been reformatted.

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