54F/74F550 • 54F/74F551

Octal Registered Transceiver With Status Flags

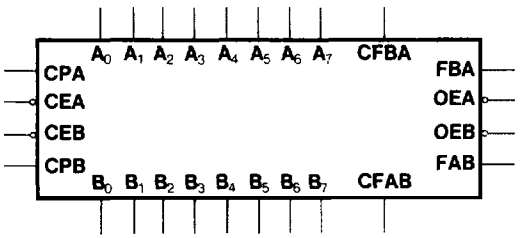
Description

The 'F550 and 'F551 octal transceivers each contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its 3-state buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

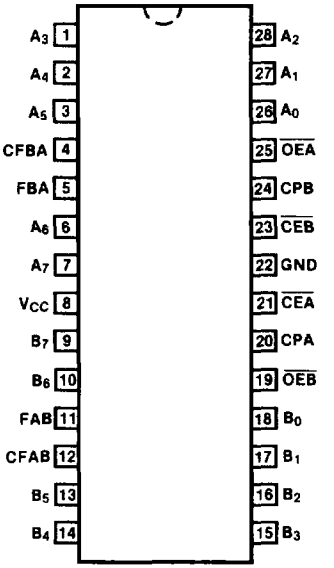
- **8-Bit Bidirectional I/O Port with Handshake**
- **Back-to-Back Registers for Storage**
- **Register Status Flag Flip-Flops**
- **Separate Edge-Detecting Clears for Flags**
- **Inverting and Non-Inverting Versions**
- **B Outputs Sink 64 mA**

Ordering Code: See Section 5

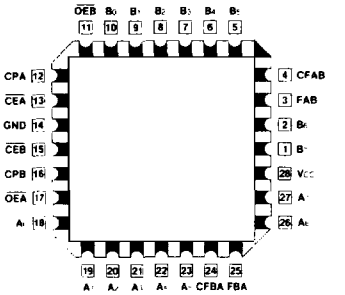
Logic Symbol



Connection Diagrams ('F550 shown*)



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

*'F551 has inverting outputs

Input Loading/Fan-Out: See Section 3 for U.L. definitions

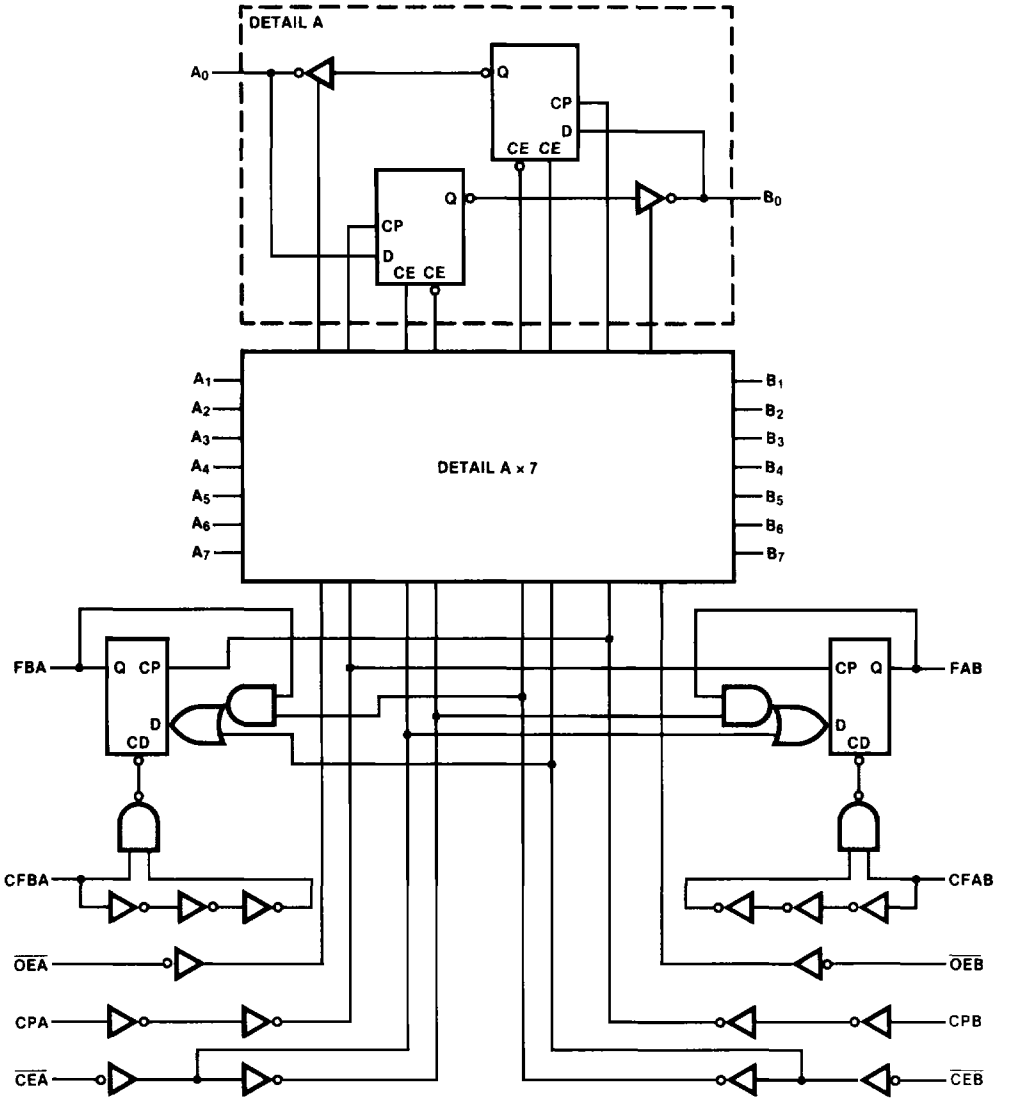
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CPA	A-to-B Clock Pulse Input (Active Rising Edge)	0.5/0.375
CPB	B-to-A Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{CEA}$	A-to-B Clock Enable Input (Active LOW)	0.5/0.375
$\overline{CEB}$	B-to-A Clock Enable Input (Active LOW)	0.5/0.375
$\overline{OEA}$	A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OEB}$	B Output Enable Input (Active LOW)	0.5/0.375
CFAB	A-to-B Flag Clear Input (Active Rising Edge)	0.5/0.5
CFBA	B-to-A Flag Clear Input (Active Rising Edge)	0.5/0.5
A_0-A_7	A-to-B Data Inputs or	1.75/0.406
	3-State B-to-A Outputs	75/15 (12.5)
B_0-B_7	B-to-A Data Inputs or	1.75/0.406
	3-State B-to-A Outputs	75/40 (30)
FAB	A-to-B Status Flag Output (Active HIGH)	25/12.5
FBA	B-to-A Status Flag Output (Active HIGH)	25/12.5

Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ($\overline{CEA}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) signal is made LOW. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH transition to the CFAB input. Optionally, the $\overline{OEA}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A flag (FBA) output HIGH. A LOW signal on $\overline{OEA}$ enables the A output buffers and a LOW-to-HIGH transition on CFBA clears the FBA flag.

Logic Diagram ('F550 shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		130	190	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	3-1 3-7
t_{PLH}	Propagation Delay CPA, CPB to FBA	3.5	6.0	8.0			3.0	9.0	ns	3-1 3-7
t_{PHL}	Propagation Delay CFAB, CFBA to FAB, FBA	5.0	9.0	11.5			4.5	13.0	ns	3-1 3-11
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	3.0 2.5	6.5 5.5	9.0 7.5			2.5 2.0	10.0 8.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n, B_n to CPA, CPB	4.0 4.0		4.5 4.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n, B_n to CPA, CPB	2.0 2.0		2.5 2.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	4.0 4.0		4.5 4.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0 2.0		2.5 2.5		
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0		3.5 3.5	ns	3-7
$t_w(H)$	Pulse Width, HIGH CFAB or CFBA	3.0		3.5	ns	3-11
t_{rec}	Recovery Time CFAB, CFBA to CPA, CPB	9.0		10.0	ns	3-11

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