

# DATA SHEET

## **BSP206**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13B

April 1995

## P-channel enhancement mode vertical D-MOS transistor

### BSP206

#### DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

#### QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain-source ON-resistance $-I_D = 200 \text{ mA}; -V_{GS} = 10 \text{ V}$	$R_{DS(on)}$	max.	6 $\Omega$
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

#### FEATURES

- Very low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

#### PINNING - SOT223

- 1 = gate
- 2 = drain
- 3 = source
- 4 = drain

#### Marking code

BSP206

#### PIN CONFIGURATION

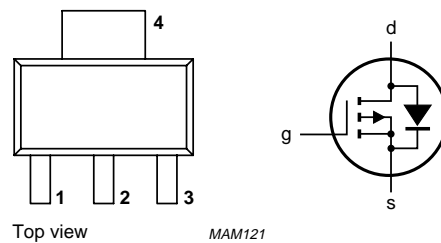


Fig.1 Simplified outline and symbol.

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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain current (peak)	$-I_{DM}$	max.	700 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ (note 1)	$P_{tot}$	max.	1.5 W
Storage temperature range	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

### THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	83.3 K/W
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### Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm<sup>2</sup>.

### CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $-I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS} = 48\text{ V}; V_{GS} = 0$	$-I_{DSS}$	max.	1.0 $\mu\text{A}$
Gate-source leakage current $\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. max.	4.5 $\Omega$ 6 $\Omega$
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ Y_{fs} $	min. typ.	100 mS 200 mS
Input capacitance at $f = 1\text{ MHz};$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{iss}$	typ. max.	55 pF 70 pF
Output capacitance at $f = 1\text{ MHz};$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{oss}$	typ. max.	30 pF 45 pF
Feedback capacitance at $f = 1\text{ MHz};$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rss}$	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_{DD} = 50\text{ V};$ $-V_{GS} = 0\text{ to }10\text{ V}$	$t_{on}$	typ. max.	4 ns 8 ns
	$t_{off}$	typ. max.	15 ns 25 ns

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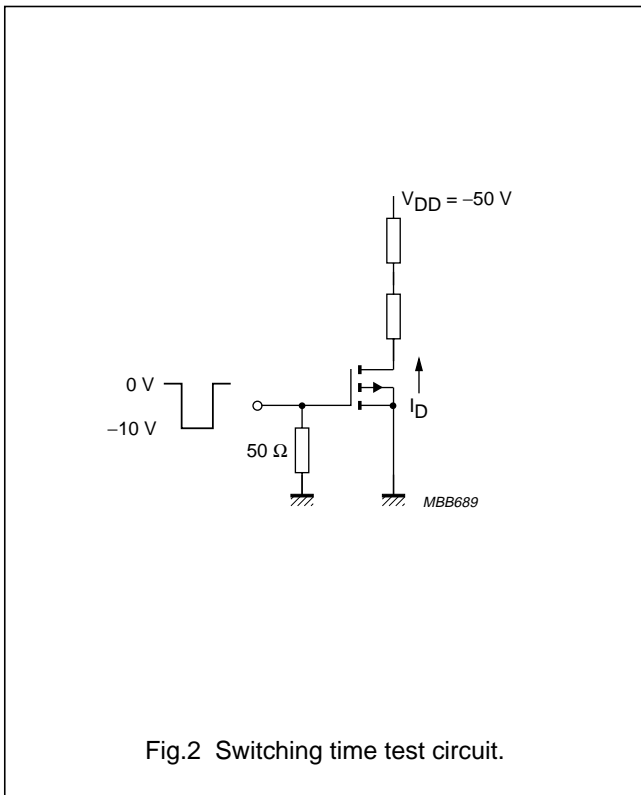


Fig.2 Switching time test circuit.

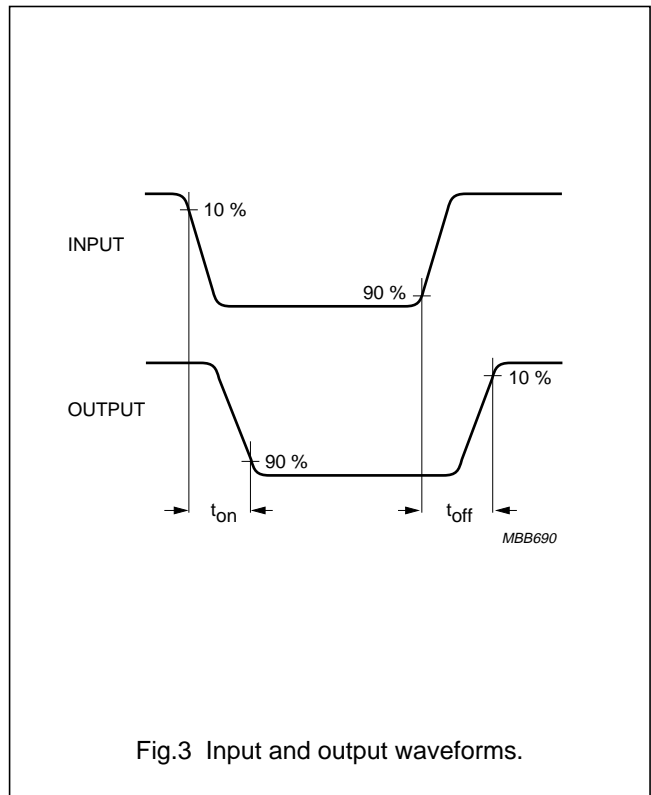


Fig.3 Input and output waveforms.

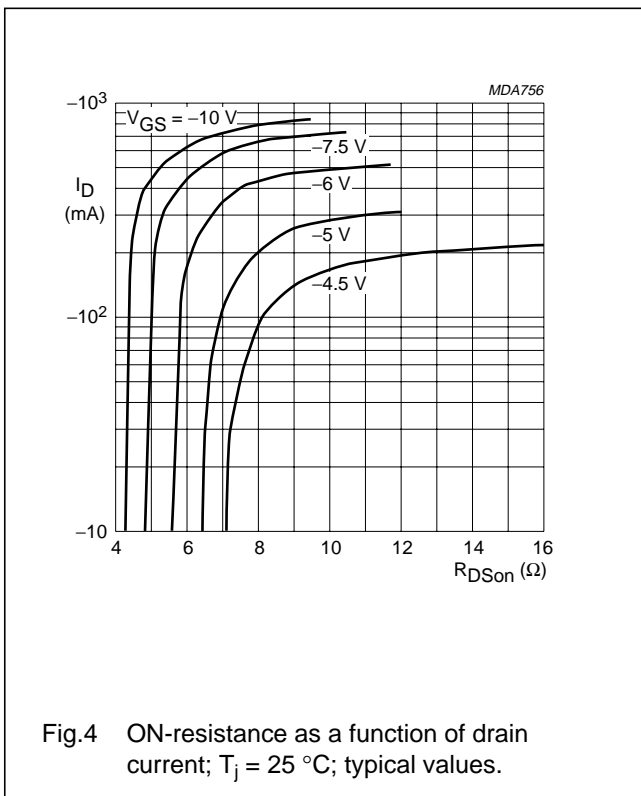


Fig.4 ON-resistance as a function of drain current;  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

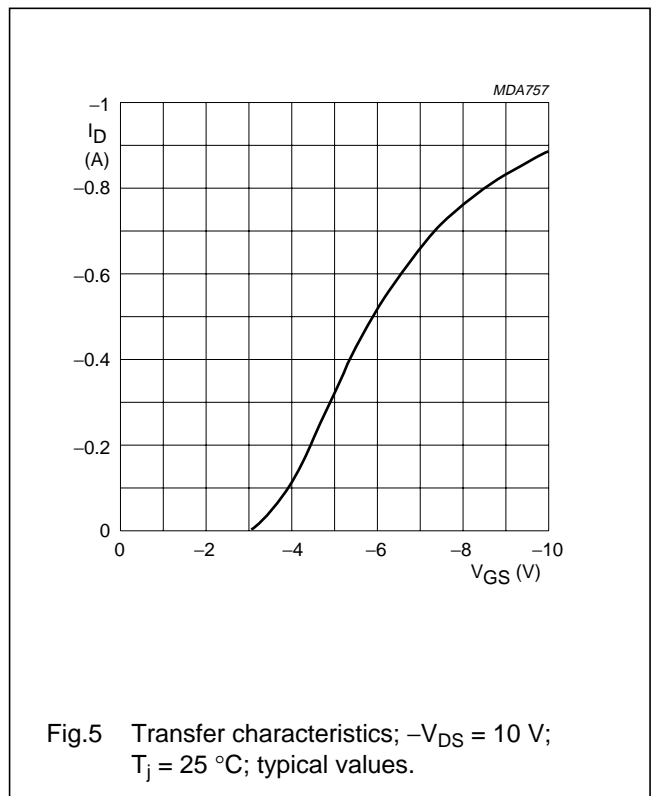
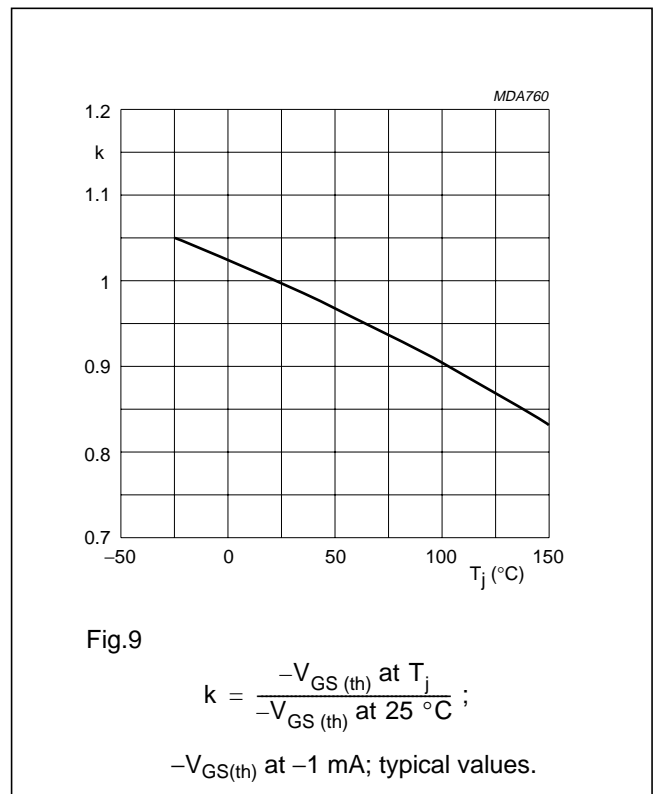
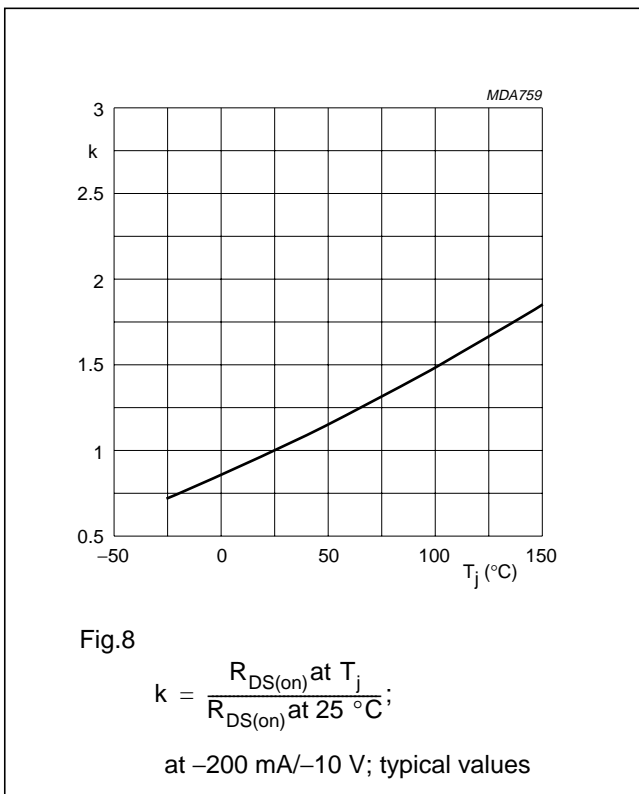
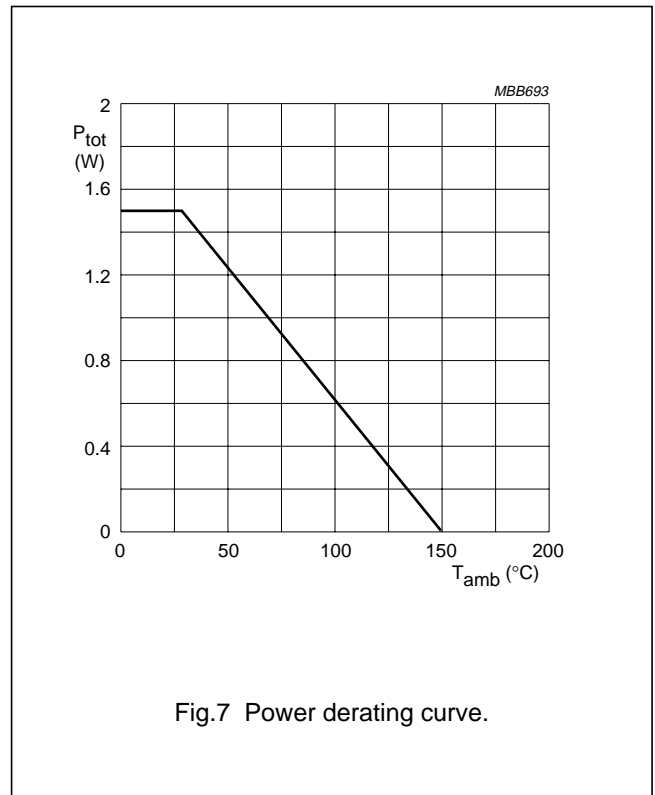
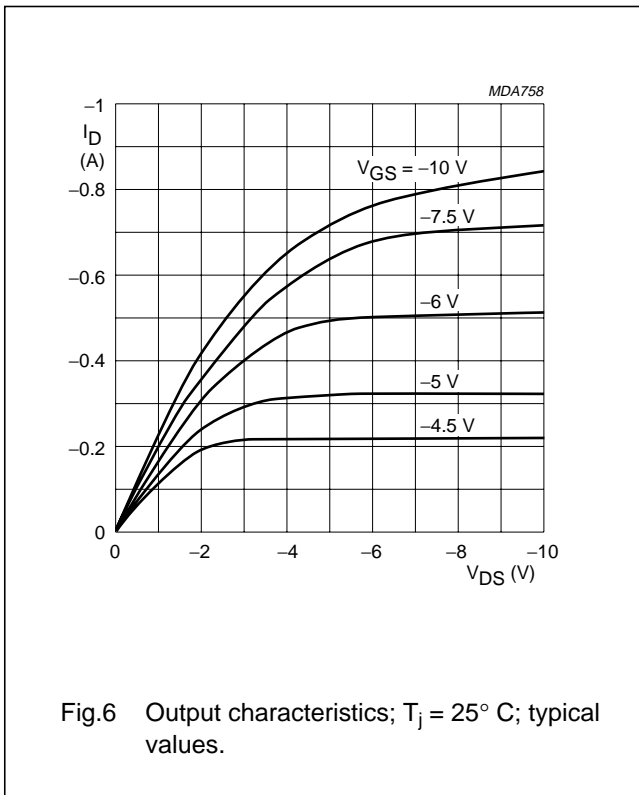


Fig.5 Transfer characteristics;  $-V_{DS} = 10\text{ V}$ ;  $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

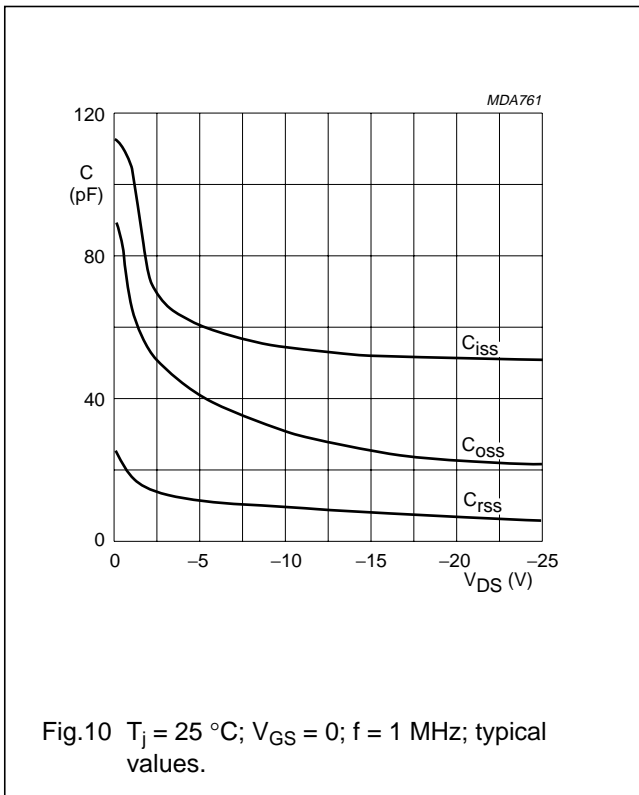
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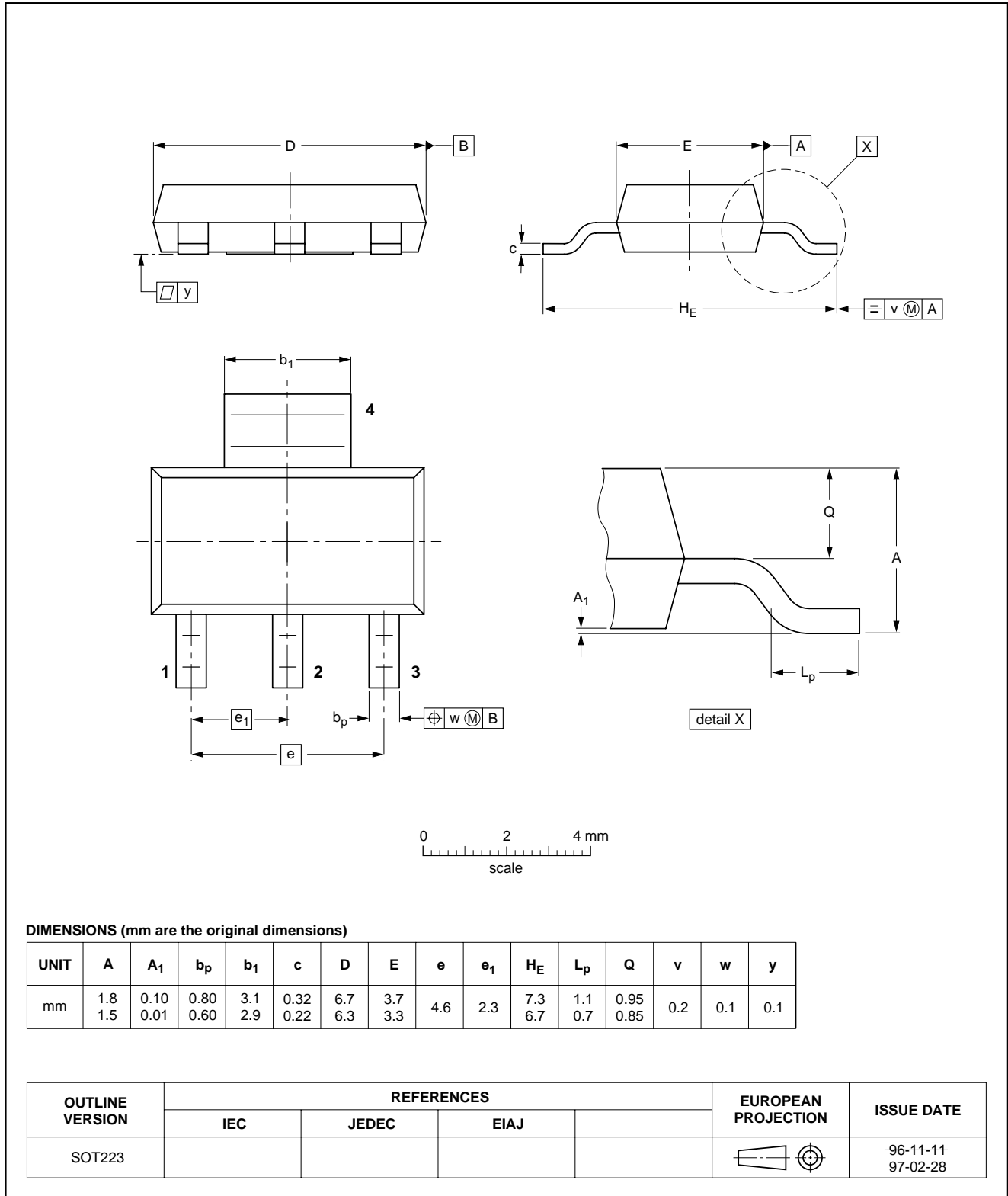
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



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**BSP206****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
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Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
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**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

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**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

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**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
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**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
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**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

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**Portugal:** see Spain

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
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**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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Printed in The Netherlands

137107/1200/01/pp12

Date of release: April 1995

Document order number: 9397 750 02481

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