ICs for Communications

ISDN DC Converter Circuit
IDCC

PEB 2023 Version 1.1

PEF 2023 Version 1.1

Data Sheet 04.99

DS 3

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1 Overview

The PEB/F 2023 is a pulse width modulator circuit designed for fixed-frequency switching regulators with very low power consumption.

In telephone and ISDN-systems a high conversion yield is crucial to maintain functionality in all supply conditions via S- or U-interfaces. The PEB/F 2023 design and technology realizes high conversion efficiency and low power dissipation. The PEB/F 2023 is fully compatible with the ITU-power recommendations of the S-interface. For these reasons the PEB/F 2023 is especially suited for telephone and ISDN-environments.

Coupled with a few external components it can provide a stable DC-supply voltage for subscriber terminals (TE's) or network terminators (NT's). Additionally other output voltages can be provided, e.g. to feed the S-lines.

It should be recognized that the PEB/F 2023 can also be used in numerous DC/DC-conversion systems other than ISDN-power supplies. For example, in a special supply voltage range the PEB/F 2023 can be supplied from a 12V battery.

For detailed technical information about **"Processing Guidelines"** and **"Quality Assurance"** for ICs, see our **"Product Overview"**.

ISDN DC Converter Circuit IDCC

PEB 2023

Version 1.1

CMOS

1.1 Features

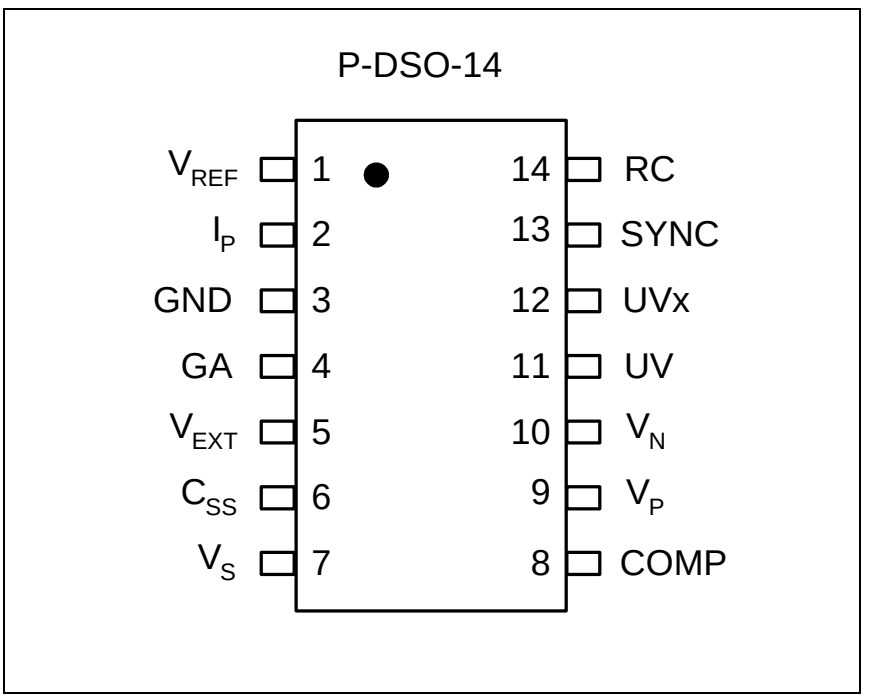
P-DSO-14

- Switched Mode DC/DC Converter
- ITU ISDN Compatible
- Low Power Dissipation
- Supply Voltage Range 0: 8V to 16V
  Supply Voltage Range 1: 12V to 80V
  Supply Voltage Range 2: 22V to 90V
  (pin striping selects between range 1 and range 2)
  Supply Voltage Range 3, with shifting by an external zener diode: U_{ZD}+8V to U_{ZD}+90V
  (minimum zener voltage U_{ZD} = 14V)
- Programmable Overcurrent Protection
- Soft Start
- Power Housekeeping Input
- Input Undervoltage Detection
- High Input Impedance (<10µA) During Undervoltage Condition
- Oscillator Synchronization Input/Output
- High Voltage Smart Power Technology 75V
- P-DSO-14/1 Package

Type	Package
PEB 2023	P-DSO-14
PEF 2023	P-DSO-14

1.2 Pin Configuration

(top view)



1.3 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1	V_{REF}	O	Output of the 4V reference voltage.
2	I_P	I	When the voltage difference between I_P and GND exceeds 100mV, the digital current limiting becomes active and turns off the external FET for the rest of this oscillator period.
3	GND	I	All analog and digital signals are referred to this pin.
4	GA	O	Output of the FET-driver.
5	V_{EXT}	I/O	Output of the internal supply. Via V_{EXT} the internal low-voltage-circuits can be supplied from an external DC-supply in order to reduce chip power dissipation. In supply voltage range 0 the positive supply voltage must be connected via a resistor to this pin.
6	C_{SS}	I	The capacitor at this pin determines the soft-start characteristic.
7	V_S	I	V_S is the positive input voltage for supply voltage range 1, 2 and 3. Must be connected to GND via a resistor when using supply voltage range 0.
8	COMP	O	Error amplifier output and **P**ulse **W**idth **M**odulator (PWM) input for loop stabilization network.
9	V_P	I	Non-inverting input of the error amplifier.
10	V_N	I	Inverting input of the error amplifier.
11	UV	I	Input undervoltage lockout. The input undervoltage lockout level depends on the used supply voltage range. Must be connected to pin V_S when using supply voltage range 0.
12	UVx	I	If this pin is connected to UV, then supply range 1 is selected. If this pin is not connected (floating), then supply range 2 or supply range 3 can be used. Must be connected to pin V_{EXT} when using supply voltage range 0.
13	SYNC	I/O	Input for synchronization of the oscillator to an external frequency, or output to synchronize multiple devices.
14	RC	I	The external timing components of the ramp generator are attached to this pin.

1.4 Functional Block Diagram

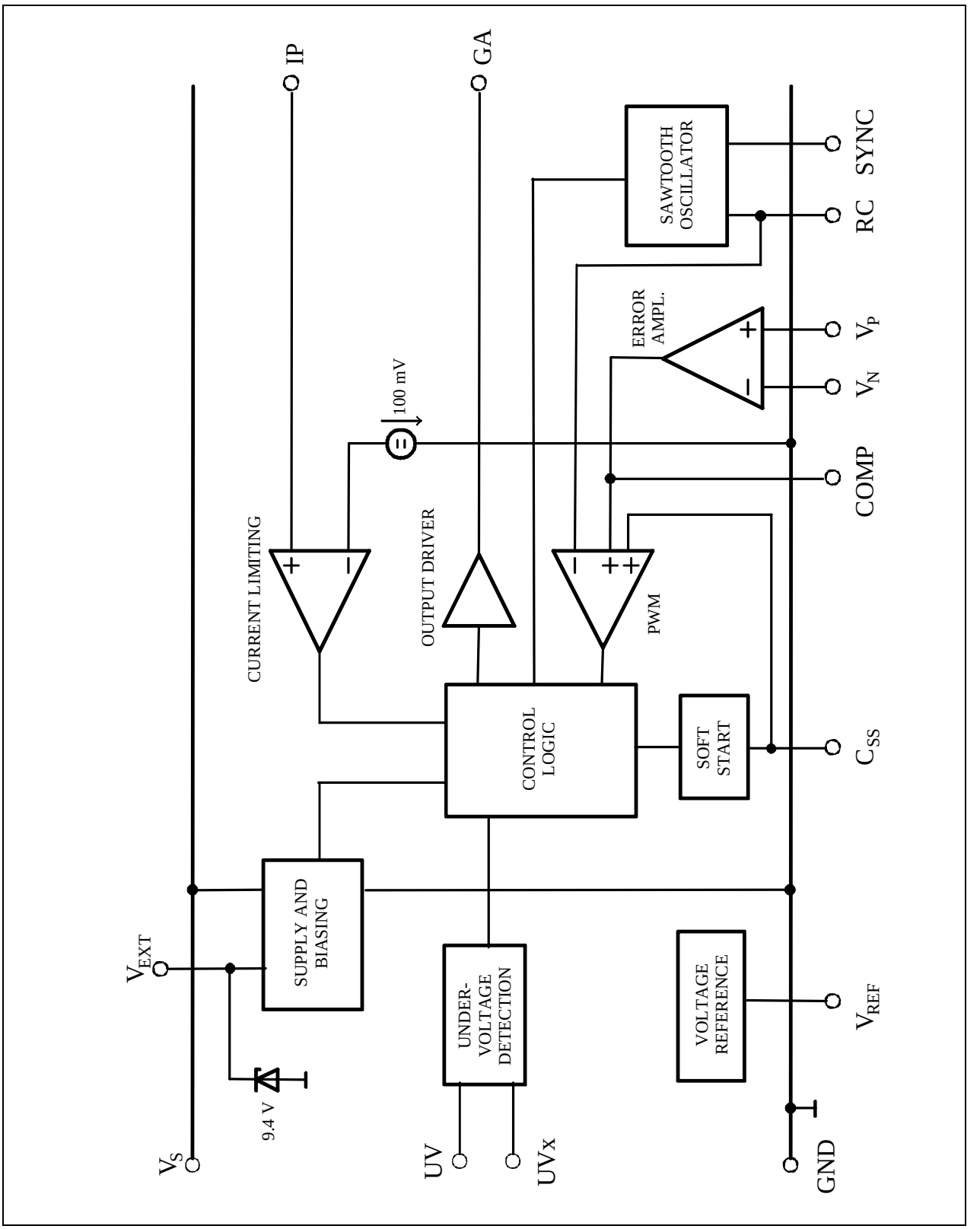


Figure 1 Block Diagram

1.5 System Integration

Figure 2 shows an example out of the wide application field of the PEB/F 2023. In network termination applications, the PEB/F 2023 supplies the internal IC's directly from the U–interface. If the local main supply of the NT is out of order, then the PEB/F 2023 will also supplies the S-interface (restricted power mode).

In the subscriber terminal the PEB/F 2023 is used for feeding the internal circuits.

The PEB/F 2023 accommodates both galvanically isolated and non-isolated configurations. Considering the diversity of DC/DC-converter applications, this part of the specification only shows how to use the special ISDN-features of the PEB/F 2023.

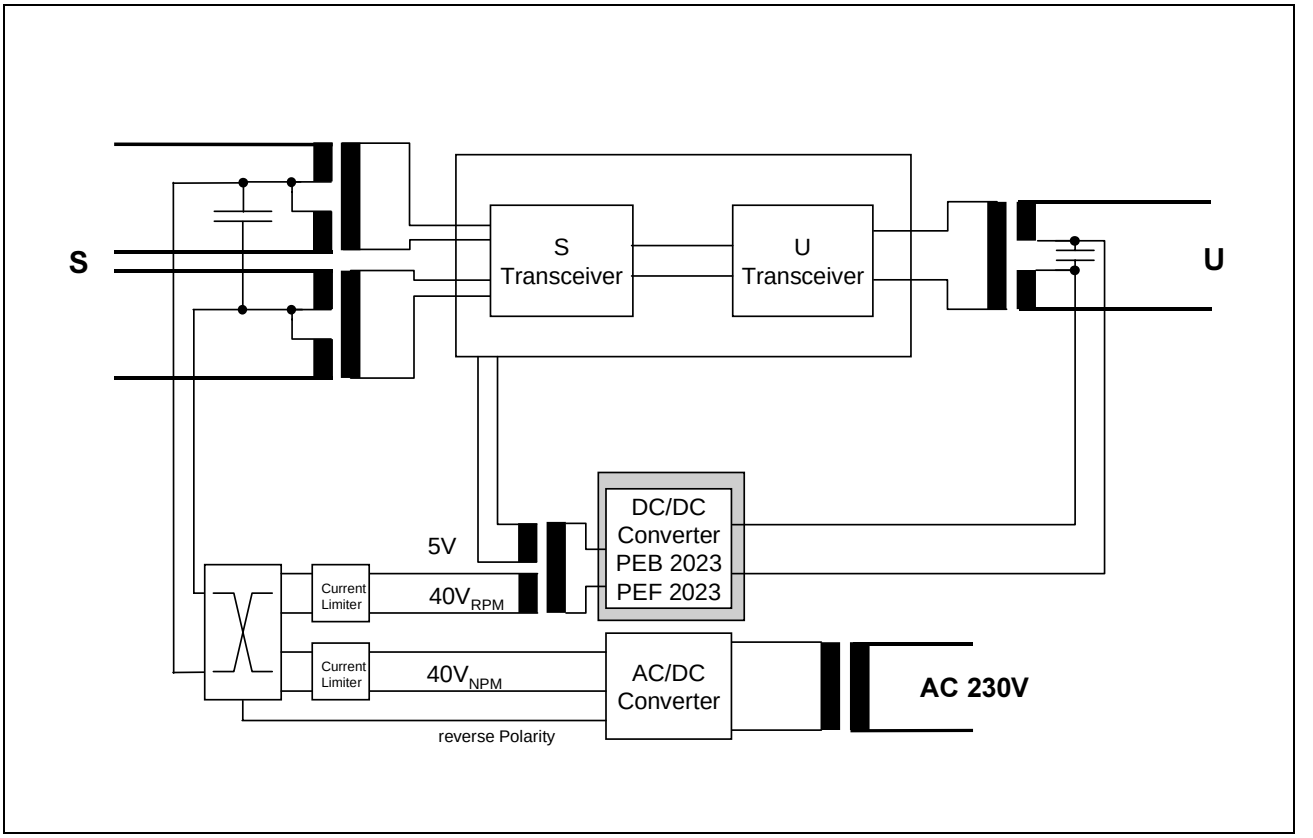


Figure 2 PEB/F 2023 in ISDN-Concept

Figure 3 shows the PEB/F 2023 in flyback configuration with transformer isolation using supply voltage range 3. This application circuit is used to supply the internal IC's of the NT from the U-interface and also to supply the S-interface in case of restricted power mode. The DC/DC-converter begins operating when the input voltage exceeds 38V (U_{ZD}+8V, see supply voltage range 3). In the start-up phase the PEB/F 2023 is supplied through V_S. After this start-up phase, the PEB/F 2023 is supplied via V_{EXT} (power housekeeping input) and the DC/DC-converter will operate until the input voltage falls below 20V (input undervoltage detection). For power saving reasons the value of resistor R_6 is as high as possibile.

The maximum static V_{IN} input voltage in this example is 120V. How to get a higher maximum dynamic V_{IN} input voltage see chapter „1.6 Surge Protection“ on pages 14 and 15.

To get a very fast input undervoltage detection see chapter „1.7 Fast Input Undervoltage Detection“ on page 15.

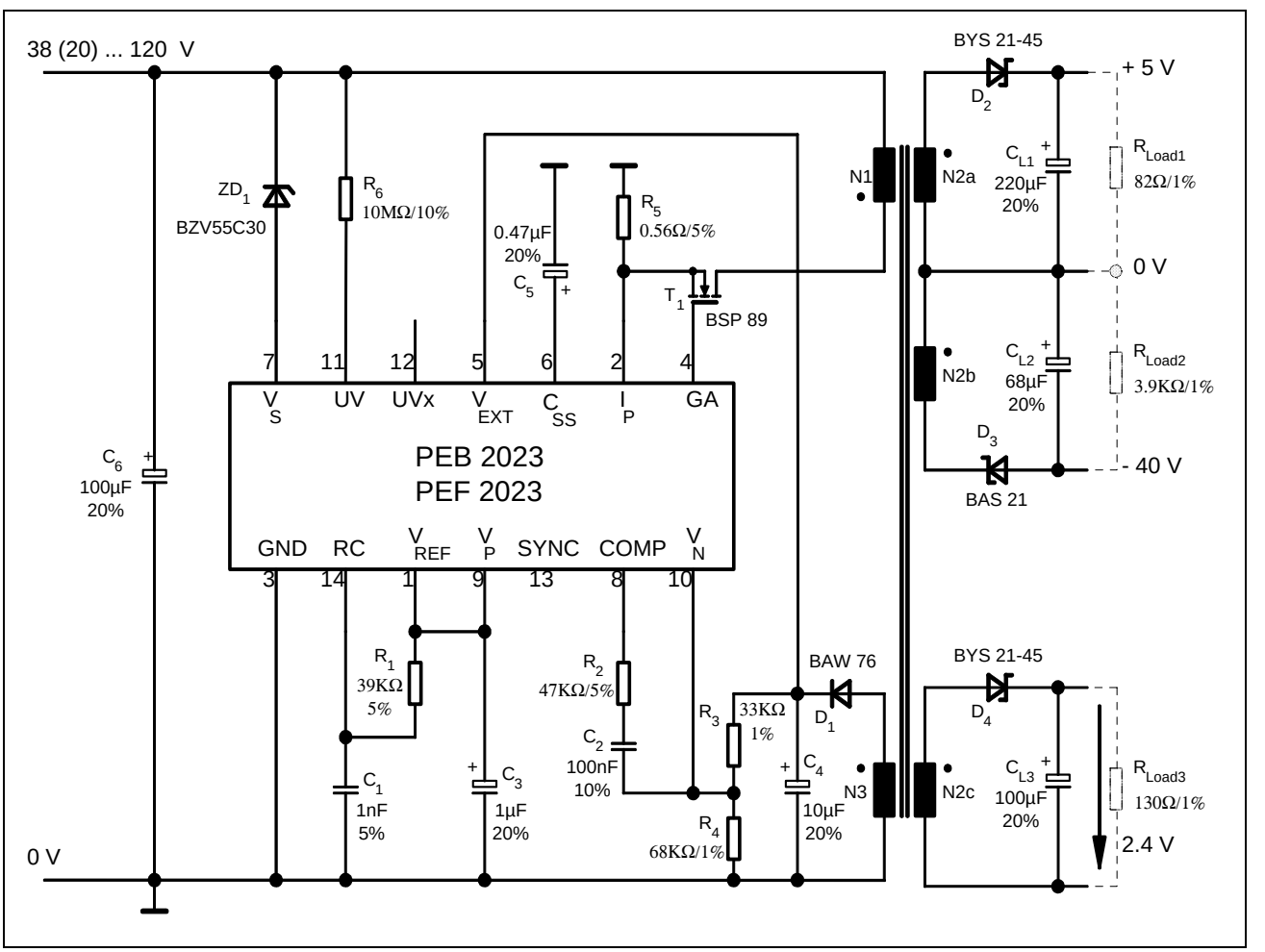


Figure 3 PEB/F 2023 in Flyback Configuration with Transformer Isolation

Figure 4 shows the PEB/F 2023 in a non-isolated minimum configuration by using supply voltage range 1 (for this input voltages also supply voltage range 2 is possible). The voltage drop over R_6 is the difference between input voltage and undervoltage detection level. To get low power dissipation the value of resistor R_6 should be as high as possibile. The minimum current through R_6 is about 100nA, the maximum current is 1mA (see absolute maximum ratings).

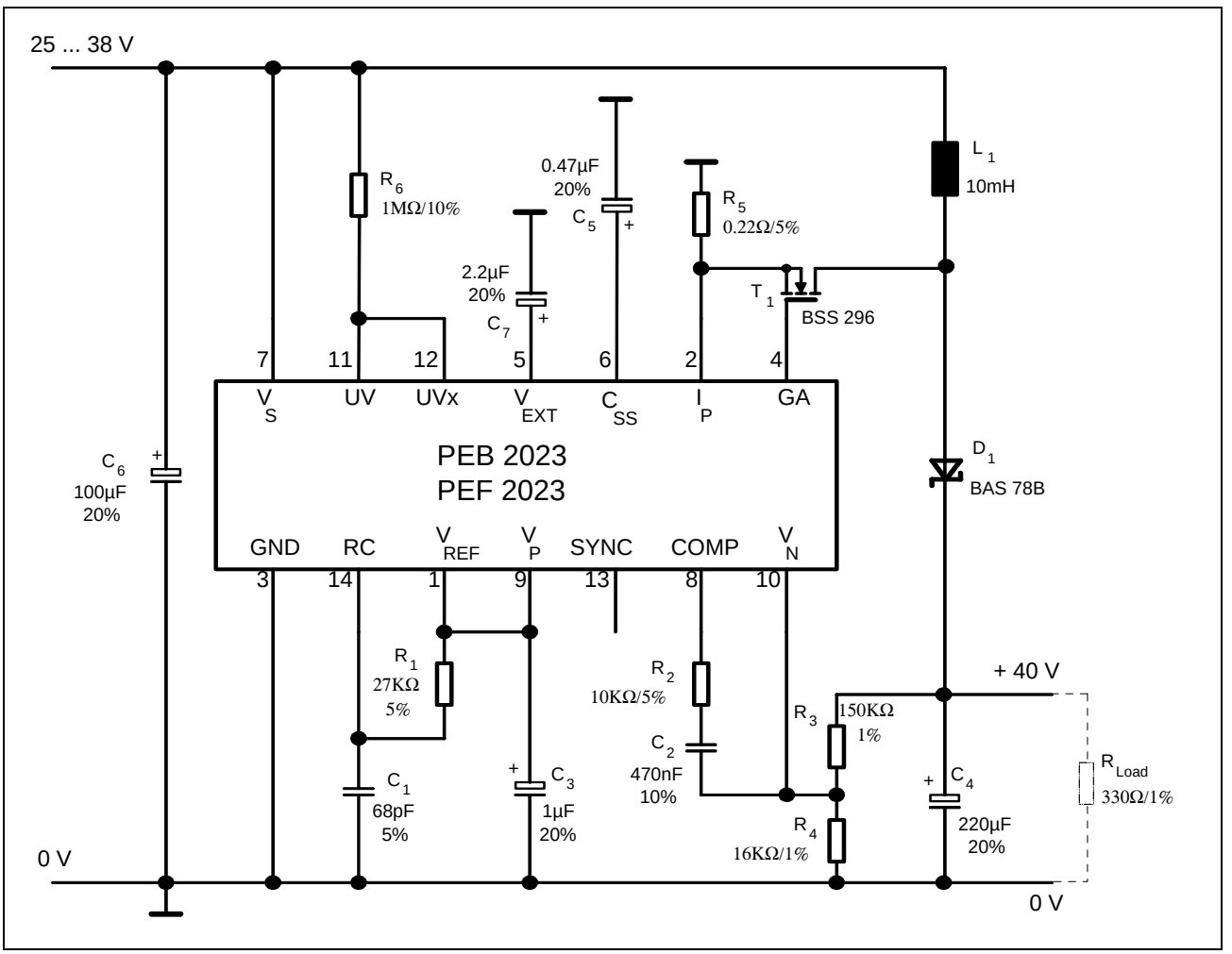


Figure 4 PEB/F 2023 in a non-isolated Minimum Configuration

Figure 5 shows the PEB/F 2023 in a non-isolated flyback configuration with transformer using supply voltage range 0. The voltage drop over R_6 is V_{EXT}-1V. To get low power dissipation the value of resistor R_6, should be as high as possibile. For calculating the value of resistor R_6 the minimum current through R_6 is about 100nA and the maximum current is about 100µA.

For calculation of resistor R_7:

V_{IN}, input voltage : V_{INmin} = 8V, V_{INmax} = 16V
V_{EXT} : V_{EXTmin} = 6V, V_{EXTmax} = 9V
I_{R7}, input current : I_{R7min} = 1mA, I_{R7max} = 6mA

$$R_{7min} = \frac{V_{INmax} - V_{EXTmax}}{I_{R7max}} = 1,667k\Omega \qquad R_{7max} = \frac{V_{INmin} - V_{EXTmin}}{I_{R7min}} = 2k\Omega$$

To get lower power dissipation the value of resistor R_7 should also be as high as possibile. For this reason we use R_{7max}. If in the calculation above R_{7min} is higher than R_{7max}, then the input voltage range is not correct; V_{INmax}-V_{INmin} is too large.

Note: If V_{INmin} = 6V and V_{INmax} = 9V then the resistor R_7 is not necessary. The input voltage V_{IN} can directly be connected to V_{EXT}.

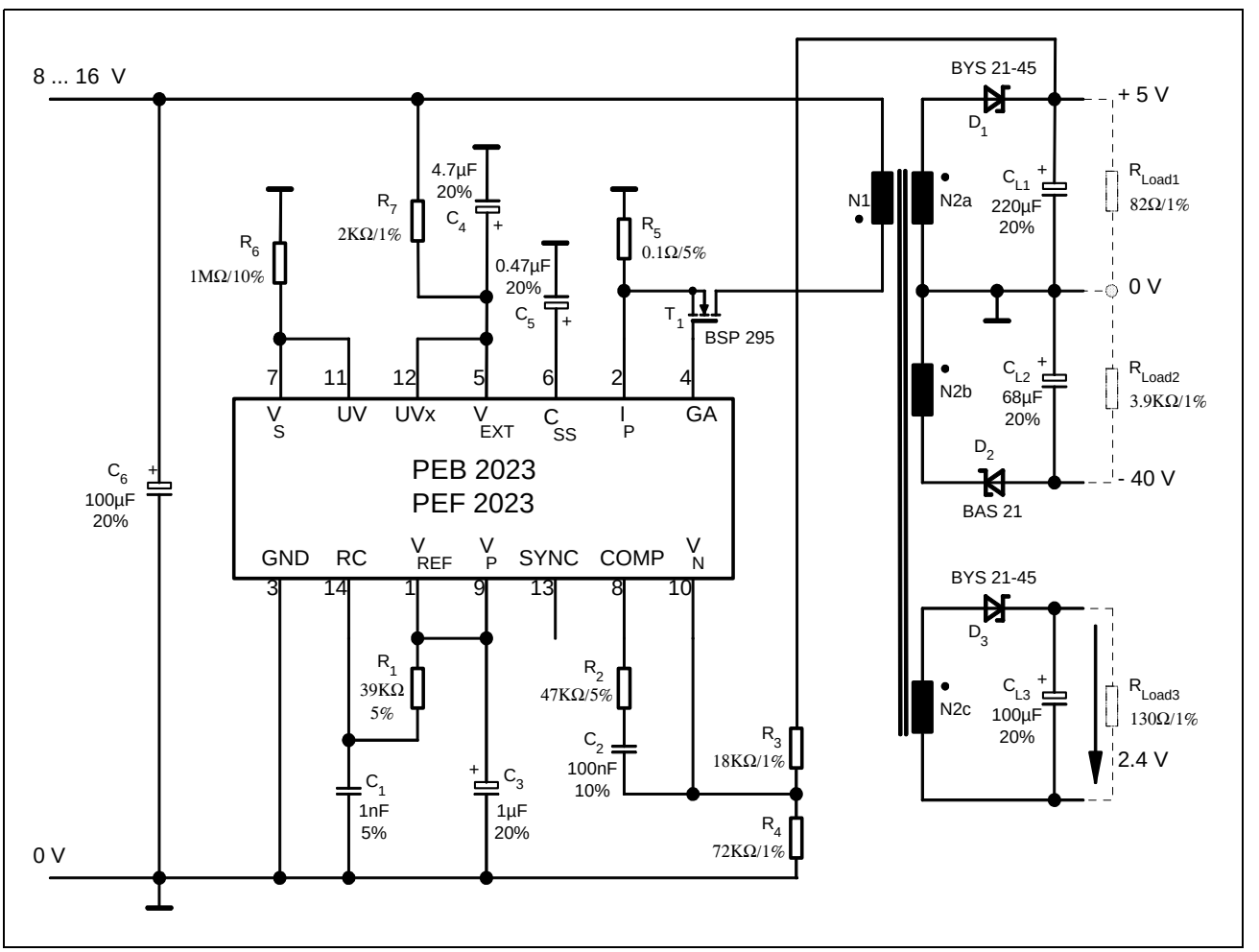


Figure 5 PEB/F 2023 in a non-isolated Flyback Configuration

1.6 Surge Protection

In telephone and ISDN-systems the topic “surge protection“ or “lightning overvoltage protection“ is very important. For the PEB/F 2023 overvoltage protection is necessary when the DC/DC converter input voltage V_{IN} is connected to the U- or S-interface-lines.

Figure 6 shows how to protect the PEB/F 2023 when using supply voltage range 3 (see also figure 3). For supply voltage ranges 1 and 2 the principle is the same.

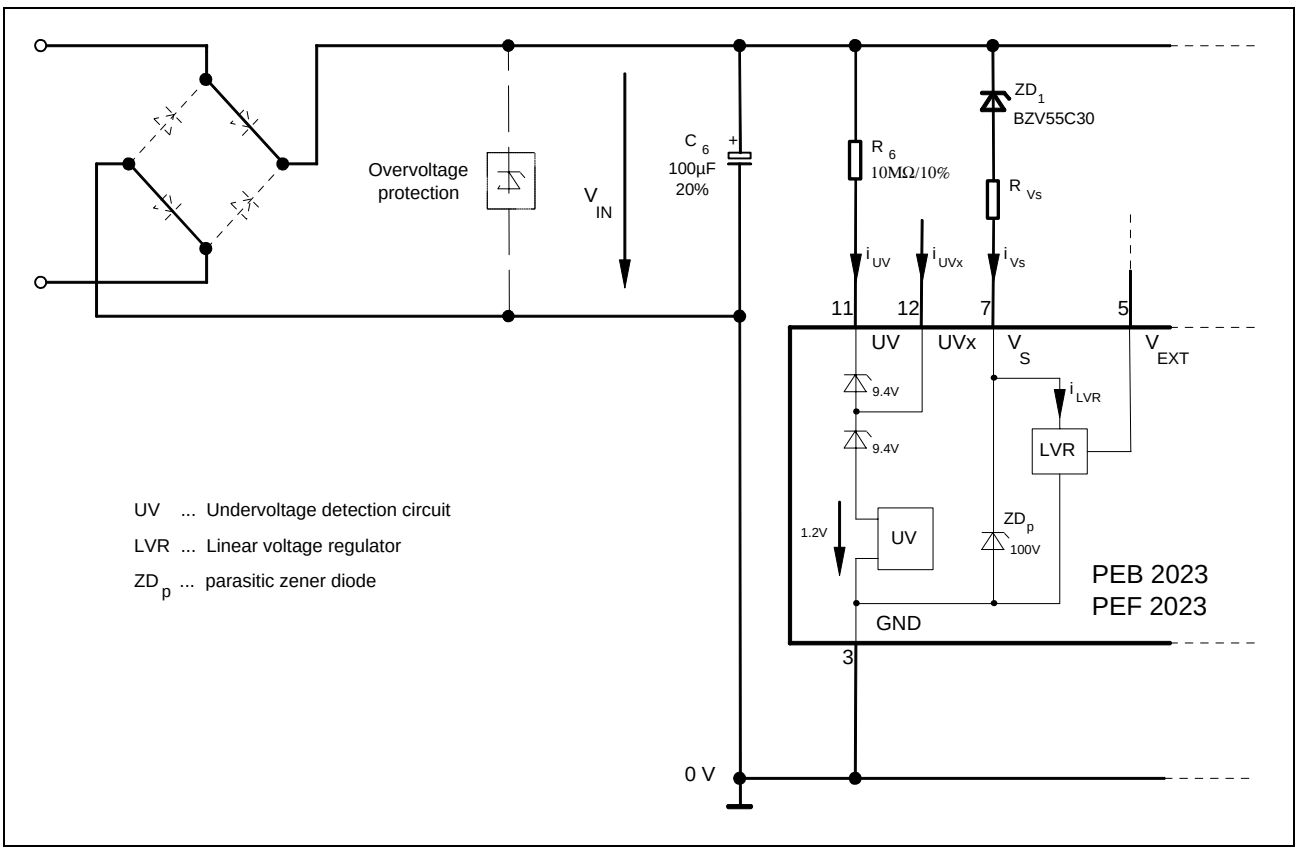


Figure 6 PEB/F 2023 Surge Protection

The DC/DC converter begins operating when the input voltage exceeds V_{ZD1}+8V+V_{RVs}. In the start-up phase the PEB/F 2023 is supplied through V_S. After this start-up phase, the PEB/F 2023 is supplied via V_{EXT} (power housekeeping input, see figure 3) and the DC/DC-converter will operate until the input voltage falls below 20V (input undervoltage detection).

The current i_{LVR} needed in the start-up phase is less than 500µA. With this current and the value of resistor R_{Vs} the voltage V_{RVs} can be calculated.

For static and transient currents i_{UV} and i_{UVx}, respectively, absulote maximum ratings are valid. Because of the high value of R_6 (for power saving reasons), i_{UV} and i_{UVx} normally are sufficiently low.

Limits for voltage and current on pin V_S are also defined in the maximum ratings.

Calculation example: figure 6 with R_{Vs} = 4,7kΩ

$$V_{INstart} = V_{ZD1} + 8 + (R_{Vs} \cdot i_{LVR}) = 30V + 8V + (4{,}7k\Omega \cdot 500\mu A) = 40{,}35V$$

for t ≤ 100msec:

$$V_{INmax} = V_{ZD1} + 100 + (R_{Vs} \cdot i_{Vsmax}) = 30V + 100V + (4{,}7k\Omega \cdot 10mA) = 177V$$

for t ≤ 10msec:

$$V_{INmax} = V_{ZD1} + 100 + (R_{Vs} \cdot i_{Vsmax}) = 30V + 100V + (4{,}7k\Omega \cdot 30mA) = 271V$$

In this example the DC/DC converter begins operating when the input voltage exceeds 40,35V. The maximum transient input voltage is 177V / 271V for a duration of 100msec / 10msec. The maximum static input voltage is given by V_{ZD1} + 90V = 120V, see absolute maximum ratings.

1.7 Fast Input Undervoltage Detection

With three extra devices (D_5, D_6 and R_8, see **figure 7**) an undervoltage state on the input can be detected faster than the voltage on capacitor C_6 decreases. See also chapter „undervoltage lockout“ on page 17.

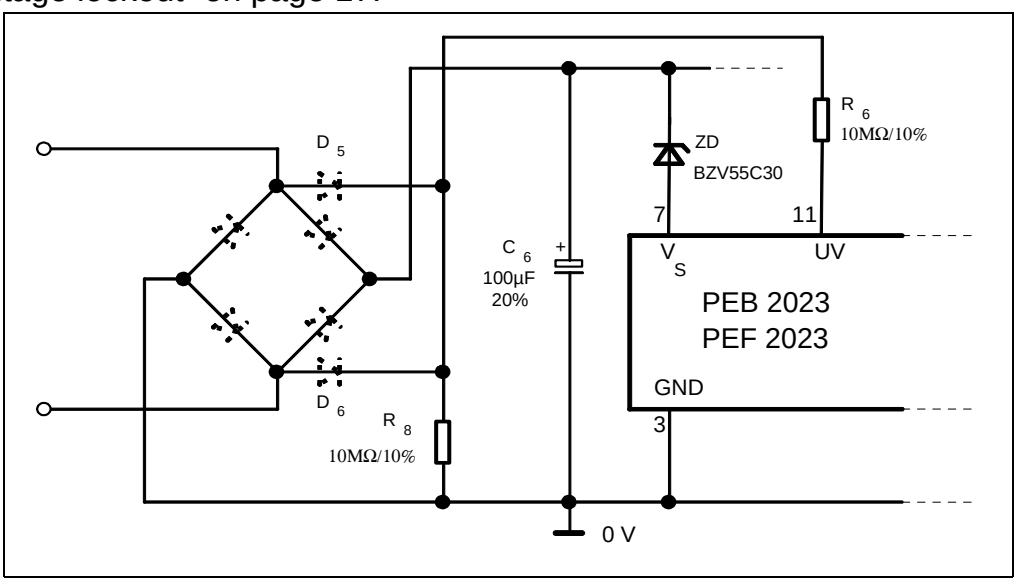


Figure 7 PEB/F 2023, Fast Input Undervoltage Detection

2 Functional Description

The PEB/F 2023 contains the following functional blocks:

- Supply and Biasing
- Undervoltage Detection
- Temperature Compensated Voltage Reference
- Sawtooth Oscillator
- Error Amplifier
- Pulse Width Modulator
- Digital Current Limiting
- Soft Start
- Control Logic (double pulse inhibit)
- Output Driver

The 4V reference voltage is provided for the regulation loop. A high gain error amplifier compares the reference voltage to the output voltage. The output of the error amplifier is then compared to a periodic ramp, which is generated by the sawtooth-oscillator circuit. The comparator output is a fixed-frequency, variable pulse width logic signal, which passes through logic circuits and the output driver and out to the external high voltage power-switching-FET.

A digital current limiting device suppresses the PWM logic signal when the voltage difference between current limit sense input I_P and GND reaches 100 mV to protect the external power-switching-FET.

Non-isolated and isolated SMPS-configurations are possible. Logic and analog circuits are implemented in BICMOS in order to achieve low power dissipation.

Start-Up Procedure

Before the switched-mode DC/DC converter starts, a sequence of several conditions has to be passed in order to avoid any system malfunction.

An integrated 6V linear voltage regulator supplies the internal low-voltage BICMOS-circuits from V_S. The generated supply voltage is connected to pin V_{EXT} and has to be buffered by an external capacitor (C_{min} = 1µF). Power dissipation of the linear voltage regulator can be reduced, if an external supply is used for that purpose by connecting it to pin V_{EXT}. If the voltage at V_{EXT} is greater than 6.2V, the internal linear voltage regulator turns off and the internal BICMOS-circuits are then fed from the external voltage source (power housekeeping input V_{EXT}). In this case, the input current at V_{EXT} is approximately 0.6mA.

Note: An internal 9.4V zener diode protects the V_{EXT} input against overvoltages. The maximum zener current is 6mA! If the external supply isn't stabilized, the input current must be limited (e.g. by a resistor, see also supply voltage range 0)!

Supply Voltage Ranges

Supply Voltage Range 0: 8V to 16V. In this supply voltage range the PEB/F 2023 can be supplied from a 12V battery. Connect the positive supply voltage via a resistor (R_7 in figure 5) to pin V_{EXT} and pin V_S via a resistor (R_6 in figure 5) to GND. Pin UV must be connected to pin V_S. Pin UVx must be connected to pin V_{EXT}. For calculating the values of the two resistors R_6 and R_7, see the description of figure 6.

Supply Voltage Range 1: 12V to 80V. Connect the input voltage to pin V_S and via a resistor (R_6 in figure 4) to pins UV and UVx. For calculating the value of this resistor see the description of figure 5.

Supply Voltage Range 2: 22V to 90V. Connect the input voltage to pin V_S and via a resistor to pin UV. Pin UVx is not connected (floating).

Supply Voltage Range 3: U_{ZD}+8V to U_{ZD}+90V. Connect the input voltage via a zener diode (minimum zener voltage U_{ZD} = 14V) to pin V_S and via a resistor (R_6 in figure 3) to pin UV. Pin UVx is not connected (floating).

Undervoltage Lockout

Note: At the undervoltage detection pin UV, a resistor with a value of about 100kΩ..10MΩ is required to protect this pin against high currents (see absolute maximum ratings). The level of undervoltage detection when using supply voltage range 1 is 8V..12V (PEF 2023: 7.5V..12V), using supply voltage range 2 or 3, it is 18V..22V (PEF 2023: 17.5V..22V). To get a higher undervoltage detection level a zener diode in series with the resistor is required.
When the PEB/F 2023 detects an undervoltage condition, the gate output driver will be turned off. The DC/DC conversion is disabled and the PEB/F 2023 shows a high input impedance seen from the undervoltage detection pins (UV, UVx) and from pin V_S to GND. Also the voltage on V_{EXT} will decrease. When the undervoltage condition is removed, the DC/DC converter will be enabled once again with a soft start.

Note: When using supply voltage range 0 the undervoltage detection circuit is not working. The resistor connected between V_S and GND bypasses this undervoltage detection circuit (R_6 in figure 5).

Voltage Reference

The reference regulator of the PEB/F 2023 is based on a temperature compensated bandgap. This circuitry is fully active at supply voltages (pin V_{EXT}) above 6 volts and provides up to 0.5mA of load current to external circuitry at 4 volts. This reference has to be buffered by an external capacitor (C_{min} = 1µF).

Sawtooth Oscillator

The oscilator frequency is programmed by the two components R_1 and C_1 (see figure 3, 4 or 5). The oscillator timing capacitor C_1 is charged by V_{REF} through R_1 and discharged by an internal 10kΩ discharge-resistor. The rise-time of the sawtooth oscillator can be programmed with R_1 and C_1. The internal discharge-resistor and C_1 define the fall-time. At the beginning of the discharge period a positive synchronization pulse is generated at pin SYNC. Otherwise the PEB/F 2023 can be synchronized via pin SYNC to an external logic clock by programming the oscillator to free run at a frequency 10% lower than the synchronization frequency. The PEB/F 2023 is synchronized by the rising edge of the sync. signal. So multiple devices can be synchronized together by programming one master unit for the desired frequency (only one possible interfering frequency).
Note that the frequency of the output driver is half the oscillator frequency. The switching frequency as a function of R_1 and C_1 is shown in **figure 8**.

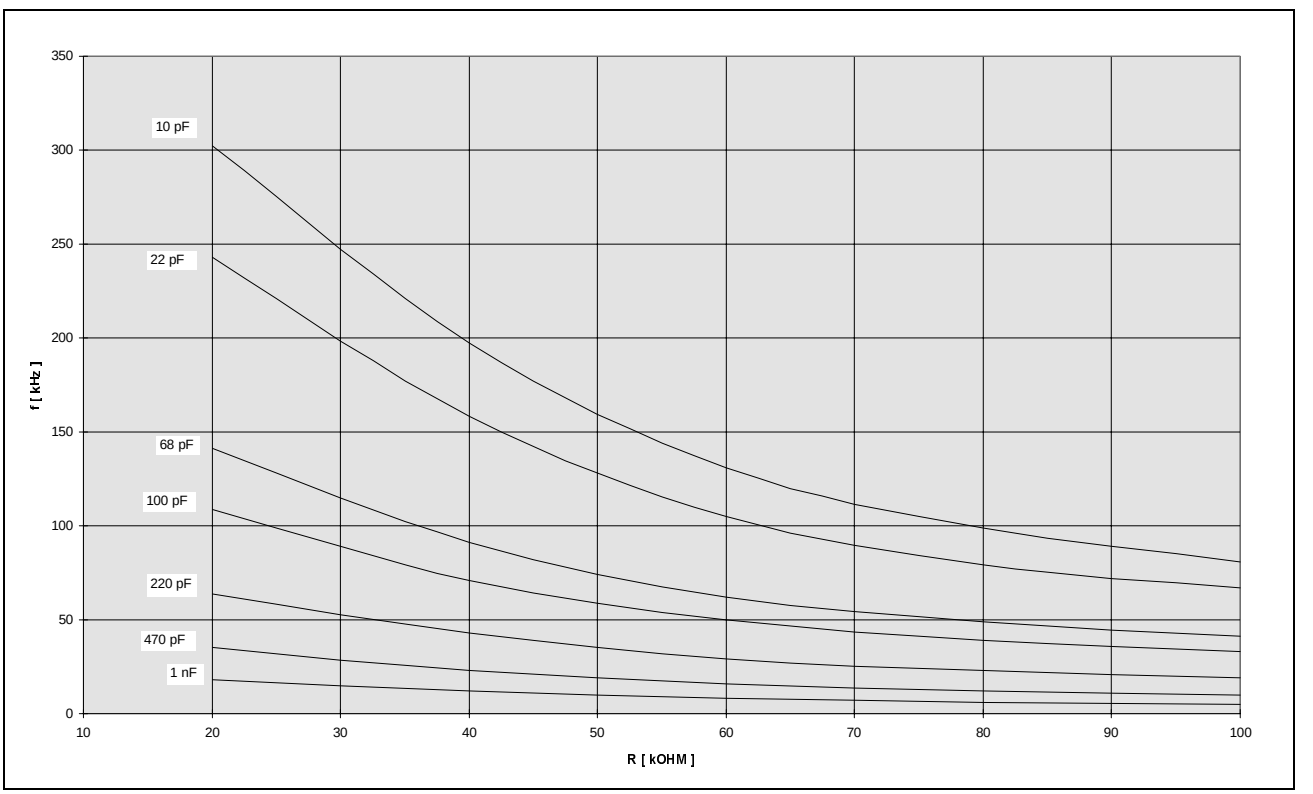


Figure 8 Switching Frequency

Error Amplifier

Conventional operational amplifier for closed-loop gain and phase compensation.
Low output impedance: unity-gain stable.

Pulse Width Modulator

The pulse width modulator compares the sawtooth-voltage of the oscillator output with the output of the error amplifier and with the voltage of the external soft start capacitor at pin C_{SS}.

Current Limiting

When the sense voltage reaches a threshold voltage of 100mV a shutdown signal is sent to the control logic. Sense voltage is the voltage between pin I_P and pin GND. Because of the small value of the current-sensing-resistor (R_5 in figure 3, 4 or 5) the board layout has to be done carefully.

Soft Start

The soft start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When the supply voltage is connected to the PEB/F 2023 the undervoltage lockout circuit holds the soft start capacitor voltage at zero. When the supply voltage reaches the normal operating range, an internal 1.5µA current source will charge the external soft start capacitor. As the soft start voltage ramps up to +5 volts, the duty cycle of the PWM linearly increases to whatever value the regulation loop requires.

Control Logic

The control logic inhibits double pulses during one duty cycle and limits the maximum duty cycle to 50%.

Disable Input Realization

One way to disable the function of the PEB/F 2023 is to connect an external n-channel MOS-transistor between the pins UV(drain) and GND(source). By switching on this external transistor the PEB/F 2023 detects an ’undervoltage’ and turns off. After switching off this external transistor the PEB/F 2023 turns on and starts the DC/DC conversion with a soft start.
A second posibility is to connect an external n-channel MOS-transistor between the pins C_{SS}(drain) and GND(source). By switching on this external transistor the PEB/F 2023 disables the gate output driver because of the soft start circutry. After switching off this external transistor the PEB/F 2023 turns on and starts the DC/DC conversion with a soft start.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage (pin V_S) for sup. voltage range 1	V_{S1}	-0.3	80	V	Referred to GND
Supply voltage (pin V_S) for sup. voltage range 2 or 3	$V_{S2,3}$	-0.3	90	V	Referred to GND
Transient input current on pin V_S (sup. voltage range 1, 2 or 3)	i_{Vs}	-10 -30	10 30	mA mA	t ≤ 100 msec t ≤ 10 msec
Analog input voltage (pins I_P, COMP, V_P, V_N, SYNC, RC)	$V_{I\,A}$	-0.3	V_{EXT} +0.3	V	Referred to GND
Reference output current (pin V_{REF})	$I_{O\,REF}$		5	mA	
SYNC-output current (pin SYNC)	$I_{O\,SYNC}$		5	mA	
Error amplifier output current (pin COMP)	$I_{O\,COMP}$		5	mA	
Z-current (pin V_{EXT})	$I_{Z\,EXT}$		6	mA	
Output current (pin V_{EXT})	$I_{O\,EXT}$		6	mA	
Driver output current (pin GA)	$I_{O\,DR}$		25	mA	
Undervoltage detection input currents (pins UV, UVx)	I_{UV}, I_{UVx} i_{UV}, i_{UVx}	 -10	1 10	mA mA	 t ≤ 10 msec
Junction temperature	T_j	0	150	℃	
Storage temperature	T_{stg}	-40	150	℃	
ESD-voltage, all pins			1	kV	Human body model

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

*Note: If not otherwise stated than this absolute maximum values are static values. For overvoltage protection (pin V_S respectively UV and UVx) see chapter **1.6 Surge Protection**.*

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature under bias PEB 2023 PEF 2023	 T_A T_A	 0 -40	 70 85	 °C °C	
Supply voltage (pin V_S) for sup. voltage range 1	V_{S1}	12	80	V	Referred to GND
Supply voltage (pin V_S) for sup. voltage range 2 or 3	$V_{S2,3}$	8	90	V	Referred to GND

Note: In the operating range the functions given in the circuit description are fulfilled.

3.3 Static Thermal Resistance

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Junction to ambient	$R_{th, jA}$		112	K/W	P-DSO-14

3.4 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current (pin V_S to GND)	I_S		6	12	µA	V_{EXT} = 6.2V, V_S = 40V
Reference V_{REF}						
Output voltage	$V_{REF\ O}$	3.96	4.0	4.04	V	T_A = 25°C, I_L = 0mA, V_S = 40V
Line regulation	$V_{REF\ Line}$		0.1	5	mV	T_A = 25°C, V_S = 25 to 65V, I_L = 0mA,
Load regulation	$V_{REF\ Load}$		2	5	mV	T_A = 25°C, I_L = 0.1 to 0.3mA, V_S = 40V
Temperature stability	$V_{REF\ TS}$		10	20	mV	T_A = -40 to 85°C, I_L = 0mA, V_S = 40V
Oscillator SYNC, RC f_{OSC} = 20kHz, R_T = 39kΩ ± 1 %, C_T = 1nF ± 1 %						
Initial accuracy	Δf_O		± 5	± 10	%	T_A = 25°C, V_S = 40V
Voltage stability of f_{OSC}	$\Delta f_{O\ Line}$		±0.1	±1	%	T_A = 25°C, V_S = 25 to 65V
Temperature stability of f_{OSC}	$\Delta f_{O\ TS}$			±5	%	T_A = -40 to 85°C, V_S = 40V
Max. frequency	f_{max}	550			kHz	R_T =20kΩ, C_T=10pF
H-sawtooth voltage	V_H	3.0	3.2	3.4	V	
L-sawtooth voltage	V_L	1.6	1.8	2.0	V	
H-sync output level	$V_{SYNC\ H}$	2.4	3.5	5.25	V	I_L = 0.5mA, V_{EXT} = 6.2V
L-sync output level	$V_{SYNC\ L}$		0.2	0.8	V	I_L = 20µA
Pulse Width Modulator						
Duty cycle	t_d	0		50	%	
Soft Start C_{ss}						
Charging current	I_C	1	1.5	2	µA	V_{CSS} = 0V

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Error Amplifier COMP, V_P, V_N						
Input offset voltage	V_{IO}	-10		10	mV	V_{CMR} = 1.8 ... 4.5V
Input current	I_I		25	50	nA	
Common mode range	V_{CMR}	1.8		4.5	V	
DC open loop gain	G_{VO}	60	70		dB	
Common mode rejection	k_{CMR}	60	70		dB	f ≤ 10kHz
Unity gain bandwidth	f	0.5	1		MHz	C_L (pin) = 10pF
Supply voltage rejection V_{EXT} / V_{COMP}	k_{SVR}	60	70		dB	f ≤ 10kHz
H-output voltage	V_{OH}	4.5			V	I_L = 100µA
L-output voltage	V_{OL}		0.02	0.1	V	I_L = 10µA
Current Limit Comparator I_P						
Sense voltage PEB 2023 PEF 2023	 V_{Sense} V_{Sense}	 90 85	 100 100	 110 110	 mV mV	 V_S = 40V V_S = 40V
Input bias current	I_I		-25	-40	µA	V_{IP} = 0V
Input voltage range	V_I	0		1	V	
Response time (signal at GA)	t_{Res}		250	500	ns	I_P = 0 → 200mV
Output Driver GA						
H-output voltage	V_{OH}	4.5		V_{EXT}	V	I_{Source} = 20mA, V_{EXT} = 6.2V
L-output voltage	V_{OL}		0.3	0.4	V	I_{Sink} = 20mA
Rise time (10% to 90%)	t_r		50	200	ns	C_L = 800pF, V_{EXT} = 6.2V
Fall time (90% to 10%)	t_f		50	200	ns	C_L = 800pF, V_{EXT} = 6.2V

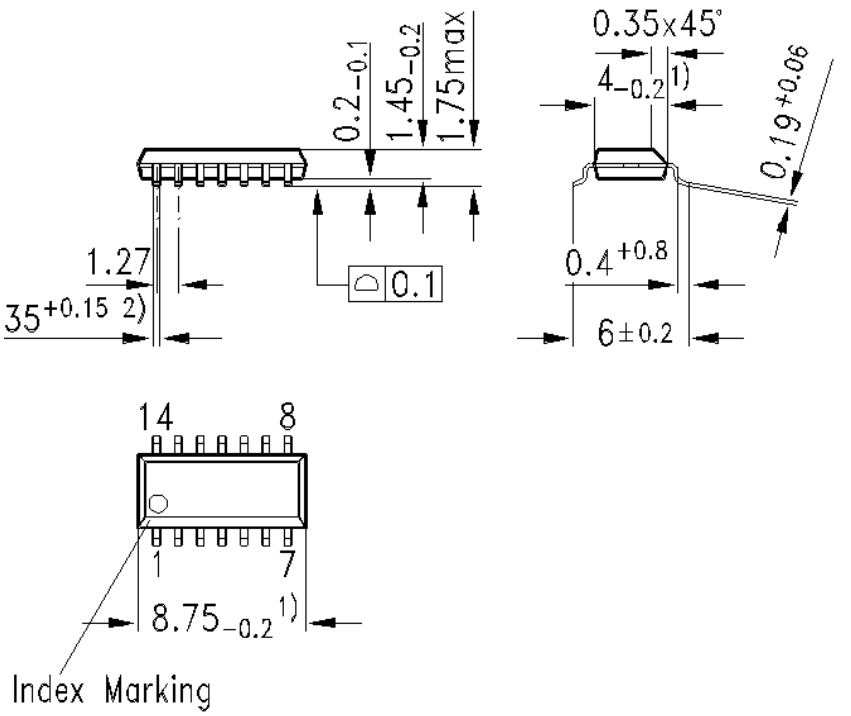
DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Undervoltage Detection UV, UVx						
Start-up threshold 1 PEB 2023 PEF 2023	 $V_{UV\ St1}$ $V_{UV\ St1}$	 8 7.5	 10 10	 12 12	 V V	supply voltage range 1
Start-up threshold 2,3 PEB 2023 PEF 2023	 $V_{UV\ St2,3}$ $V_{UV\ St2,3}$	 18 17.5	 20 20	 22 22	 V V	supply voltage range 2 or 3
External Supply V_{EXT}						
Output voltage	V_O	5.8	6.0	6.2	V	
Output current	I_O			2	mA	
Input voltage	V_I	6.2		9	V	
Z-current	I_Z			6	mA	
General Parameters						
Power consumption	P_{tot}		5	6	mW	V_S = 40V, f_{OSC} = 20kHz, $C_{L\ GATE}$ = 470pF, V_{EXT} = 6.2 to 6.7V
High impedance input current	I_{HI}			10	µA	„undervoltage“

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

4 Package Outlines

Plastic Package, P-DSO-14
(Plastic Dual Small Outline



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side