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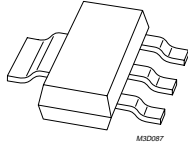
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Kind regards,

Team Nexperia



# PHT6N06T

TrenchMOS™ standard level FET

Rev. 02 — 03 February 2003

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHT6N06T in SOT223.

### 1.2 Features

- Low on-state resistance
- Fast switching
- Low  $Q_{GD}$
- Surface mounting package.

### 1.3 Applications

- DC to DC converters
- General purpose switching.

### 1.4 Quick reference data

- $V_{DS} \leq 55 \text{ V}$
- $I_D \leq 5.5 \text{ A}$
- $P_{tot} \leq 8.3 \text{ W}$
- $R_{DSon} \leq 150 \text{ m}\Omega$

## 2. Pinning information

Table 1: Pinning - SOT223, simplified outline and symbol

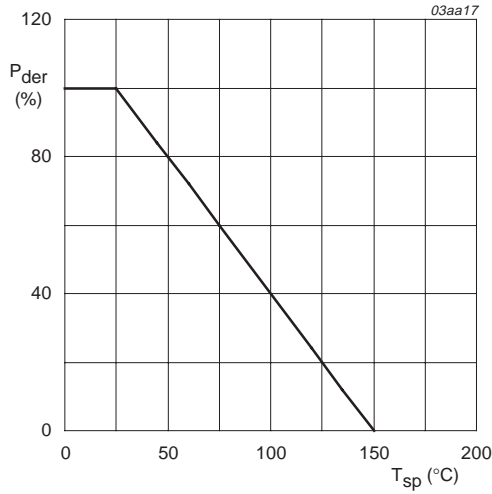
Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view</p> <p>MSB002 - 1</p> <p>SOT223</p>	<p>MBB076</p>
2	drain (d)		
3	source (s)		
4	drain (d)		

### 3. Limiting values

**Table 2: Limiting values**

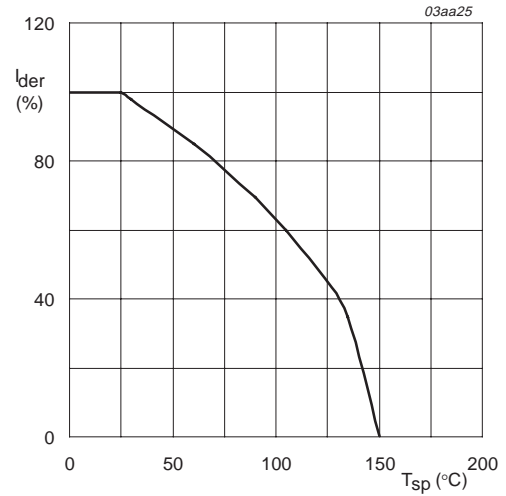
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	55	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2 and 3</b>	-	5.5	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2</b>	-	3.8	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <b>Figure 3</b>	-	22	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; <b>Figure 1</b>	-	8.3	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	5.5	A
$I_{SM}$	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	22	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

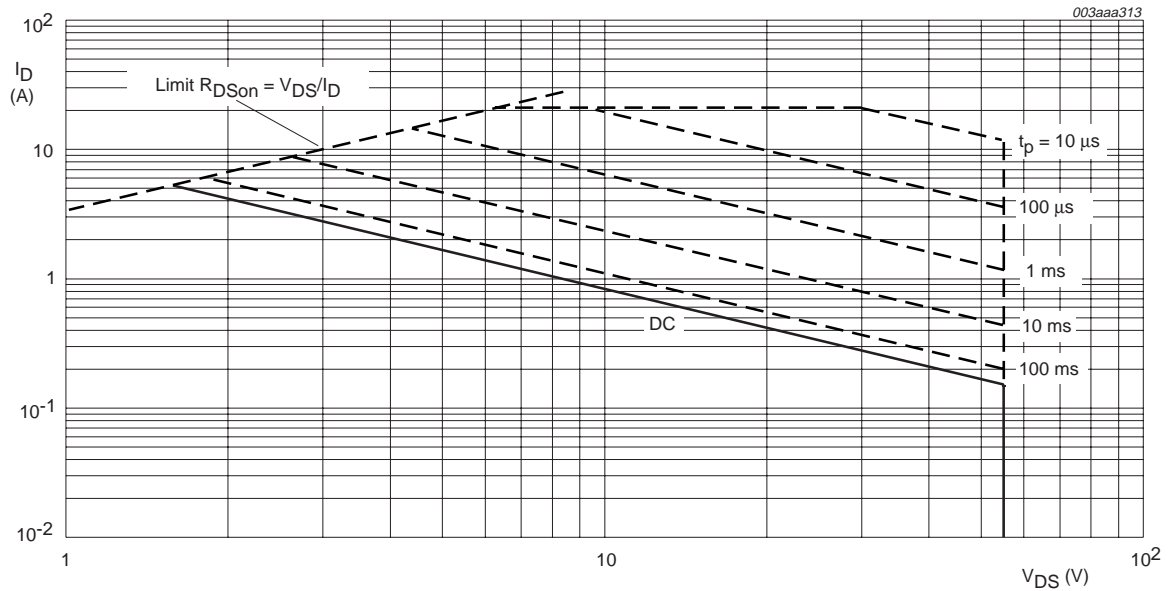
Fig 1. Normalized total power dissipation as a function of solder point temperature.



V<sub>GS</sub> ≥ 10 V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T<sub>sp</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 10 V.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	70	-	K/W

### 4.1 Transient thermal impedance

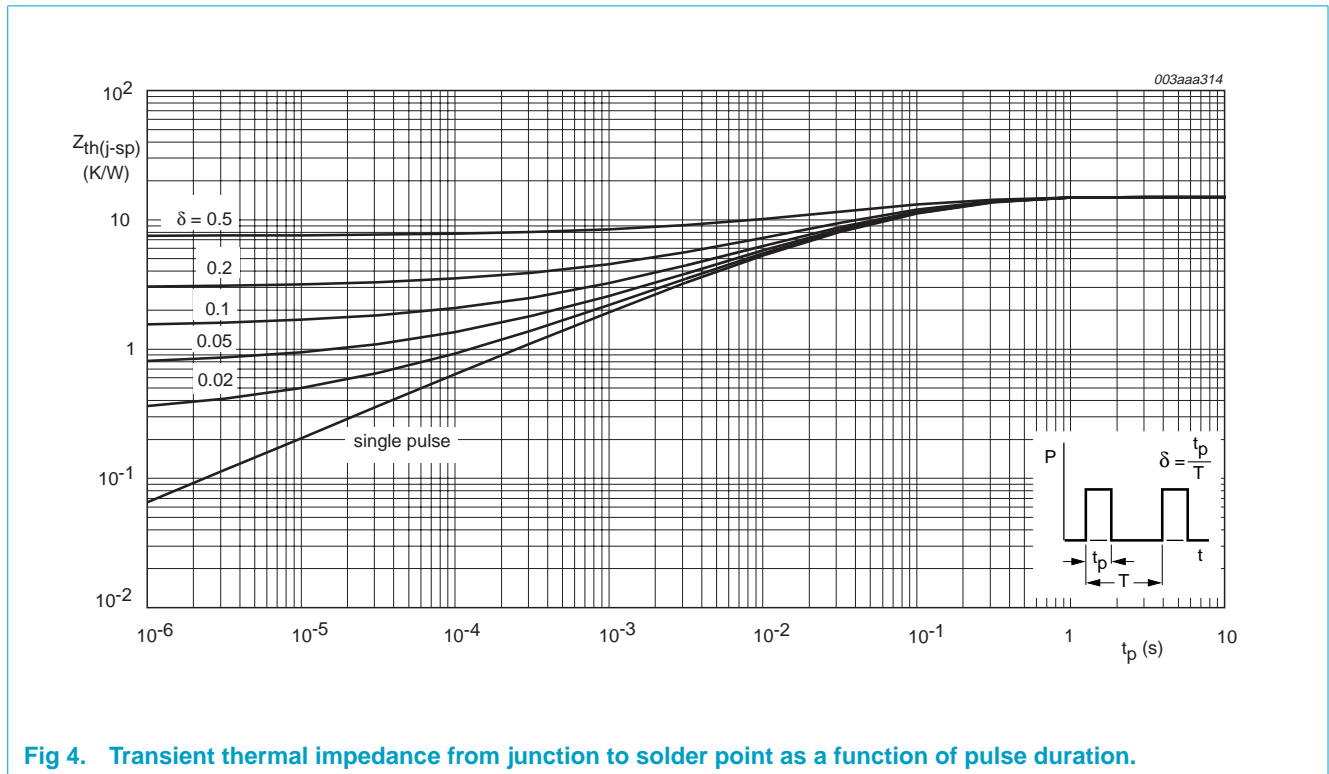
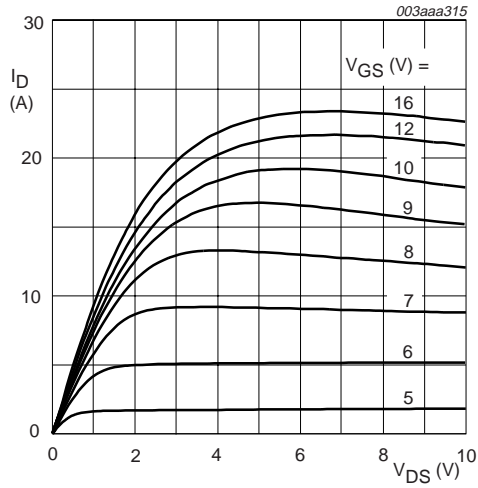


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

## 5. Characteristics

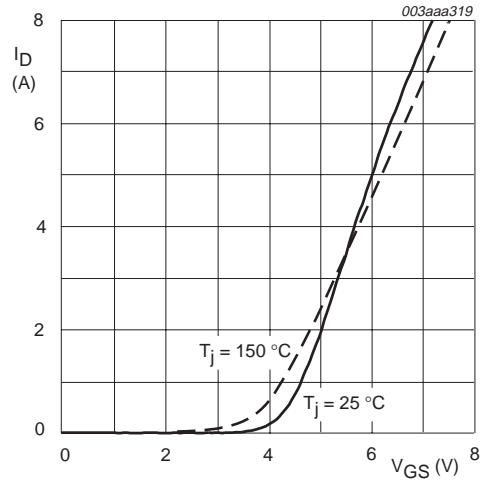
**Table 4: Characteristics**
 $T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; <b>Figure 9</b>				V
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 55\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	0.05	10	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}$ ; $V_{DS} = 0\ \text{V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$ ; $I_D = 5\ \text{A}$ ; <b>Figure 7 and 8</b> $T_j = 25\text{ °C}$	-	128	150	m $\Omega$
		$T_j = 150\text{ °C}$	-	-	278	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$I_D = 5\ \text{A}$ ; $V_{DD} = 44\ \text{V}$ ; $V_{GS} = 10\ \text{V}$ ; <b>Figure 13</b>	-	5.6	-	nC
$Q_{gs}$	gate-source charge		-	1.2	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	2.6	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}$ ; $V_{DS} = 25\ \text{V}$ ; $f = 1\ \text{MHz}$ ; <b>Figure 11</b>	-	175	-	pF
$C_{oss}$	output capacitance		-	58	-	pF
$C_{rss}$	reverse transfer capacitance		-	40	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\ \text{V}$ ; $I_D = 5\ \text{A}$ ; $V_{GS} = 10\ \text{V}$ ; $R_G = 6\ \Omega$	-	4.9	-	ns
$t_r$	rise time		-	14.5	-	ns
$t_{d(off)}$	turn-off delay time		-	7.8	-	ns
$t_f$	fall time		-	4.5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 5\ \text{A}$ ; $V_{GS} = 0\ \text{V}$ ; <b>Figure 12</b>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\ \text{A}$ ; $di_S/dt = -100\ \text{A}/\mu\text{s}$ ; $V_{GS} = 0\ \text{V}$ ;	-	32	-	ns
$Q_r$	recovered charge	$V_R = 30\ \text{V}$	-	50	-	nC



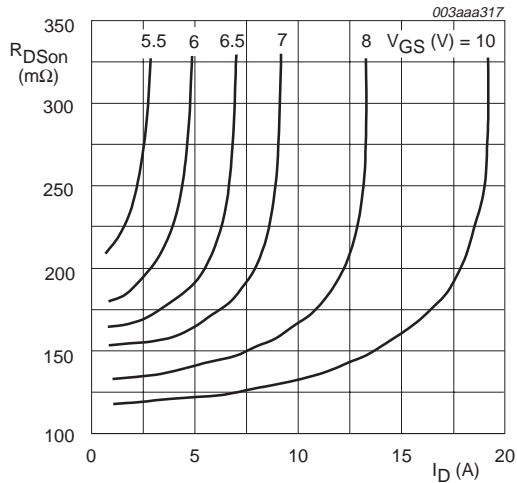
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



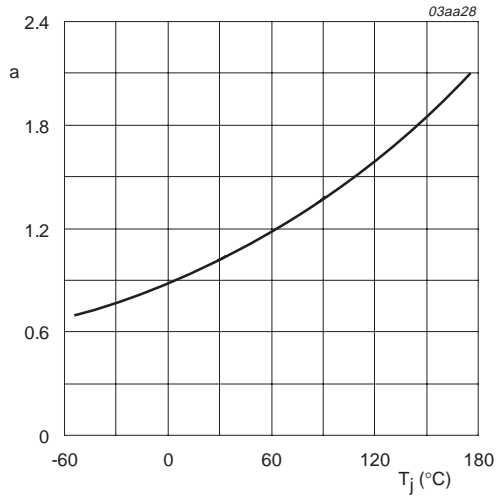
$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



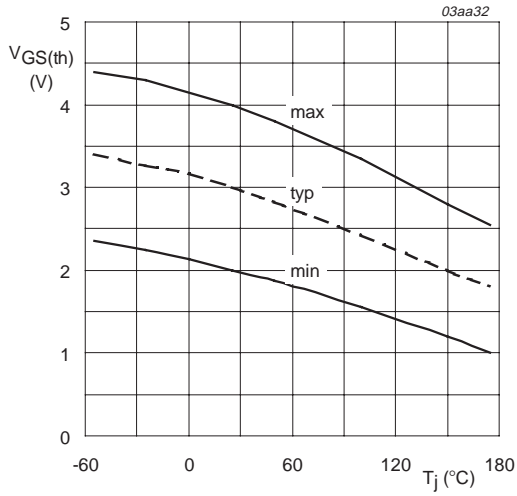
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



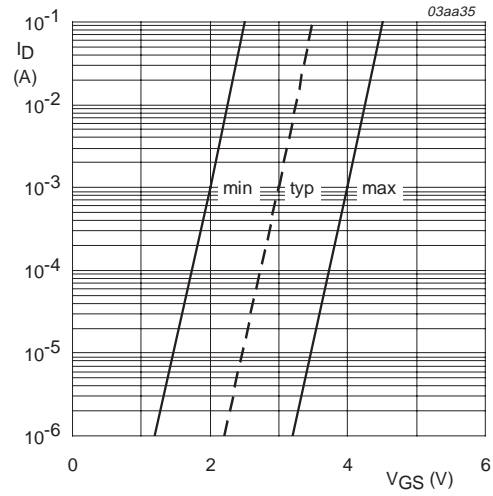
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ °C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



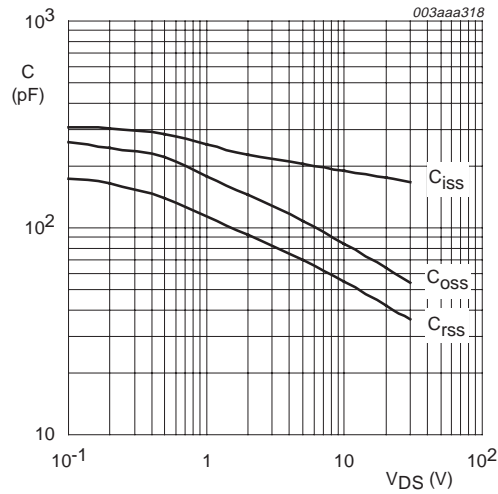
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

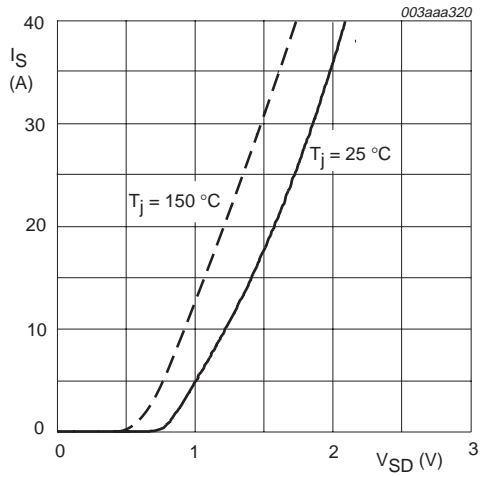
Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

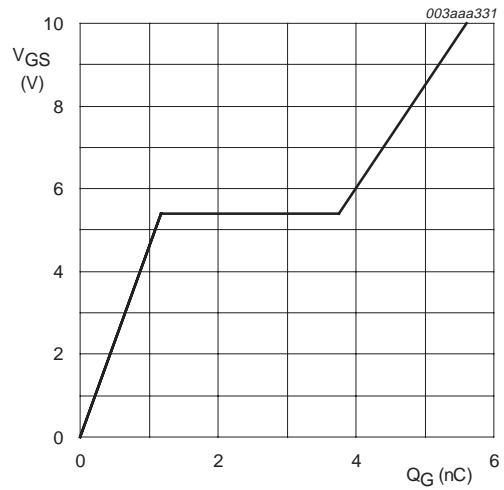
Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.





$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 5\text{ A}$ ;  $V_{DD} = 44\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

6. Package outline

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223

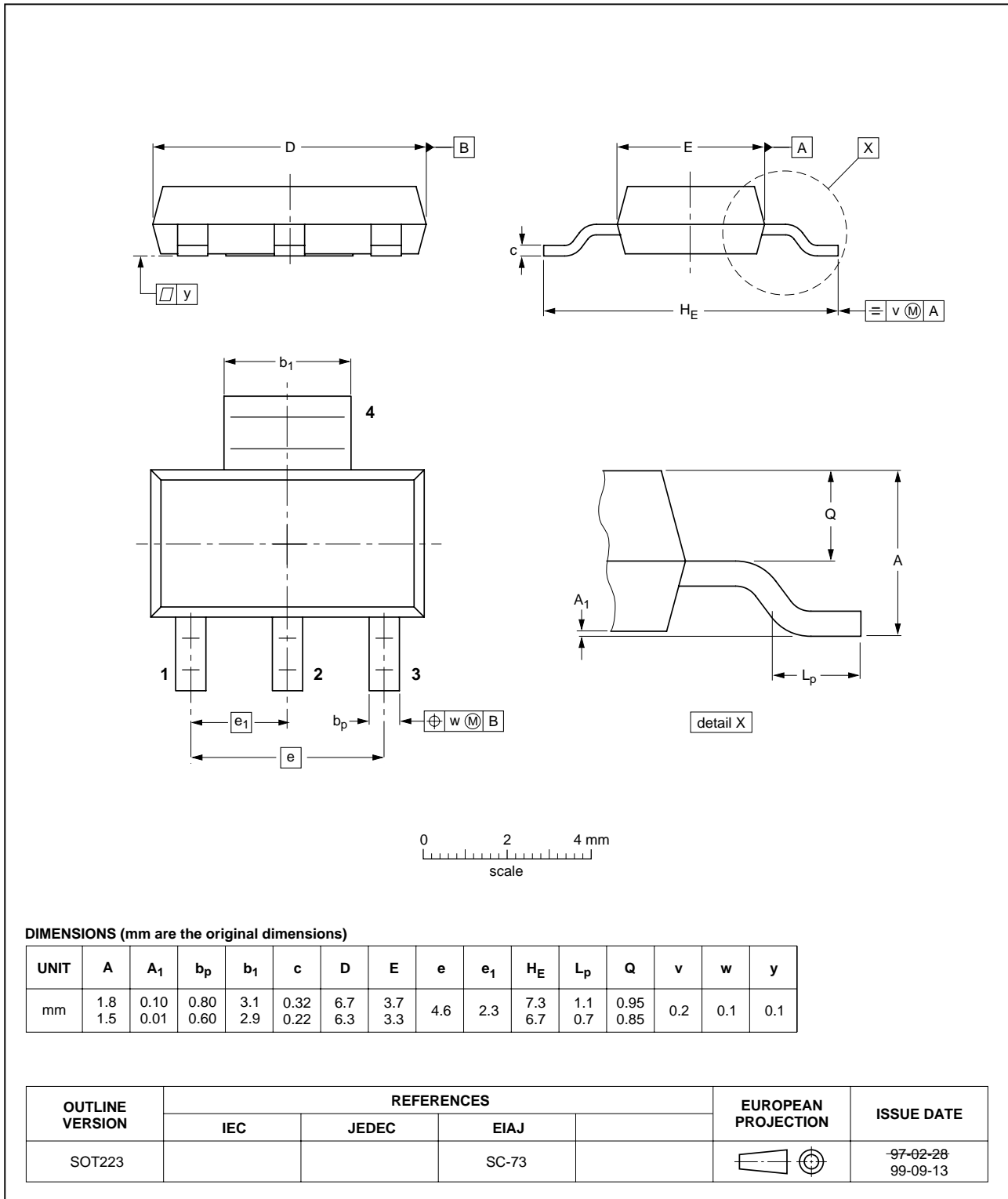


Fig 14. SOT223.

## 7. Revision history

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Table 5: Revision history

Rev	Date	CPCN	Description
02	20030203	200209006	<p>Product data (9397 750 10633); supersedes product specification PHT6N06T Rev 1.000 of September 1997</p> <p>Modifications:</p> <ul style="list-style-type: none"><li>• The format of this specification has been redesigned to comply with Philips Semiconductors new presentation and information standard</li><li>• ESD diodes removed from device and specification</li><li>• Characteristics updated in <a href="#">Table 4</a>.</li></ul>

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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