

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

ICS840002-01

GENERAL DESCRIPTION



The ICS840002-01 is a 2 output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL1:0): 156.25MHz, 125MHz, and 62.5MHz. The ICS840002-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Ethernet jitter requirements. The ICS840002-01 is packaged in a small 16-pin TSSOP package.

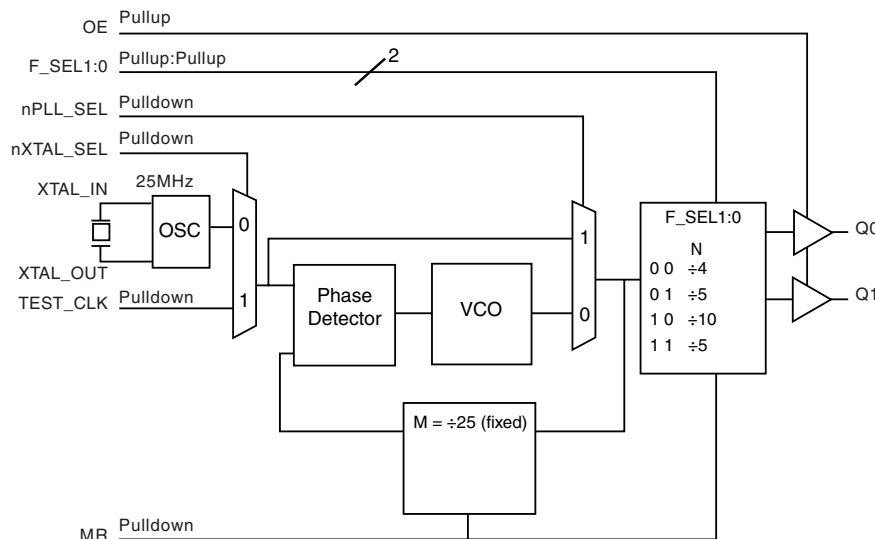
FEATURES

- Two LVCMOS/LVTTL outputs @ 3.3V, 17Ω typical output impedance
 - Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
 - Output frequency range: 56MHz - 175MHz
 - VCO range: 560MHz - 700MHz
 - Output skew: 12ps (maximum)
 - RMS phase jitter at 156.25MHz (1.875MHz - 20MHz): 0.47ps (typical)
- Phase noise:
- | Offset | Noise Power |
|--------|---------------|
| 100Hz | -97.4 dBc/Hz |
| 1kHz | -120.2 dBc/Hz |
| 10kHz | -127.6 dBc/Hz |
| 100kHz | -126.1 dBc/Hz |
- Full 3.3V or 3.3V core/2.5V output supply mode
 - -30°C to 85°C ambient operating temperature
 - Available in both standard and lead-free RoHS compliant packages

FREQUENCY SELECT FUNCTION TABLE

Inputs				Output Frequency (25MHz Ref.)
F_SEL1	F_SEL0	M Divider Value	N Divider Value	
0	0	25	4	156.25
0	1	25	5	125
1	0	25	10	62.5
1	1	25	5	125

BLOCK DIAGRAM



PIN ASSIGNMENT

F_SEL0	1	16	F_SEL1
nXTAL_SEL	2	15	GND
TEST_CLK	3	14	GND
OE	4	13	Q0
MR	5	12	Q1
nPLL_SEL	6	11	VDD0
VDDA	7	10	XTAL_IN
VDD	8	9	XTAL_OUT

ICS840002-01
16-Lead TSSOP
 4.4mm x 5.0mm x 0.92mm package body
G Package
 Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	F_SEL0	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
2	nXTAL_SEL	Input	Pulldown	Selects between the crystal or TEST_CLK inputs as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
3	TEST_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL clock input.
4	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing active outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
7	V _{DDA}	Power		Analog supply pin.
8	V _{DD}	Power		Core supply pin.
9, 10	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
11	V _{DDO}	Power		Output supply pin.
12, 13	Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
14, 15	GND	Power		Power supply ground.
16	F_SEL1	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance			8		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	3.3V±5%	14	17	21	Ω
		2.5V±5%	16	21	25	Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5$ V
Outputs, V_O	-0.5V to $V_{DDO} + 0.5$ V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -30^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	OE, F_SEL0, F_SEL1	$V_{DD} = V_{IN} = 3.465$ V or 2.625V		5	μA
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = V_{IN} = 3.465$ V or 2.625V		150	μA
I_{IL}	Input Low Current	OE, F_SEL0, F_SEL1	$V_{DD} = 3.465$ V or 2.625V, $V_{IN} = 0$ V	-150		μA
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = 3.465$ V or 2.625V, $V_{IN} = 0$ V	-5		μA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.465V \pm 5\%$	2.6		V
			$V_{DDO} = 2.5V \pm 5\%$	1.8		V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3$ V or $2.5V \pm 5\%$		0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuits.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -30^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01	112		140	MHz
		F_SEL[1:0] = 10 or 11	56		70	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 3			12	ps	
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 2	156.25MHz (1.875MHz - 20MHz)		0.47		ps
		125MHz (1.875MHz - 20MHz)		0.57		ps
		62.5MHz (1.875MHz - 20MHz)		0.51		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -30^\circ C$ TO $85^\circ C$

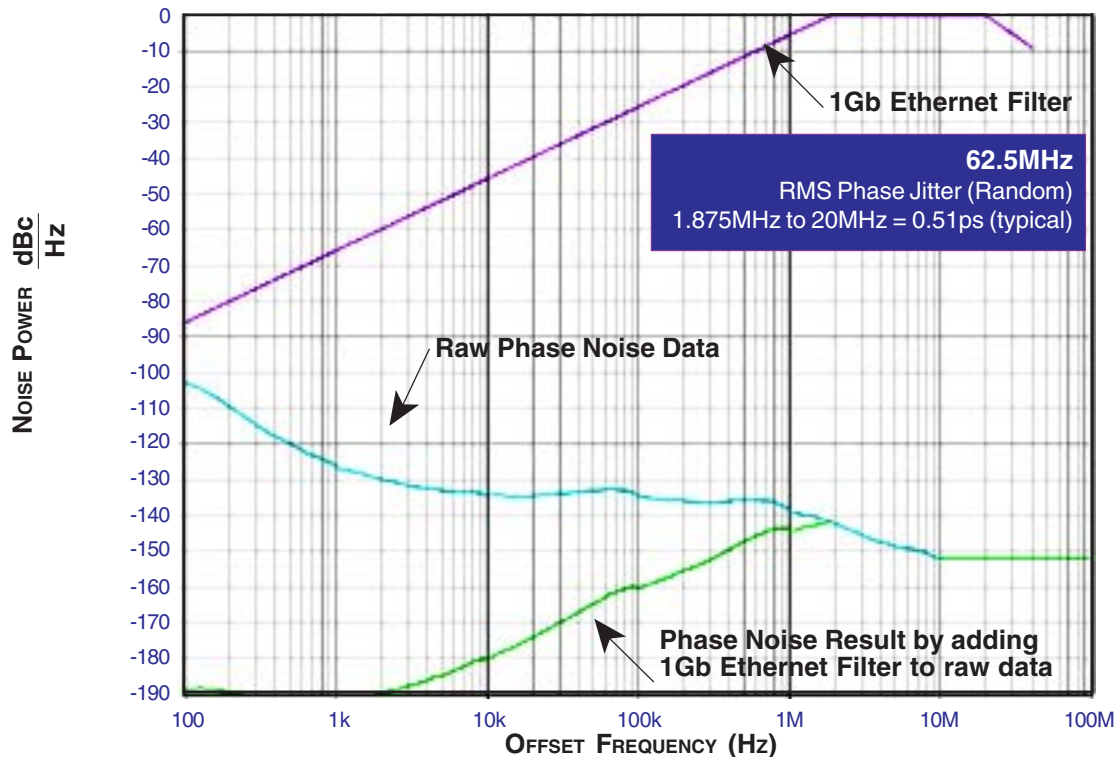
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01	112		140	MHz
		F_SEL[1:0] = 10 or 11	56		68	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 3			12	ps	
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 2	156.25MHz (1.875MHz - 20MHz)		0.47		ps
		125MHz (1.875MHz - 20MHz)		0.55		ps
		62.5MHz (1.875MHz - 20MHz)		0.49		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.

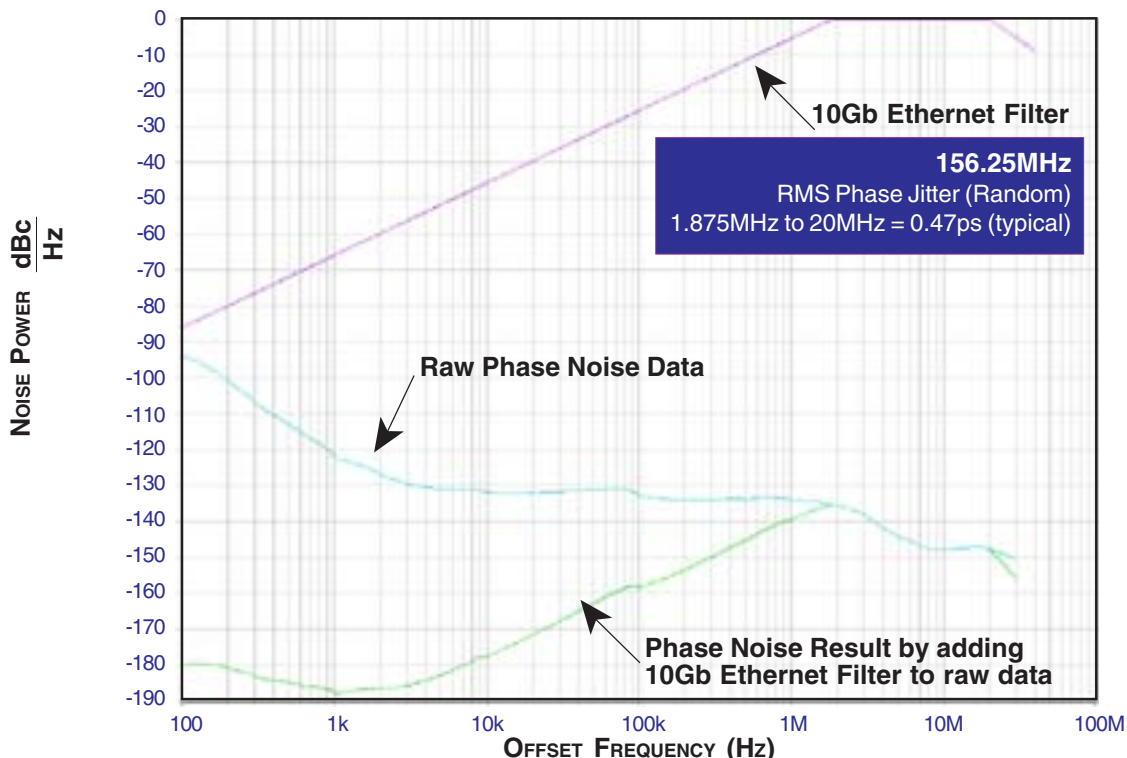
NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

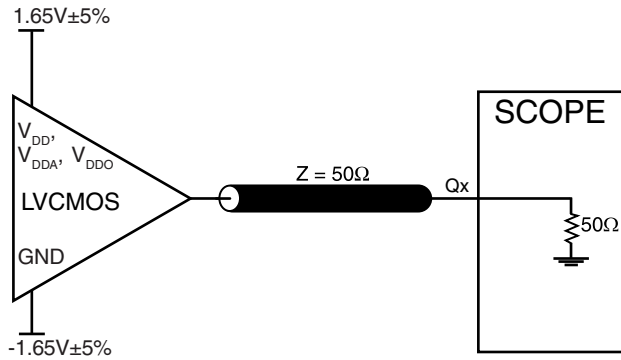
TYPICAL PHASE NOISE AT 62.5MHz @3.3V



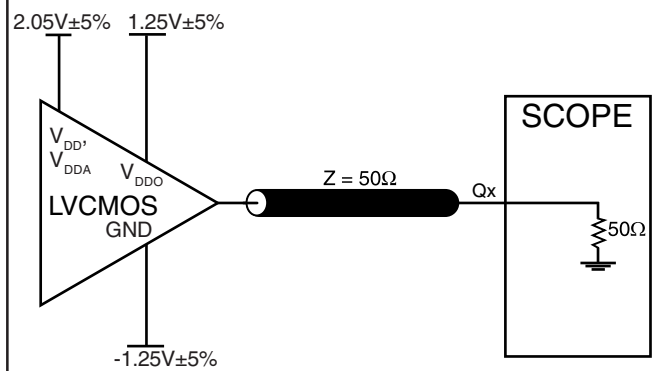
TYPICAL PHASE NOISE AT 156.25MHz @3.3V



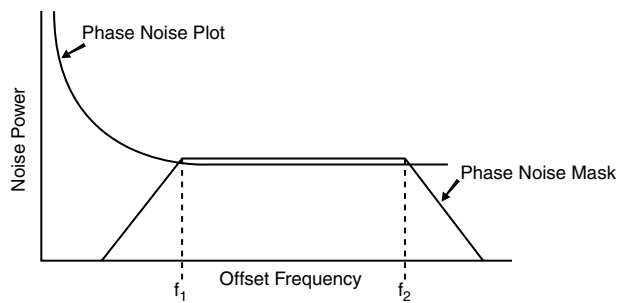
PARAMETER MEASUREMENT INFORMATION



3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

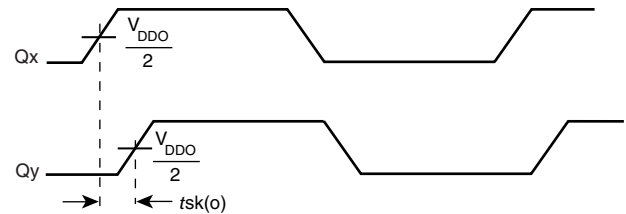


3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

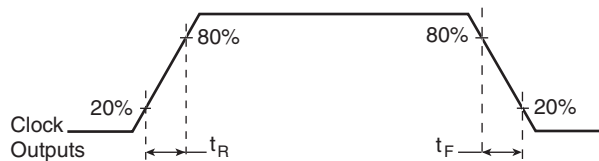


$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

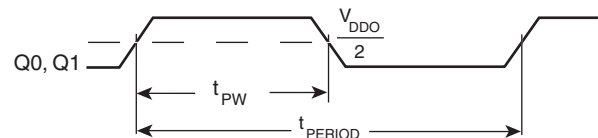
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840002-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} . The 10Ω resistor can also be replaced by a ferrite bead.

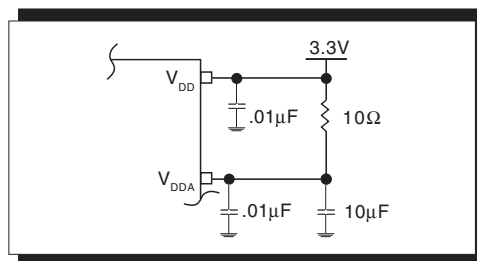


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840002-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

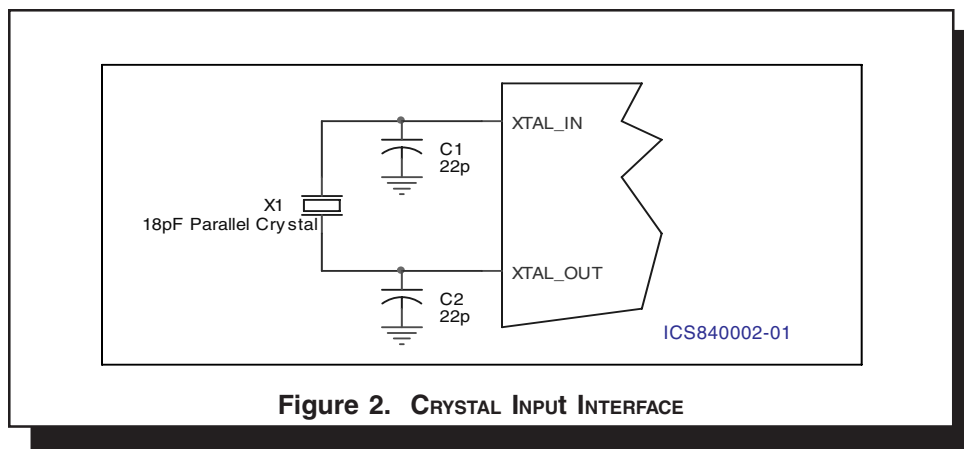


Figure 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LAYOUT GUIDELINE

Figure 3 shows a schematic example of the ICS840002-01. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18 pF parallel resonant 25MHz crystal is used. The C1=22pF and

C2=22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. 1KΩ pullup or pulldown resistors can be used for the logic control input pins.

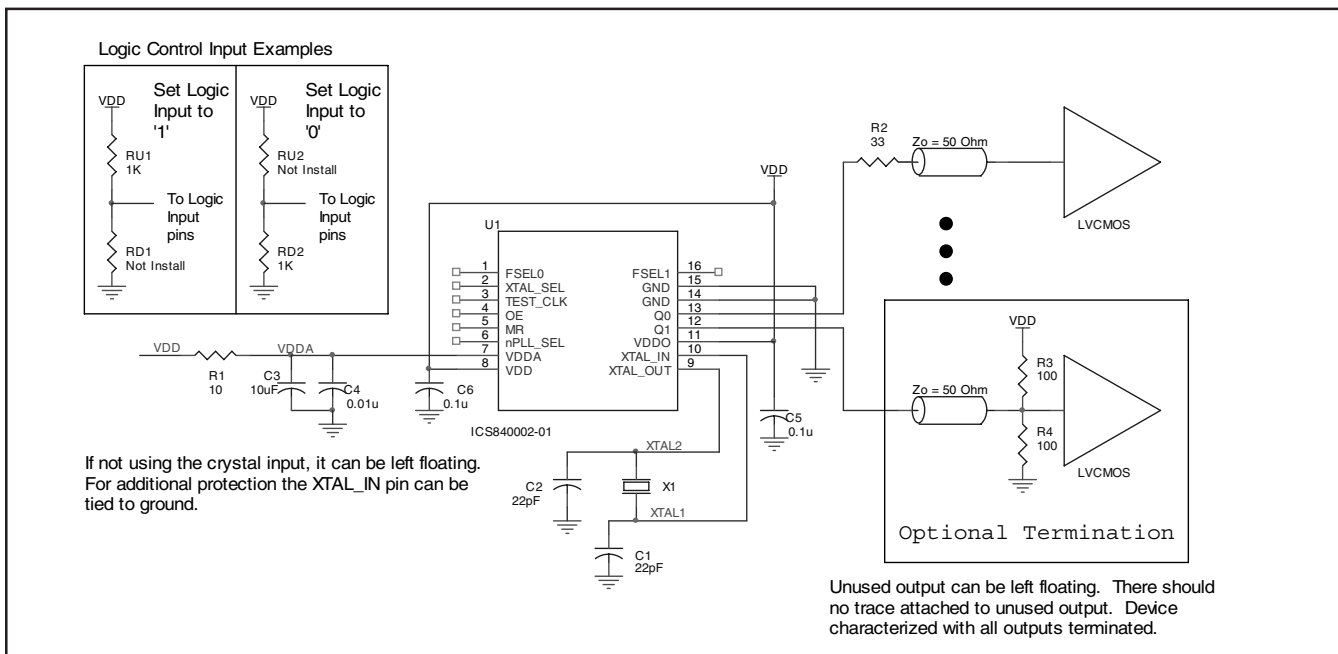


FIGURE 3. ICS840002-01 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} vs. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840002-01 is: 3085

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

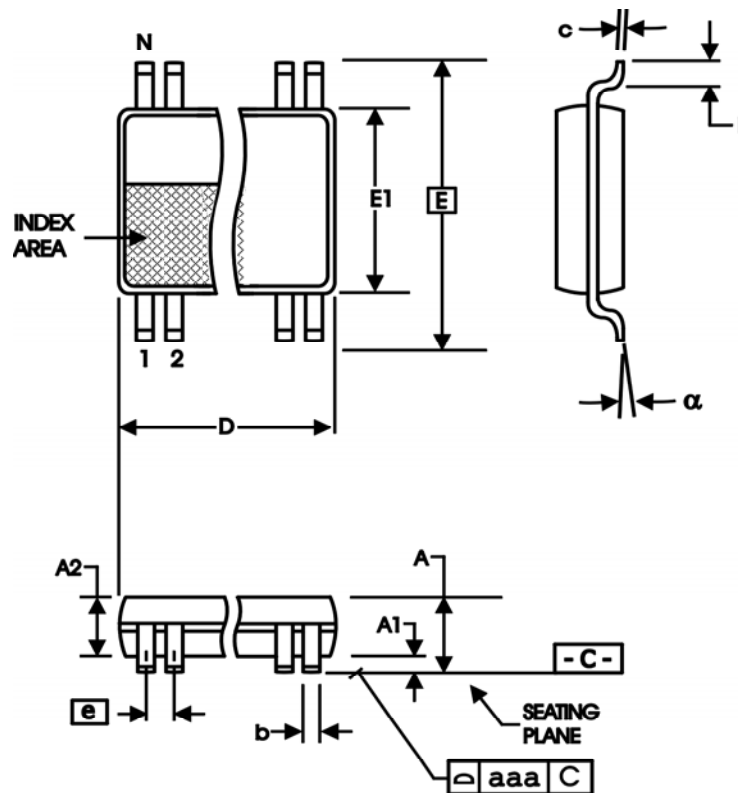


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840002AG-01	40002A01	16 Lead TSSOP	tube	-30°C to 85°C
ICS840002AG-01T	40002A01	16 Lead TSSOP	2500 tape & reel	-30°C to 85°C
ICS840002AG-01LF	0002A01L	16 Lead "Lead-Free" TSSOP	tube	-30°C to 85°C
ICS840002AG-01LFT	0002A01L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-30°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

The aforementioned trademarks, HiPerClockS and FemtoClocks are trademarks of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T4 T8	1	Features Section - corrected the integration range from 1.875MHz - 175MHz to 1.875MHz - 20MHz in the RMS phase jitter bullet.	1/13/06
		4	Crystal Characteristics Table - added Drive Level.	
		8	Added <i>Recommendations for Unused Input and Output Pins</i> .	
		11	Ordering Information Table - corrected standard marking and added Lead-Free part number, marking and note.	

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

clockhelp@idt.com
408-284-8200

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan

Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe

IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339