



128Kx32 SRAM MODULE

FEATURES

- Access Time 20nS
- MIL-STD-883 Compliant Devices Available
- Packaging
 - 66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic Package, Industry Standard Pinout, SMD Number 5962-93187-09HXX
 - 68 lead, 40mm, Hermetic CQFP

- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS128K32-XHX - 13 grams typical
 - WS128K32-XG4X - 20 grams typical

FIG. 1 PIN CONFIGURATION FOR WS128K32N-20HX, SMD 5962-93187-09HXX

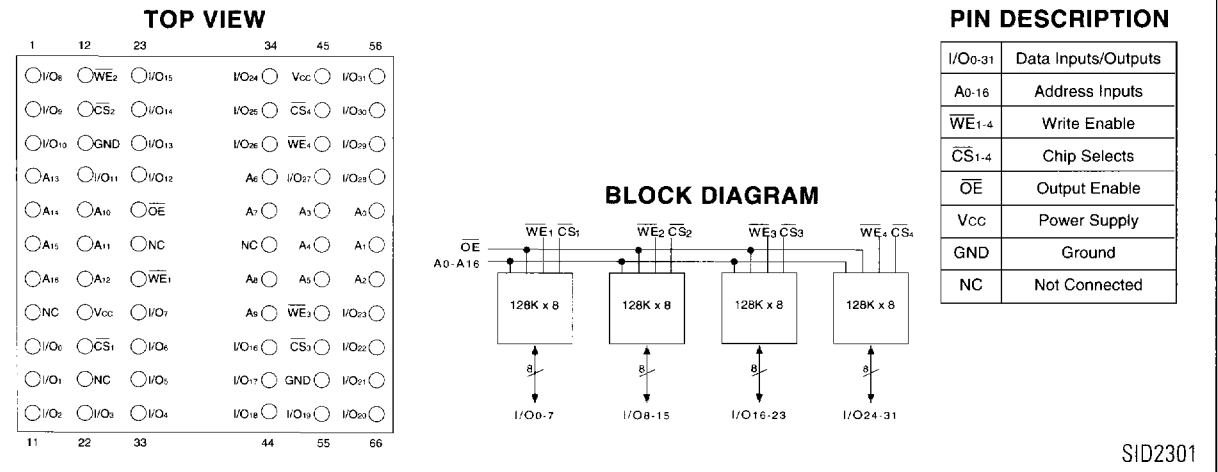
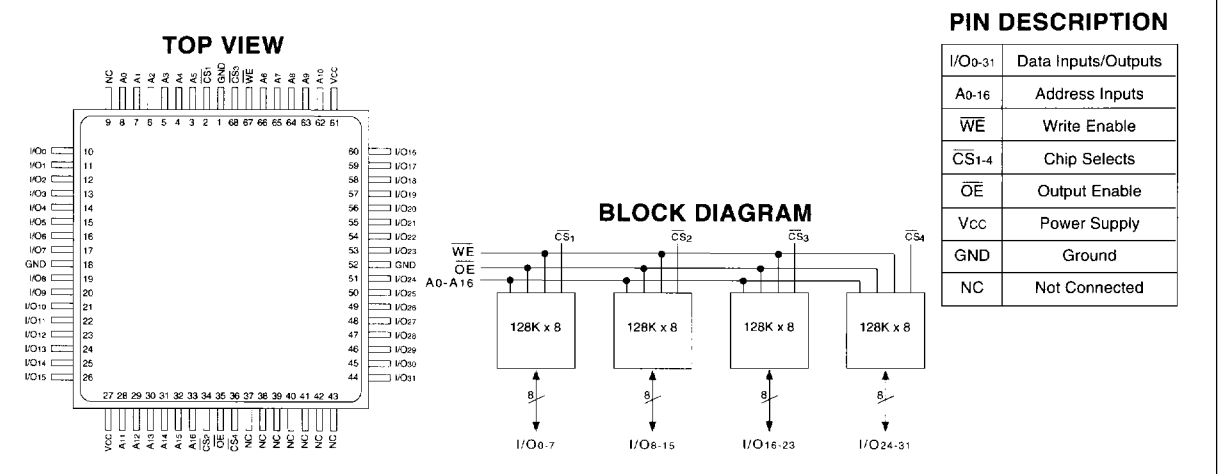


FIG. 2 PIN CONFIGURATION FOR WS128K32-20G4X





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature Range	T _{STG}	-65	+150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V
Signal Voltages Any Pin	V _G	-0.5	V _{CC} + 0.5	V
Junction Temperature	T _J		150	°C

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE
(@ T_A = +25°C)

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
\overline{OE} capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz		50	pF
\overline{WE} 1-4 capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz		30	pF
\overline{CS} 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz		30	pF
D0 - D31 capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz		30	pF
A0 - A16 capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz		50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-20			Units
			Min	Typ	Max	
Input Leakage Current	I _{LI}	V _{CC} = Max, V _{IN} = GND to V _{CC}			10	μA
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{CC}			10	μA
Operating Supply Current x32 mode	I _{CCX32}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		430	750	mA
Standby Current	I _{SB}	\overline{CS} = V _{CC} , V _{IN} = V _{IL} or V _{IH} , Duty Cycle = 100%		60	100	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5			0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4			V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-20			Units
			Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - 2V$	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		0.1	8.5	mA

2 SRAM MODULES



AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-20		Units
		Min	Max	
Read Cycle				
Read Cycle Time	t _{RC}	20		nS
Address Access Time	t _{AA}		20	nS
Output Hold from Address Change	t _{OH}	4		nS
Chip Select Access Time	t _{ACS}		20	nS
Output Enable to Output Valid	t _{OE}		15	nS
Chip Select to Output in Low Z	t _{CLZ'}	4		nS
Output Enable to Output in Low Z	t _{OLZ'}	4		nS
Chip Select to Output in High Z	t _{CHZ'}		12	nS
Output Enable to Output in High Z	t _{OHZ'}		12	nS

1. This parameter is guaranteed by design but not tested.

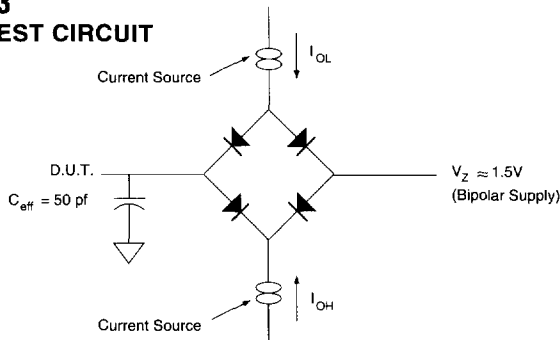
AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-20		Units
		Min	Max	
Write Cycle				
Write Cycle Time	t _{WC}	20		nS
Chip Select to End of Write	t _{CW}	15		nS
Address Valid to End of Write	t _{AW}	15		nS
Data Valid to End of Write	t _{DW}	12		nS
Write Pulse Width	t _{WP}	15		nS
Address Setup Time	t _{AS}	0		nS
Address Hold Time	t _{AH}	0		nS
Output Active from End of Write	t _{OW'}	4		nS
Write Enable to Output in High Z	t _{WHZ'}		10	nS
Data Hold Time	t _{DH}	0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 3 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75 \Omega$.
 V_z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG. 4
TIMING WAVEFORM - READ CYCLE

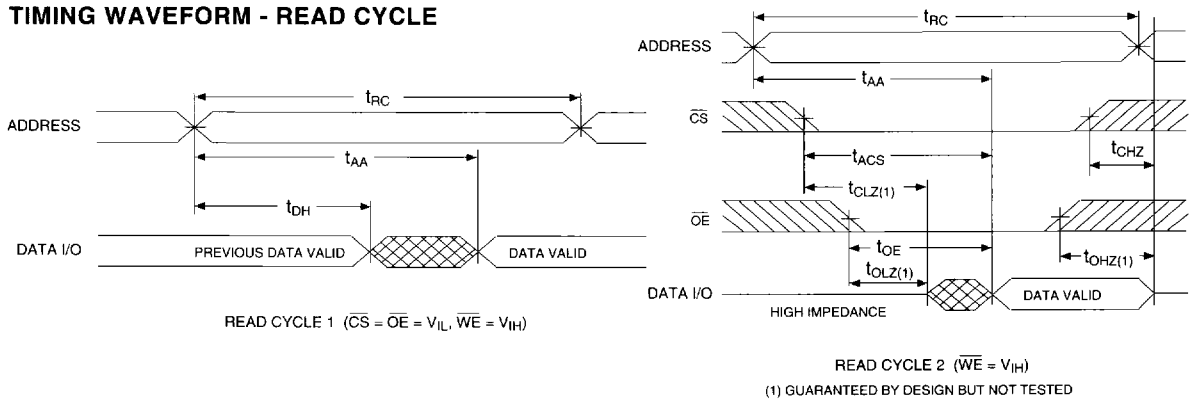


FIG. 5
WRITE CYCLE - \overline{WE} CONTROLLED
(OE IS INACTIVE - HIGH)

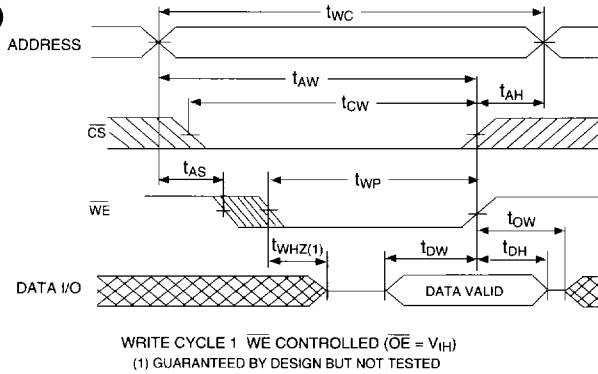
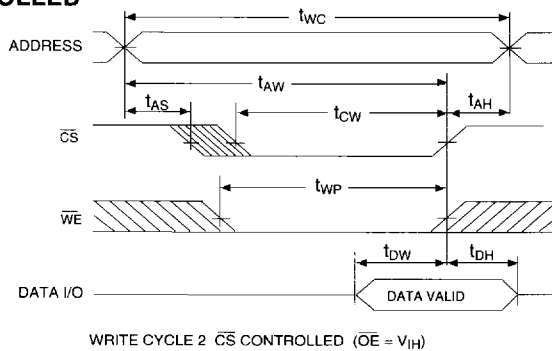


FIG. 6
WRITE CYCLE - \overline{CS} CONTROLLED



NOTE: Output enable (\overline{OE}) is inactive (HIGH).



FIG. 7
PACKAGE DIMENSIONS
(16A06)

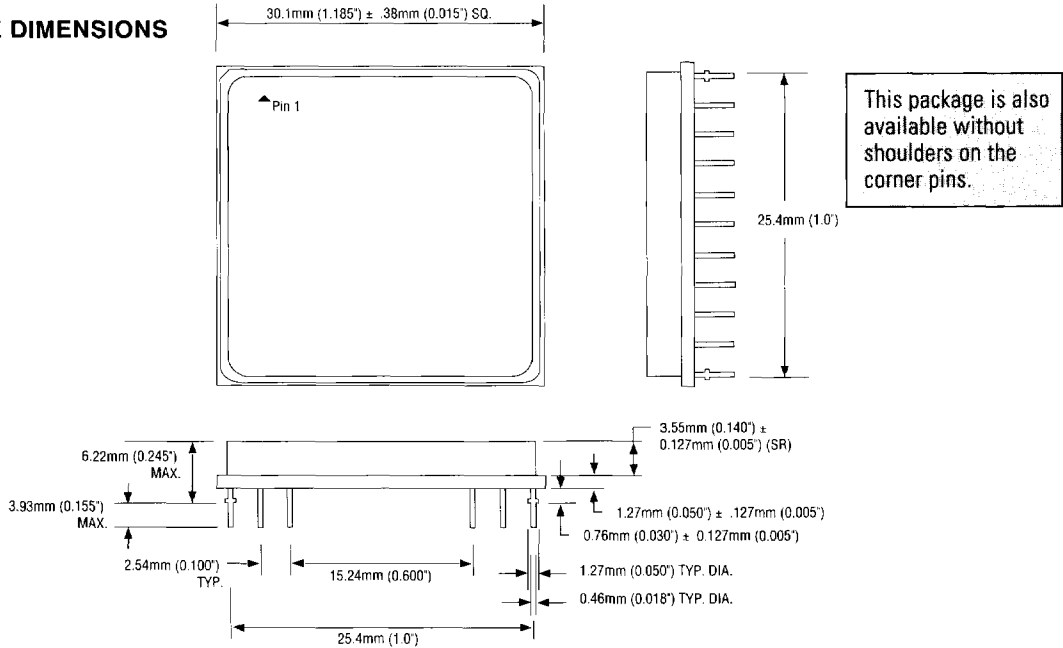
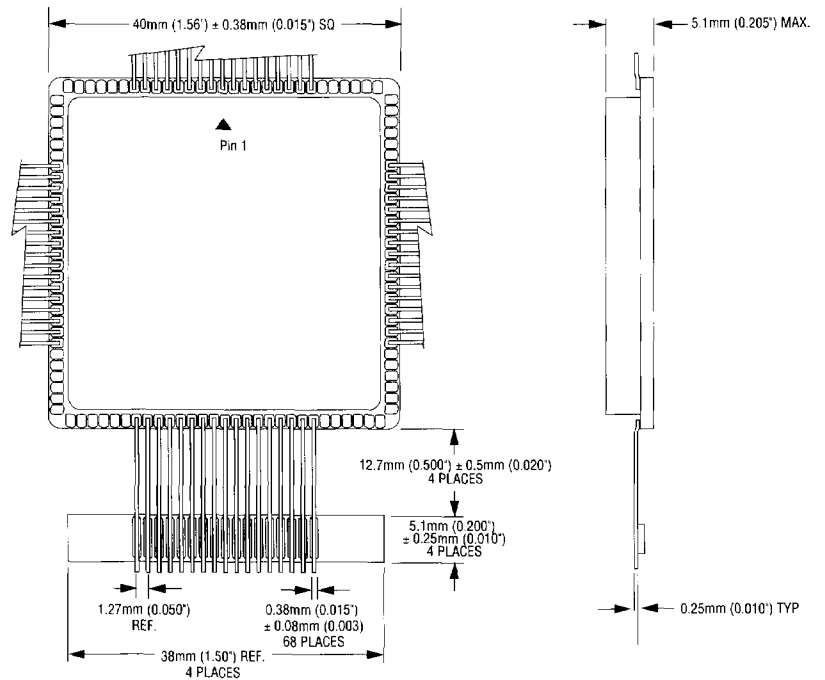


FIG. 8
PACKAGE DIMENSIONS
(14A15)





ORDERING INFORMATION

W S 128K 32 X - XXX X X

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H = Ceramic hex-in-line package
- HS = Ceramic hex-in-line package, no shoulders
- G4= 40 mm Ceramic Quad Flat Pack

ACCESS TIME in nS

IMPROVEMENT MARK:

- N = No Connect at pin 8, 21, 28 and 39
- Blank = GND at 8, 21, 28 and 39

ORGANIZATION, 128K x 32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE MICROELECTRONICS