Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

IDT7133S/L
IDT7143S/L

FEATURES:

- High-speed access
  - — Military: 55/70/90ns (max.)
  - — Commercial: 45/55/70/90ns (max.)
- Low-power operation
  - — IDT7133/43S
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7133/43L
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic or plastic PGA, LCC, PLCC, and Flatpack
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

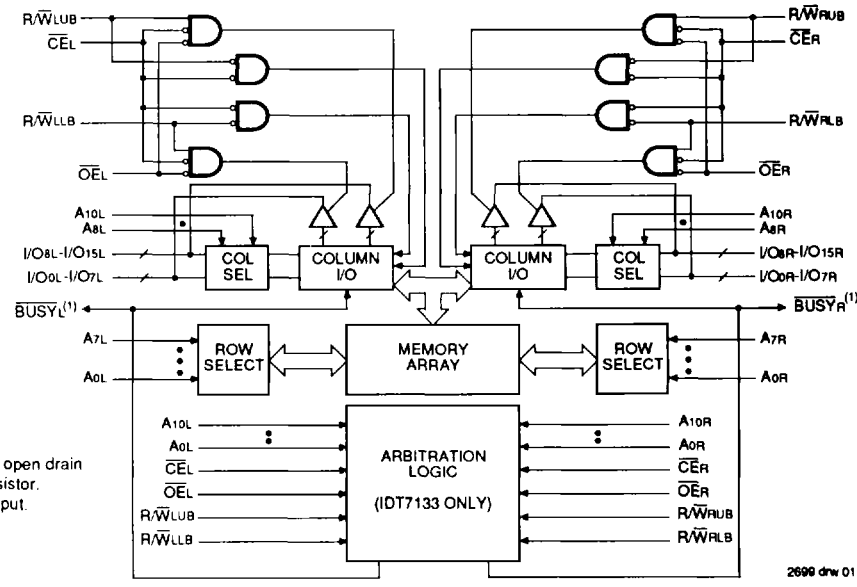
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 1mW for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed on a 68-pin ceramic or plastic PGA, 68-pin LCC, 68-pin flatpack, and 68-pin PLCC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. IDT7133 (MASTER): BUSY is open drain output and requires pull-up resistor.
   IDT7143 (SLAVE): BUSY is input.
2. LB = LOWER BYTE
3. UB = UPPER BYTE

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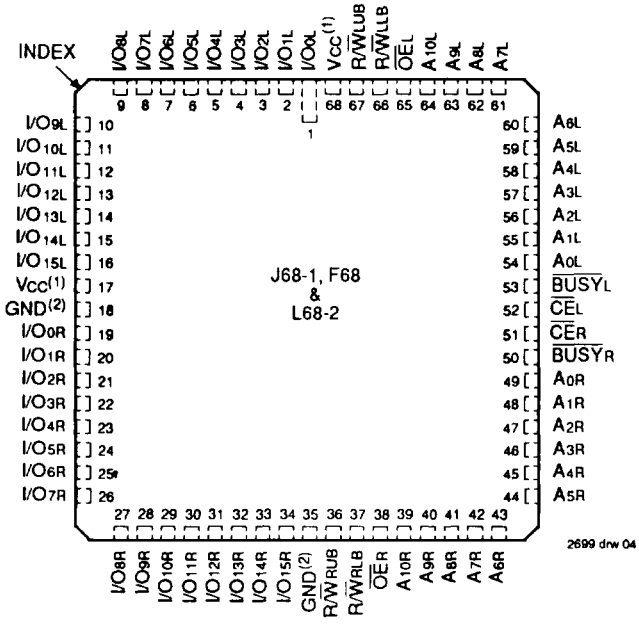
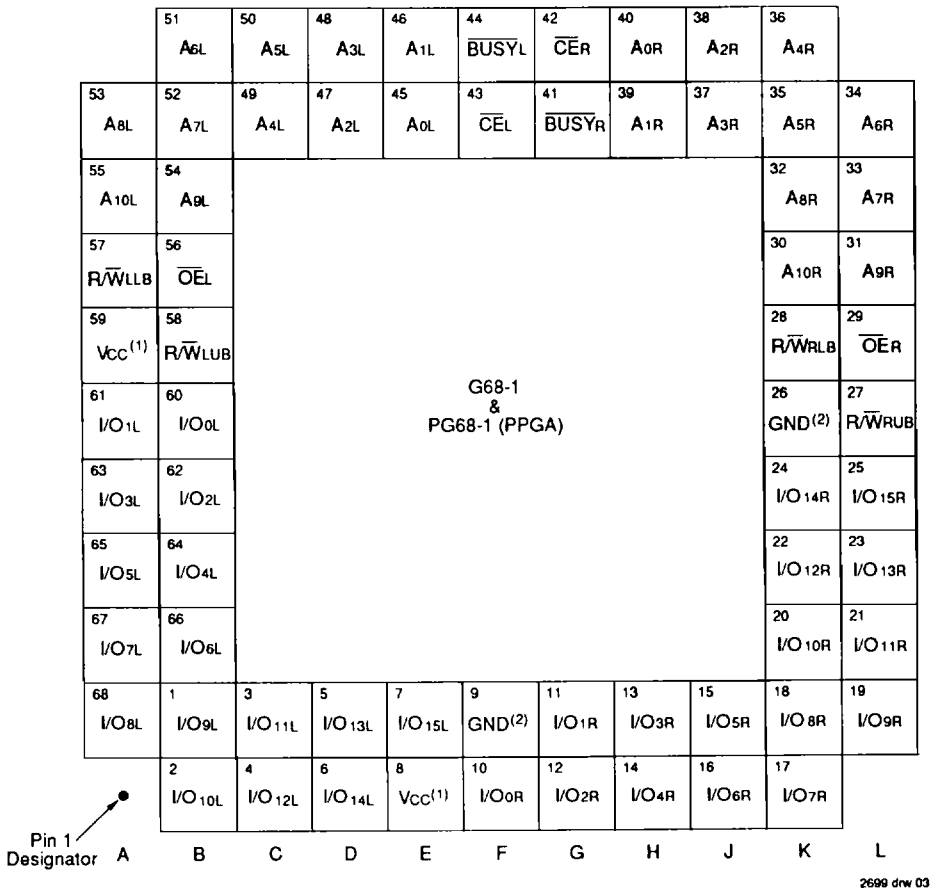
PIN CONFIGURATIONS



LCC/PLCC/FLATPACK
TOP VIEW

PIN CONFIGURATIONS (Continued)



PGA TOP VIEW (Ceramic or Plastic)

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte.

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2699 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Input/Output Capacitance	$V_{I/O}$ = 0V	11	pF

NOTE: 2699 tbl 02

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2699 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2699 tbl 04

1. V_{IL} (min) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7133S IDT7143S		IDT7133L IDT7143L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2699 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7133x45[1] IDT7143x45[1]		IDT7133x55 IDT7143x55		IDT7133x70 IDT7143x70		IDT7133x90 IDT7143x90		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	S	—	—	75	280	75	260	75	260	mA
				L	—	—	75	260	75	240	75	240	
			COM'L	S	—	260	75	240	75	240	75	235	
				L	—	240	75	220	75	220	75	215	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	MIL.	S	—	—	25	80	25	75	25	75	mA
				L	—	—	25	70	25	65	25	65	
			COM'L	S	—	75	25	70	25	70	25	65	
				L	—	65	25	60	25	60	25	55	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4] Active Port Outputs Open	MIL.	S	—	—	50	180	50	170	50	170	mA
				L	—	—	50	160	50	150	50	150	
			COM'L	S	—	160	50	150	50	150	50	145	
				L	—	140	50	130	50	130	50	125	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ - 0.2V	MIL.	S	—	—	30	30	1	30	1	30	mA
				L	—	—	10	10	0.2	10	0.2	10	
		$V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	COM'L	S	—	15	1	15	1	15	1	15	
				L	—	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (OnePort — All CMOS Level Inputs f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	S	—	—	45	170	45	160	45	155	mA
				L	—	—	40	150	40	140	40	135	
			COM'L	S	—	150	45	140	45	140	45	135	
				L	—	130	40	120	40	120	40	115	

NOTES:

2699 tbl 06

1. 0°C to +70°C temperature range only.
2. V_{CC} = 5V, T_A = +25°C.
3. "x" in part number indicates power rating (S or L).
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

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DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

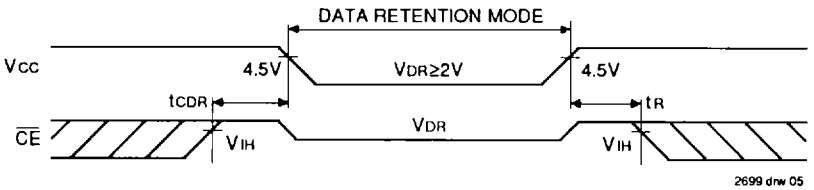
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		IDT7133/IDT7143 Min.	IDT7133/IDT7143 Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	ns
I_{LI}[3]	Input Leakage Current			—	2	µA

2699 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2699 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2699 tbl 08

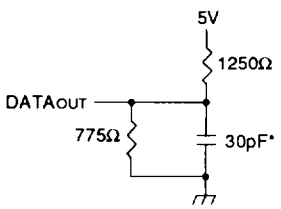


Figure 1. Output Load

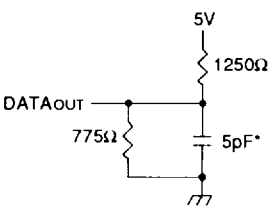
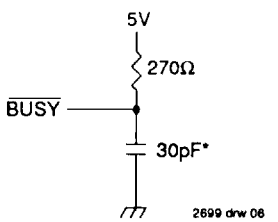


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig



2699 drw 06

Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

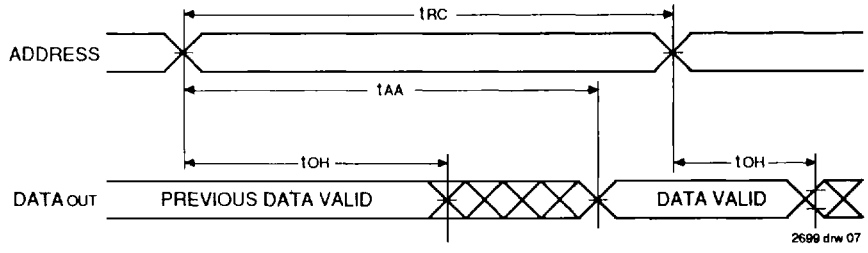
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7133S/L45[2] IDT7143S/L45[2]		IDT7133S/L55 IDT7143S/L55		IDT7133S/L70 IDT7143S/L70		IDT7133S/L90 IDT7143S/L90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	45	—	55	—	70	—	90	—	ns
tAA	Address Access Time	—	45	—	55	—	70	—	90	ns
tACE	Chip Enable Access Time	—	45	—	55	—	70	—	90	ns
tAOE	Output Enable Access Time	—	30	—	35	—	40	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	10	—	ns
tLZ	Output Low Z Time[1, 3]	0	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 3]	—	20	—	20	—	25	—	25	ns
tPU	Chip Enable to Power Up Time[3]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[3]	—	50	—	50	—	50	—	50	ns

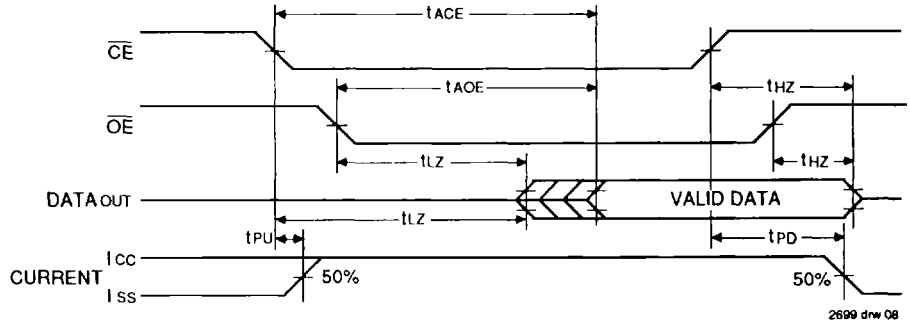
2699 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7133S/L45[2] IDT7143S/L45[2]		IDT7133S/L55 IDT7143S/L55		IDT7133S/L70 IDT7143S/L70		IDT7133S/L90 IDT7143S/L90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time[4]	45	—	55	—	70	—	90	—	ns
tEW	Chip Enable to End of Write	30	—	40	—	50	—	85	—	ns
tAW	Address Valid to End of Write	30	—	40	—	50	—	85	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	30	—	40	—	50	—	55	—	ns
tWR	Write Recovery Time	5	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time[1, 3]	—	20	—	20	—	25	—	25	ns
tDH	Data Hold Time[5]	5	—	5	—	5	—	5	—	ns
tWZ	Write Enable to Output in High Z[1, 3]	—	20	—	20	—	25	—	25	ns
tOW	Output Active from End of Write[1, 3, 5]	5	—	5	—	5	—	5	—	ns

NOTES: 2699 tbl 10

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, tWC = tBAA + tWR + tWP.
5. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).

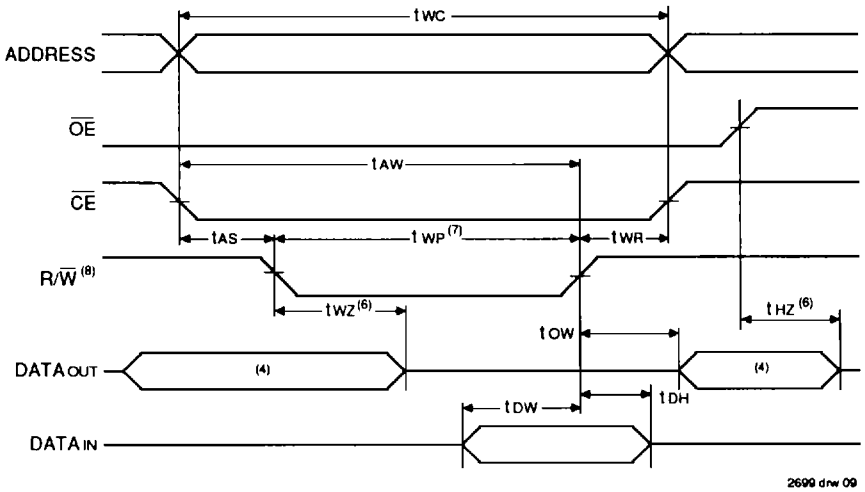
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7133S/L45[1] IDT7143S/L45[1]		IDT7133S/L55 IDT7143S/L55		IDT7133S/L70 IDT7143S/L70		IDT7133S/L90 IDT7143S/L90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (FOR MASTER IDT7133)										
tBAA	$\overline{BUSY}$ Access Time to Address	—	45	—	50	—	55	—	55	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	—	45	—	45	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	30	—	35	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	25	—	30	—	30	—	45	ns
tWDD	Write Pulse to Data Delay[2]	—	80	—	80	—	90	—	100	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	55	—	55	—	70	—	90	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 4	—	Note 4	—	Note 4	—	Note 4	ns
tAPS	Arbitration Priority Set Up Time[4]	5	—	5	—	5	—	10	—	ns
BUSY INPUT TIMING (For SLAVE IDT7143)										
tWB	Write to $\overline{BUSY}$[5]	0	—	—	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	30	—	30	—	30	—	30	—	ns
tWDD	Write Pulse to Data Delay[7]	—	80	—	80	—	90	—	100	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	55	—	55	—	70	—	90	ns

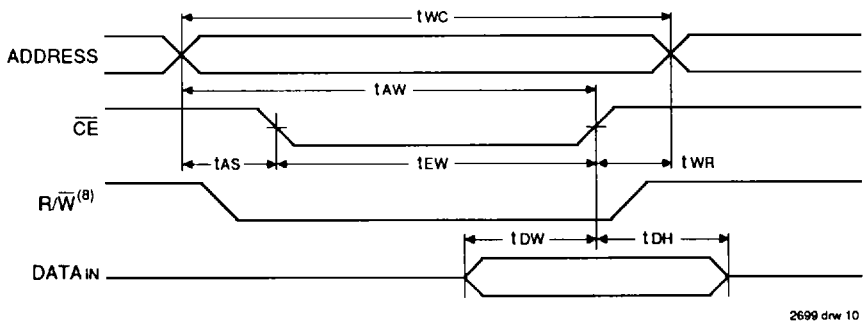
NOTES: 2699 tbl 11

1. 0°C to +70°C temperature range only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH BUSY (For Master IDT7133)"
3. tBDD is calculated parameter and is greater of 0, tWDD - tWP (actual) or tDDD - tDW (actual).
4. To ensure that the earlier of the two ports wins.
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (For Slave IDT7143)"

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



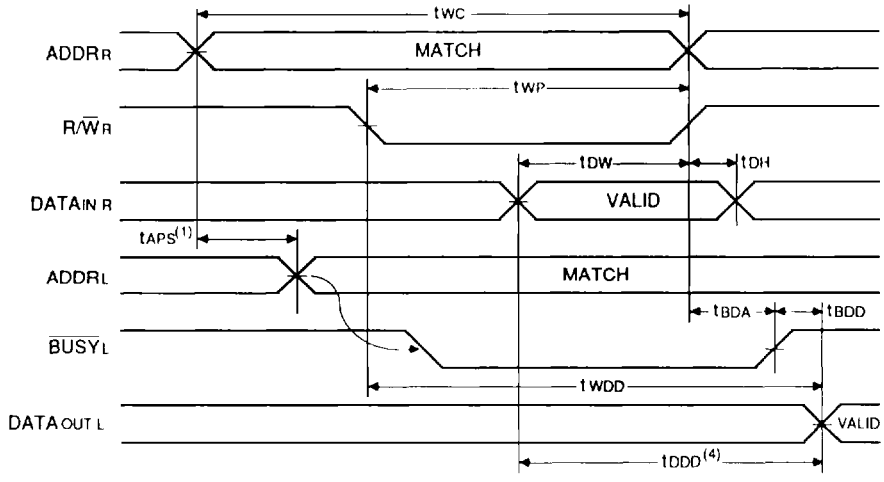
WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .
8. R/$\overline{W}$ for either upper or lower byte.

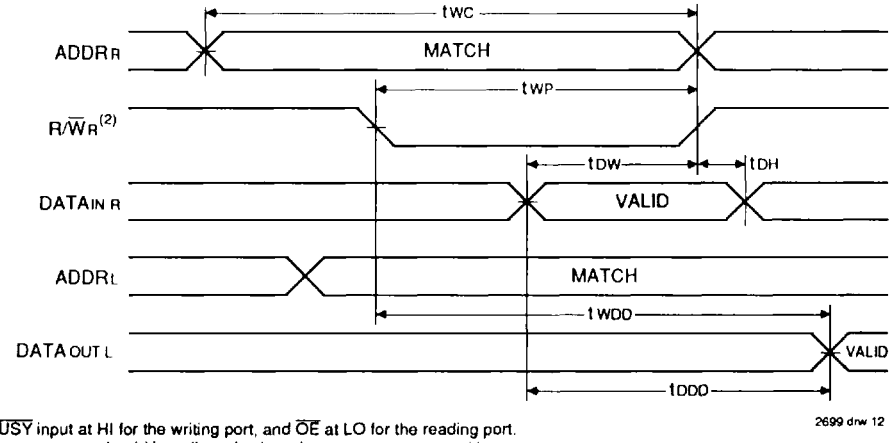
7

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$(1, 2, 3) (For MASTER IDT7133)



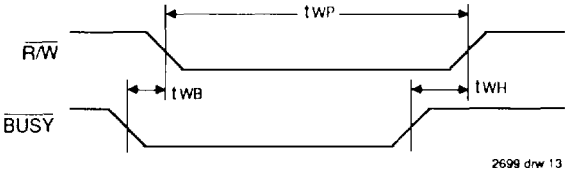
NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2, 3) (For SLAVE IDT7143)



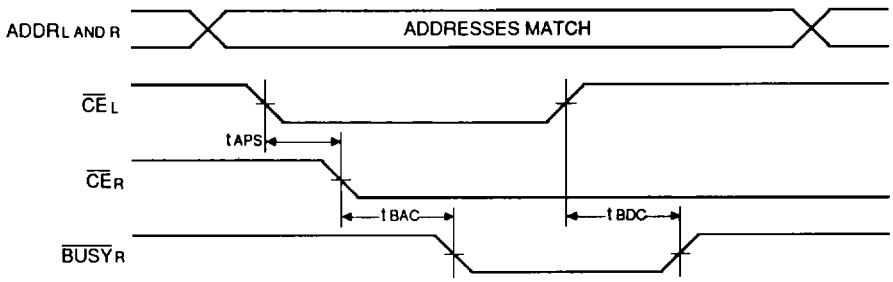
NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (For SLAVE IDT7143)

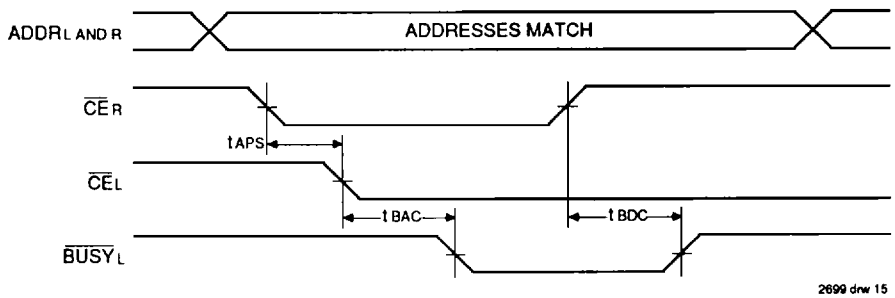


TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

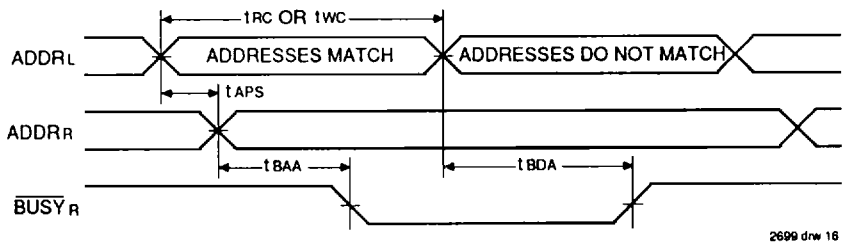


$\overline{CE}_R$ VALID FIRST:

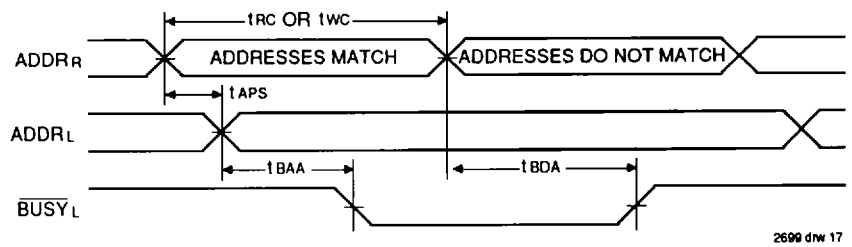


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1)

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is pemitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to 32 bits or more in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will await indefinately for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT[1]						
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory[2], Data in Memory Output on Upper Byte[3]
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte[3], Data on Upper Byte Written into Memory[2]
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory[2]
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

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NOTES:
1. A_{0L} - $A_{10L} \neq A_{0R}$ - A_{10R}
2. If $\overline{BUSY}$ = LOW, data is not written.
3. If $\overline{BUSY}$ = LOW, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance, LB = Lower Byte, UB = Upper Byte

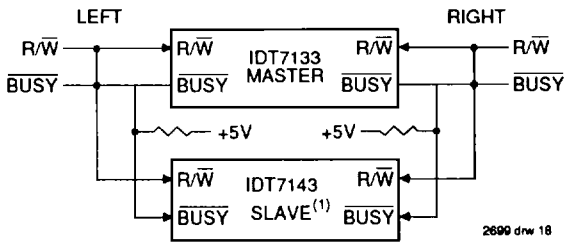
TABLE II — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS[1]		
$\overline{CE}_L$	A_{0L} - A_{10L}	$\overline{CE}_R$	A_{0R} - A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A_{0R} - A_{10R}	L	≠ A_{0L} - A_{10L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	= A_{0R} - A_{10R}	LL5R	= A_{0L} - A_{10L}	H	L	L-Port Wins
RL5L	= A_{0R} - A_{10R}	RL5L	= A_{0L} - A_{10L}	L	H	R-Port Wins
LW5R	= A_{0R} - A_{10R}	LW5R	= A_{0L} - A_{10L}	H	L	Arbitration Resolved
LW5R	= A_{0R} - A_{10R}	LW5R	= A_{0L} - A_{10L}	L	H	Arbitration Resolved

2699 tbl 12

NOTES:
1. H = HIGH, L = LOW, X = Don't Care
   LV5R = Left Address Valid ≥ 5ns before right address
   RV5L = Right Address Valid ≥ 5ns before left address
   Same = Left and Right Address match within 5ns of each other
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other

32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTES:
1. No arbitration in IDT7143 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7143 (SLAVE).

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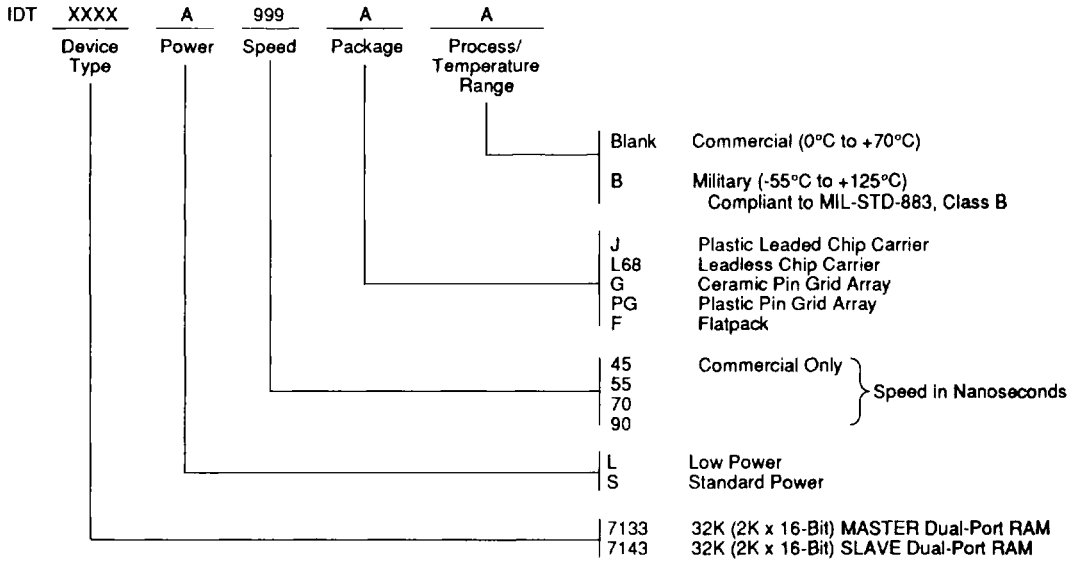
ORDERING INFORMATION



2699 drw 19