National Semiconductor

MICROCIRCUIT DATA SHEET

MDNS41256S15-X REV 0A0

Original Creation Date: 11/28/95
Last Update Date: 02/05/97
Last Major Revision Date: 11/28/95

256K Static RAM (32K x 8 bit)

General Description

NS41256S15 is a high performance, standard power version CMOS static RAM organized as 32,768 X 8 bits with 15nS address to access time. NS41256 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible.

Industry Part Number

NS41256S15

NS Part Numbers

NS41256S15E-SMD *
NS41256S15J-SMD **

Prime Die

PDM41256V

Controlling Document

5962-8866208YA*, UA** REV C

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

Truth Table:

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	FUNCTION
H	X	X	HI-Z	STANDBY (ICC2)
$\geq$ VCC -0.2V	X	X	HI-Z	STANDBY (ICC3)
L	H	H	HI-Z	OUTPUT DISABLE
L	H	L	DOUT	READ
L	L	X	DIN	WRITE

Applications

Graphic Notes: * = This note does not apply for this device.

*1. The parameter is tested with CL = 5pF as shown in Fig. 2. Transition is measured $\pm$200mV from steady state voltage.

*2. At any given temperature and voltage condition, tHZCE is less than tLZCE.

*3. This parameter is sampled.

*4. $\overline{WE}$ is high for a READ cycle.

5. The device is continously selected. All the Chip Enables are held in their active state. Applies to READ cycle 1.

6. The address is valid prior to or coincident with the latest occuring Chip Enable. Applies to READ cycle 2.

*7. Vcc = 5V $\pm$10%.

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage Range (VCC) (Note 2)	-0.5Vdc to +7.0Vdc
Input Voltage Range	-0.5Vdc to +6.0Vdc
Ambient Storage Temperature	-65 C to +150 C
Thermal Resistance Junction-to-Case (ThetaJC)	See MIL-STD-1835
Junction Temperature (TJ) (Note 3)	+150 C
Power Dissipation (PD)	1.0W
Lead Temperature (Soldering, 10 seconds)	+260 C

Note 1: Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of document 5962-88662, and will also be listed in MIL-BUL-103.
Note 2: All voltages referenced to VSS.
Note 3: Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

Recommended Operating Conditions

Supply Voltage Range (VCC) (Note 1)	4.5Vdc to 5.5Vdc
Ground Voltage (VSS)	0 Vdc
Input High Voltage Range (VIH)	2.2Vdc to Vcc +0.5Vdc
Input Low Voltage Range (VIL)	-0.5Vdc to 0.8Vdc
Operating Case Temperature (TC)	-55 C to +125 C

Note 1: All voltages referenced to VSS.

Electrical Characteristics

DC PARAMETERS: ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: -55 C ≤ Tc ≤ +125 C, Vss = 0V, 4.5V ≤ Vcc ≤ 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ILI	Input Leakage Current	Vcc = max, Vin = Gnd to Vcc				10	uA	1, 2, 3
ILO	Output Leakage Current	Vcc = max, Vout = Gnd to Vcc, $\overline{CE}$ ≥ Vih; $\overline{WE}$ ≤ Vil				10	uA	1, 2, 3
Vol	Output Low Voltage	Vcc = 4.5V, Iol = 8mA, Vil=0.8V, Vih=2.2V				0.4	V	1, 2, 3
Voh	Output High Voltage	Vcc = 4.5V, Ioh = -4mA, Vil = 0.8V, Vih = 2.2V			2.4		V	1, 2, 3

DC PARAMETERS: Maximum Operating Conditions

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: -55 C ≤ Tc ≤ +125 C, Vss = 0V, 4.5V ≤ Vcc ≤ 5.5V

Icc1	Operating Supply Current	Vcc=5.5V, f=fmax, $\overline{CE}$ = Vil, outputs open, all other inputs at Vil	1			180	mA	1, 2, 3
Icc2	Standby Power Supply Current (TTL)	$\overline{CE}$ ≥ Vih, outputs open, Vcc=5.5V				50	mA	1, 2, 3
Icc3	Standby Power Supply Current (CMOS)	$\overline{CE}$ ≥ (Vcc-0.2V), f=0MHz, outputs open, Vcc=5.5Vall other inputs ≤ 0.2V or ≥ (Vcc-0.2V)				20	mA	1, 2, 3

AC PARAMETERS: Capacitance

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: -55 C ≤ Tc ≤ +125 C, Vss = 0V, 4.5V ≤ Vcc ≤ 5.5V

Cin	Input Capacitance	Vi=5.0V or Gnd, f=1MHz, TC=+25 C	2, 6			11	pF	4
Cout	Output Capacitance	Vo=5.0V or Gnd, f=1MHz, TC=+25 C	2, 6			11	pF	4

Electrical Characteristics

AC PARAMETERS: ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: -55 C ≤ Tc ≤ +125 C, Vss = 0V, 4.5V ≤ Vcc ≤ 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tAVAV	Read Cycle Time		3		15		nS	9, 10, 11
tAVQV	Address Access Time		3			15	nS	9, 10, 11
tELQV	Chip Enable Access Time		3			15	nS	9, 10, 11
tAVQX	Output Hold after Address Change		3		3		ns	9, 10, 11
tOLQV	Output Enable to Output Valid		3, 5			8	nS	9, 10, 11
tELQX	Chip Select to Output in Low Z		2, 3, 4		3		nS	9, 10, 11
tEHQZ	Chip Deselect to Output in High Z		2, 3, 4, 5			10	nS	9, 10, 11
tOHQZ	Output Disable to Output in High Z		2, 3, 4, 5			10	nS	9, 10, 11
tWLQZ	Write Enable to Output in High Z		2, 3, 4, 5			10	nS	9, 10, 11
tOLQX	Output Enable to Output in Low Z		2, 3, 4		0		nS	9, 10, 11
tDVWH/ tDVEH	Data Valid to end of Write		3, 5		10		nS	9, 10, 11
tWHDX/ tEHDX	Data Hold Time		3		0		nS	9, 10, 11
tWHQX	Output Active from end of Write		2, 3, 4		0		nS	9, 10, 11
tAVAV	Write Cycle Time		3		15		nS	9, 10, 11
tELWH	Chip Select to end of Write		3		12		nS	9, 10, 11
tAVWH	Address Valid to end of Write		3		12		nS	9, 10, 11
tAVWL	Address-setup Time		3		0		nS	9, 10, 11
tWLWH	Write Pulse Width		3		12		nS	9, 10, 11
tWHAX/ tEHAX	Write Recovery Time		3		0		nS	9, 10, 11

Note 1: fmax = 1/tAVAV (minimum).

(Continued)

Note 2: This parameter tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
Note 3: For load circuits see figure 3 and for timing waveforms see figure 4.
Note 4: Transition is measured ±500mV from steady state voltage.
Note 5: This parameter has been tightened for device type 04. Any date code prior to the date of Rev C of this drawing may not meet this limit. See Rev B for the electrical parameter value that applies to prior date codes.
Note 6: Subgroup 4 (Cin and Cout measurements) shall be measured only for the initial test and after any process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

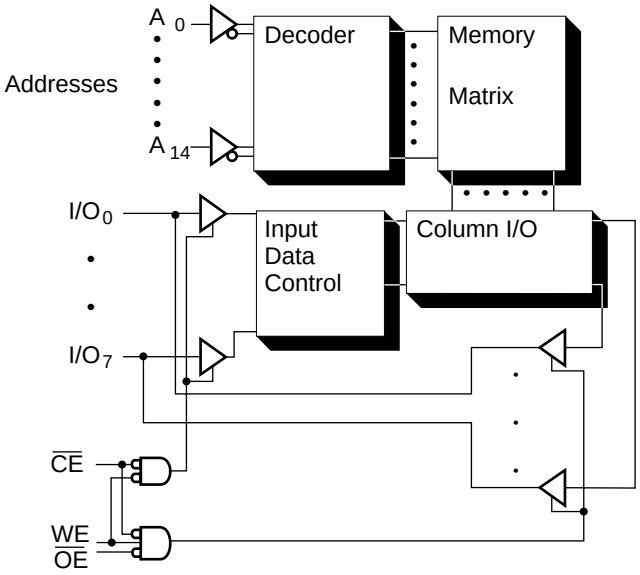
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
AN00012A	BLOCK DIAGRAM - NS41256
AN00016A	FIGURE 1 - OUTPUT LOAD EQUIVALENT
AN00017A	FIGURE 2 - OUTPUT LOAD EQUIVALENT
AN00019A	FIGURE 4 - CAPACITIVE LOADING GRAPH
AN00020A	READ CYCLE 1 (APPLICATION NOTES)
AN00022A	READ CYCLE 2 (APPLICATION NOTES)
AN00025A	WRITE CYCLE 1 - WRITE ENABLE CONTROLLED
AN00027A	WRITE CYCLE 2 - CHIP ENABLE CONTROLLED
AN00029A	LOW VCC DATA RETENTION WAVEFORM
P000141A	CERDIP (J), 28 LEAD, 300 MIL (PIN OUT)
P000142A	CERAMIC LCC (E), 32 LEAD, 450 X 550 MIL (PIN OUT)

See attached graphics following this page.

AN00012A

Functional Block Diagram



NS41256

AN00016A

Output Load Equivalent

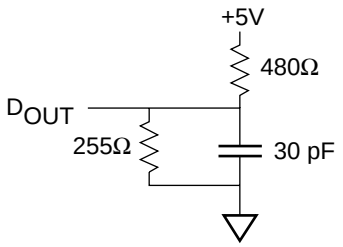


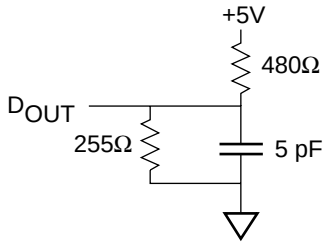
FIG. 1

AN00017A

FIG. 2

Output Load Equivalent

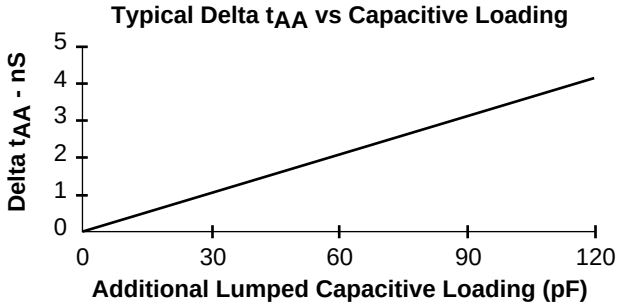
(for tLZCE, tHZWE, tLZWE, tHZWE, tLZOE, tHZOE)



NS41024
NS41096
NS41256
NS4A024
NS4A028
NS4M096
NS4R024

AN00019A

FIG. 4

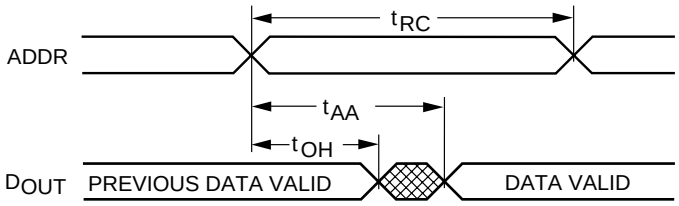


NS41256
NS41257
NS41258
NS4A024
NS4A028

AN00020A

Read Cycle #1

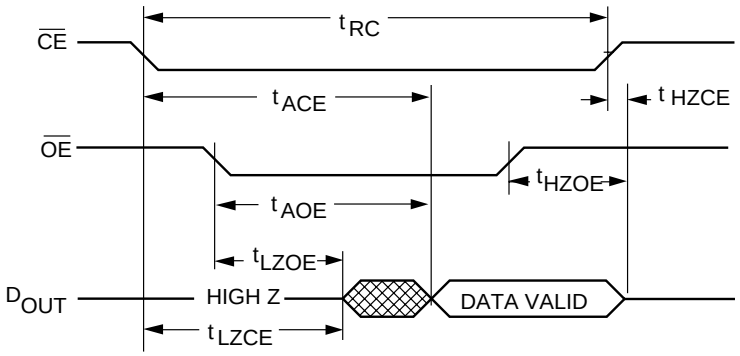
Notes : 4,5,6 apply



NS41024
NS41096
NS41256
NS41257
NS41258
NS4A024
NS4A028
NS4M096
NS4R024

AN00022A

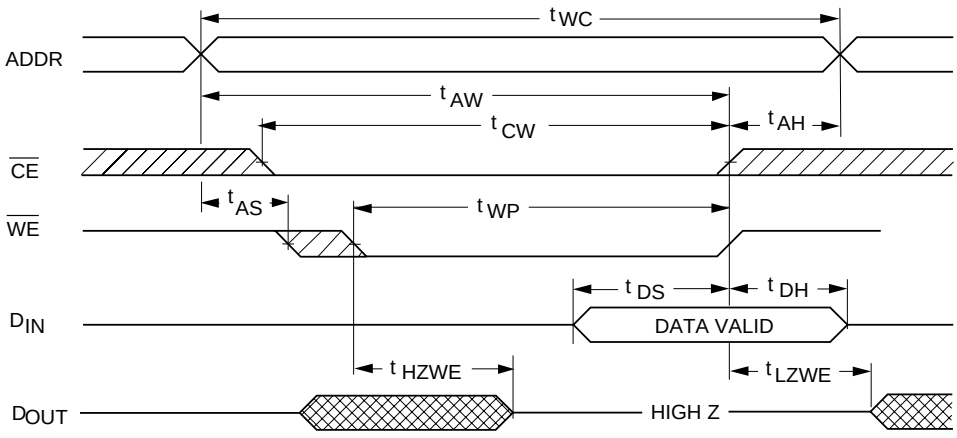
Read Cycle #2 Notes 2,4,6 & 7



NS41096
NS41256
NS4M096

AN00025A

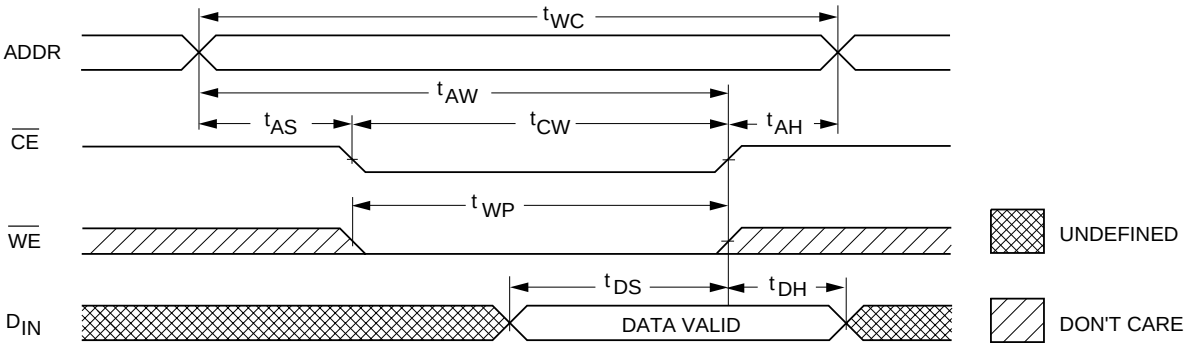
Write Cycle #1 (write enable controlled)



NS41096
NS41256
NS41257
NS41258
NS4A028
NS4M096

AN00027A

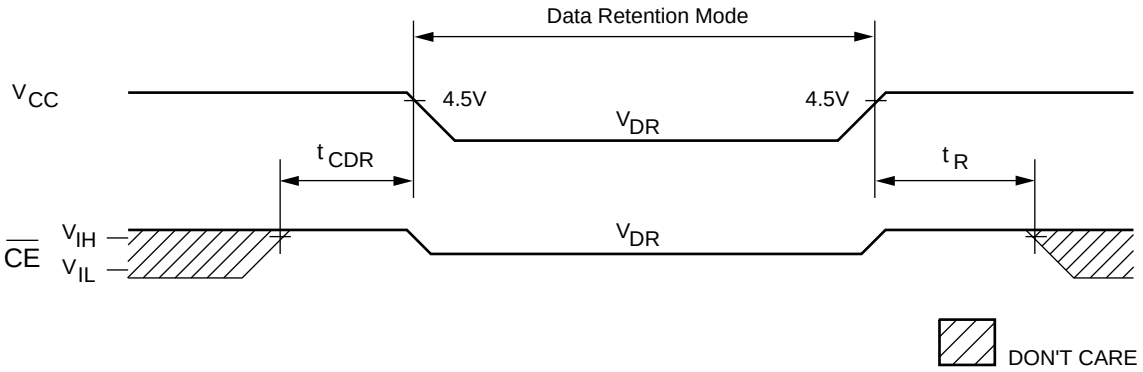
Write Cycle #2 (chip enable controlled)



NS41096
NS41256
NS41257
NS41258
NS4A028
NS4M096

AN00029A

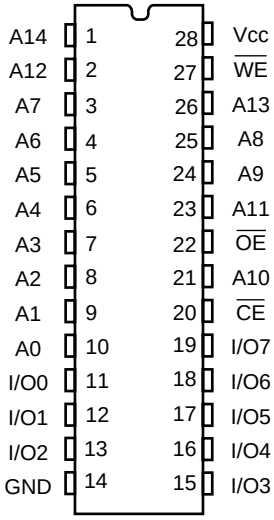
Low Vcc Data Retention Waveform



NS41096
NS41256
NS41257
NS41258
NS4A028
NS4M096

P000141A

Pin Configuration
CERDIP (J Suffix)
28LD (pinout)

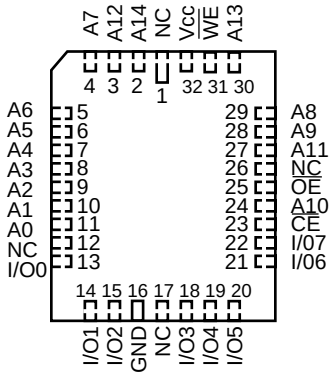


NS41256

P000142A

Pin Configuration

LCC (E Suffix) 32LD (pinout)



NS41256