

FAST 74F113 Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flops Without Reset
Product Specification

FAST Products

DESCRIPTION

The 74F113, Dual Negative Edge-Triggered JK-Type Flip-Flop, features individual J, K, Clock (\overline{CP}) and Set (\overline{S}_D) inputs, true and complementary outputs.

The asynchronous \overline{S}_D input, when Low, forces the outputs to the steady state levels as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock (\overline{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the \overline{CP} is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the \overline{CP} .

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F113	100MHz	15mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
16-Pin Plastic DIP	N74F113N
16-Pin Plastic SO	N74F113D

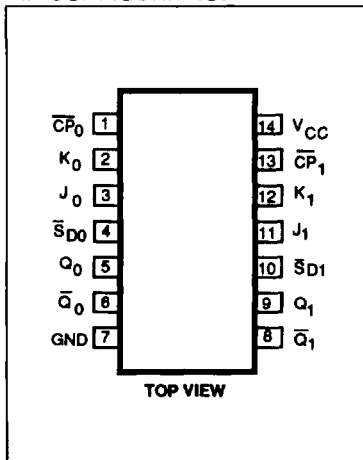
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20 μ A/0.6mA
K_0, K_1	K inputs	1.0/1.0	20 μ A/0.6mA
$\overline{S}_{D0}, \overline{S}_{D1}$	Set inputs (Active Low)	1.0/5.0	20 μ A/3.0mA
$\overline{CP}_0, \overline{CP}_1$	Clock Pulse inputs (Active rising edge)	1.0/4.0	20 μ A/2.4mA
$Q_0, \overline{Q}_0, Q_1, \overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

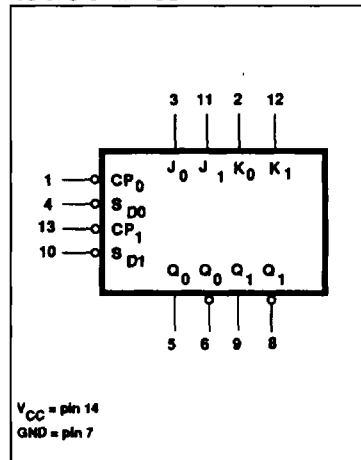
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

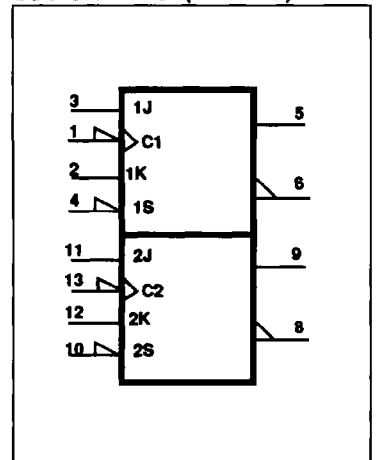
PIN CONFIGURATION



LOGIC SYMBOL



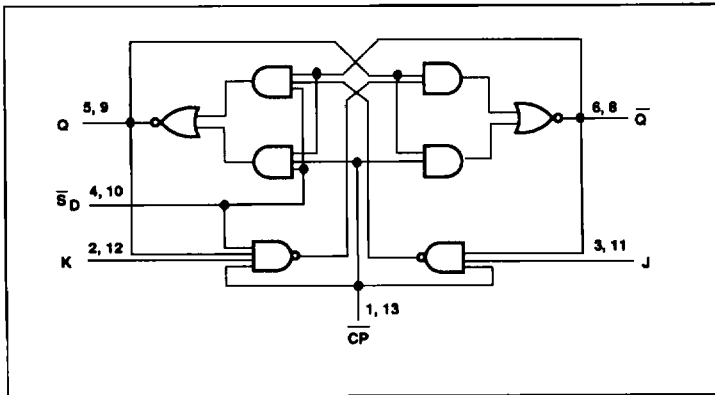
LOGIC SYMBOL (IEEE/IEC)



Flip-Flop

FAST 74F113

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
\bar{S}_0	\overline{CP}	J	K	Q	\bar{Q}	
L	X	X	X	H	L	Asynchronous Set
H	↓	h	h	\bar{q}	q	Toggle
H	↓	l	h	L	H	Load "0" (Reset)
H	↓	h	l	H	L	Load "1" (Set)
H	↓	l	l	q	\bar{q}	Hold "no change"

H = High voltage level

h = High voltage level one setup time prior to High-to-Low clock transition

L = Low voltage level

l = Low voltage level one setup time prior to High-to-Low clock transition

q = Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition

X = Don't care

↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

Flip-Flop

FAST 74F113

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			Min	Typ ²	Max		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\% V_{CC}$	2.5		V	
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\% V_{CC}$	2.7	3.4	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\% V_{CC}$		0.35	0.50	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\% V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA	
I_{IL}	Low-level input current	J_n, K_n			-0.6	mA	
		\overline{CP}_n	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-2.4	mA
		\overline{SD}_n				-3.0	mA
I_{OS}	Short circuit output current ³	$V_{CC} = \text{MAX}$		-60	-150	mA	
I_{CC}	Supply current (total) ⁴	$V_{CC} = \text{MAX}$		15	21	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
- Measure I_{CC} with the clock input grounded and all outputs open, with the Q and \overline{Q} outputs High in turn.

Flip-Flop

FAST 74F113

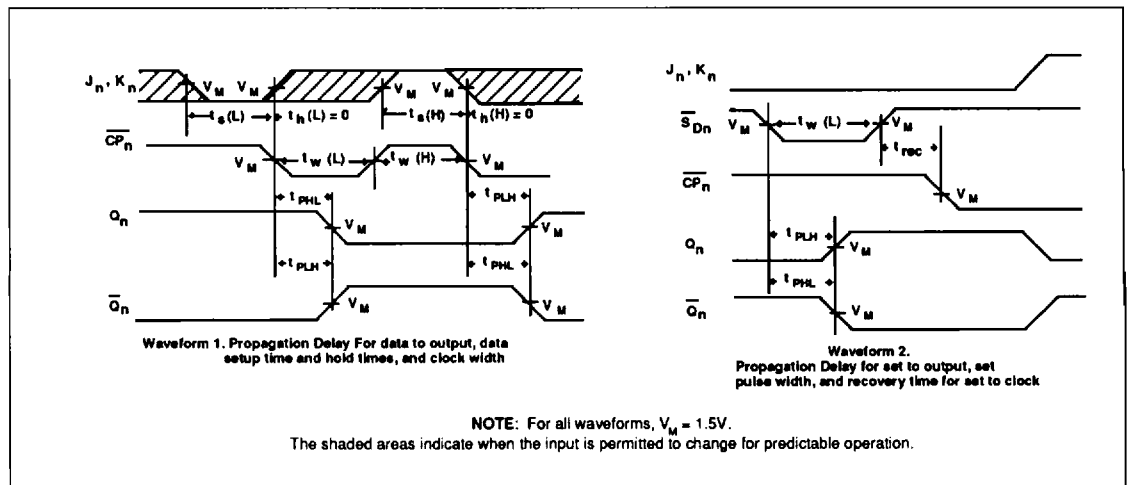
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or \bar{Q}_n	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay \bar{S}_{Dn} to Q_n or \bar{Q}_n	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, K_n to CP_n	Waveform 1	4.0 3.5			5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, K_n to CP_n	Waveform 1	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP_n Pulse width, High or Low	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	\bar{S}_{Dn} Pulse width, Low	Waveform 2	4.5			5.0		ns
t_{REC}	Recovery time \bar{S}_{Dn} to CP_n	Waveform 2	4.5			5.0		ns

AC WAVEFORMS



Flip-Flop

FAST 74F113

TEST CIRCUIT AND WAVEFORMS

Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns