SPEED/PACKAGE AVAILABILITY

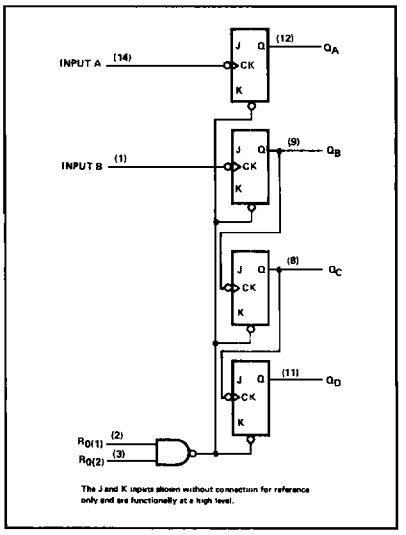
54	A,F,W	74	A,F
54LS	F,W	74LS	A,F

DESCRIPTION

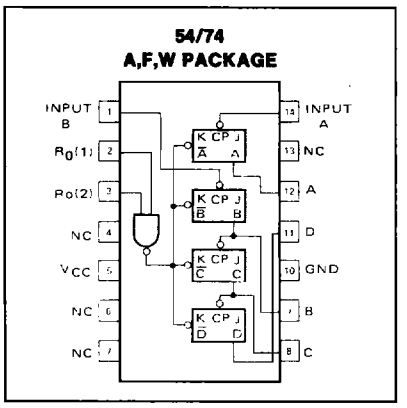
This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-eight.

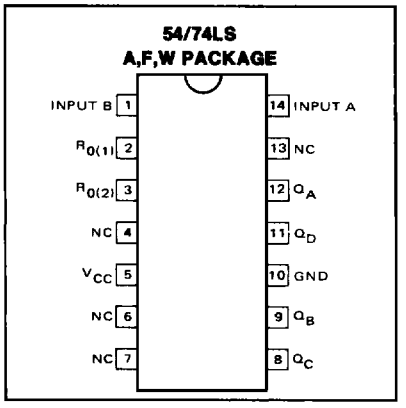
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

BLOCK DIAGRAM



PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency			10	18					MHz
		A	Q_A				32	42		
		B	Q_B				16			
t_w	Width of pulse			50						ns
		A	Q				15			
		B	Q				30			
		Reset	Q	50			15			
t_{Setup}	Input setup time						25			ns
Propagation delay time										
t_{PLH}	Low-to-high	Input Count Pulse	Q_D		75	135				ns
t_{PHL}	High-to-low				75	135				
t_{PLH}	Low-to-high	A	Q_A					10	16	
t_{PHL}	High-to-low							12	18	
t_{PLH}	Low-to-high	A	Q_D					46	70	
t_{PHL}	High-to-low							46	70	
t_{PLH}	Low-to-high	B	Q_B					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_C					21	32	
t_{PHL}	High-to-low							23	35	
t_{PLH}	Low-to-high	B	Q_D					34	51	
t_{PHL}	High-to-low							34	51	
t_{PHL}	High-to-low	Set-to-0	Any					26	40	

COUNT SEQUENCE

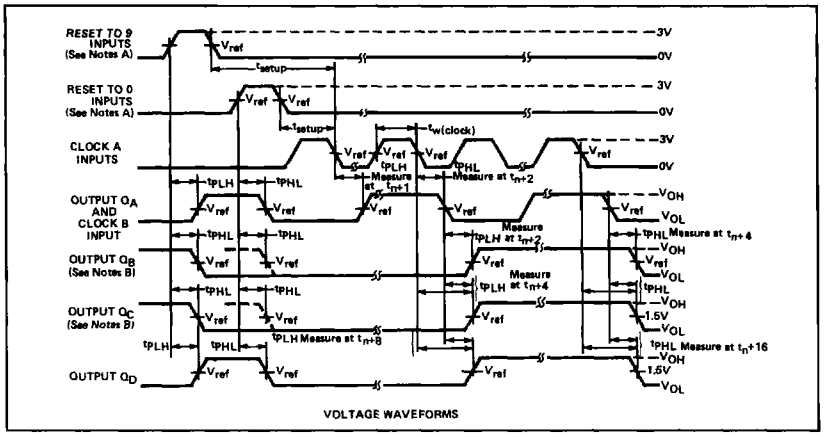
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

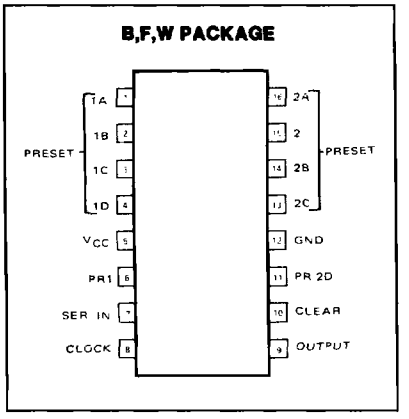
NOTES:

A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.8 V.
Load circuit shown at front of book (for totem pole outputs).

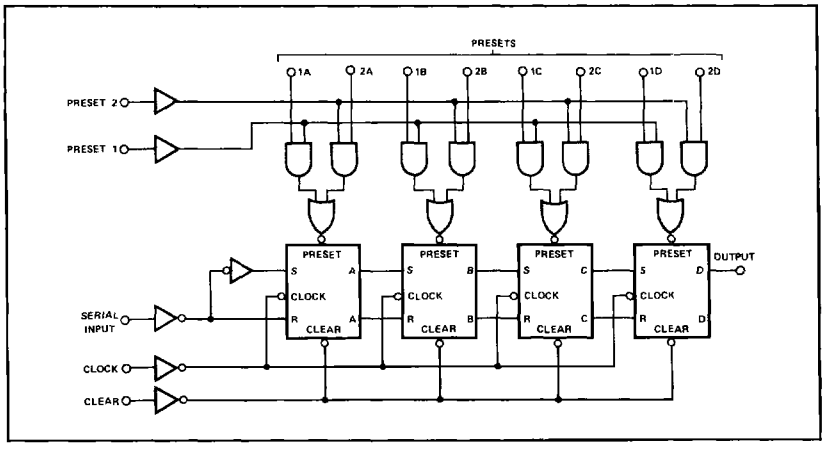
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION



LOGIC DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF R_L = 400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			10			MHz
$t_{w(Clock)}$	Width of clock pulse			35			ns
$t_{w(Clear\ \&\ Preset)}$	Width of clear and preset pulse			30			ns
t_{Setup}	Input setup time						
	High level			35			ns
	Low level			25			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Clock			25	40	ns
t_{PHL}	High-to-low				25	40	
t_{PLH}	Low-to-high	Preset				35	
t_{PHL}	High-to-low	Clear				40	

Load circuit and typical waveforms are shown at the front of section.

4-BIT PARALLEL-ACCESS SHIFT REGISTER 54/7495/95B

SPEED/PACKAGE AVAILABILITY

54 F 74 A,F
54LS F,W 74LS A,F

DESCRIPTION

This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three modes of operation:

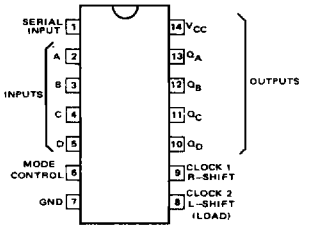
Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

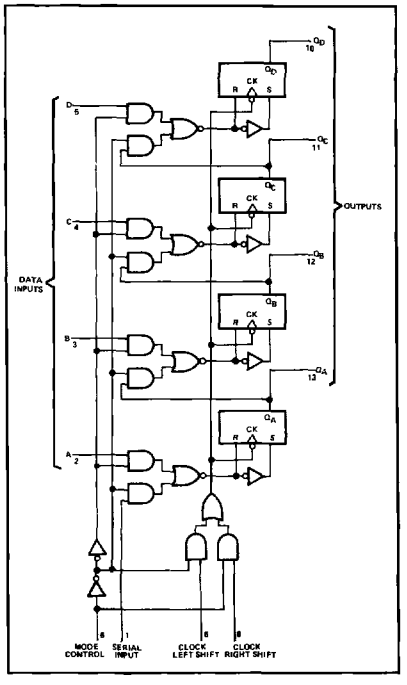
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

PIN CONFIGURATION

A,F,W PACKAGE



BLOCK DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS			
MODE	CLOCKS			PARALLEL							
CONTROL	2(L)	1(R)	SERIAL	A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B*	Q_C*	Q_D*	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

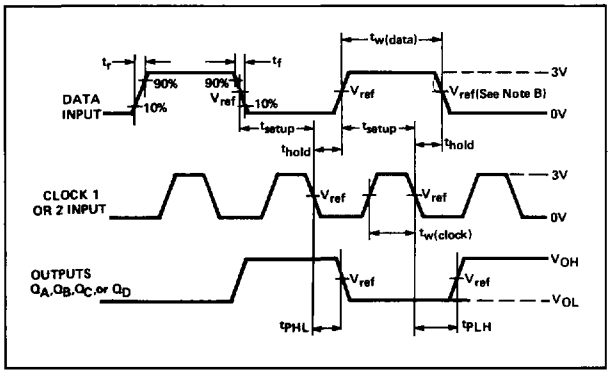
*Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0} Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS		54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Max}		25	36		25	36		MHz
$t_{w(Clock)}$	Width of clock pulse	(54) 20	10		25			ns
		(74) 15	10					
t_{Setup}	Input setup time	10			20↓			ns
t_{Hold}	Input hold time	0			10↓			ns
$t_{Enable\ 1}$	Time to enable clock 1	15			20↓			ns
$t_{Enable\ 2}$	Time to enable clock 2	15			20↓			ns
$t_{Inhibit\ 1}$	Time to enable clock 1	5			20↑			ns
$t_{Inhibit\ 2}$	Time to inhibit clock 2	5			20↑			ns
Propagation delay time								
t_{PLH}	Low-to-high (CLK)		18	27		18	27	ns
t_{PHL}	High-to-low (CLK)		21	32		21	32	

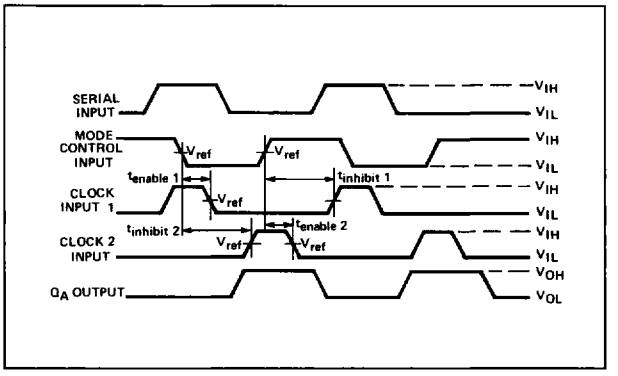
LOGIC

PARAMETER MEASUREMENT INFORMATION



SWITCHING TIMES

NOTES:
A. When testing f_{Clock} vary PRR. $t_{w(Data)} \geq 20$ ns. $t_{w(Clock)} \geq 15$ ns.
B. $V_{ref} = 1.3$v
Load circuit shown at front of book (totem pole outputs).



CLOCK ENABLE/INHIBIT TIMES

NOTES:
A. Input A is at a low level.
B. $V_{ref} = 1.3$ V.

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

DESCRIPTION

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

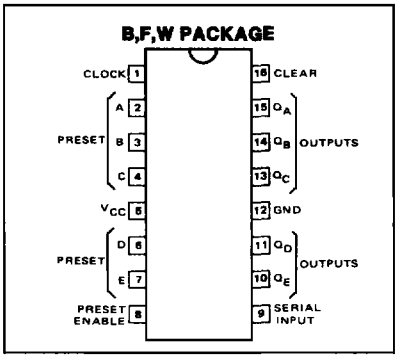
All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

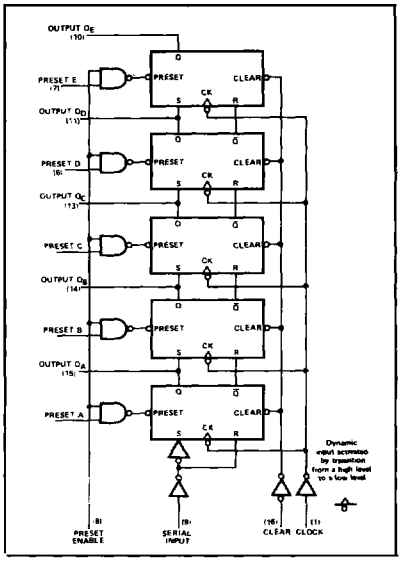
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

PIN CONFIGURATION

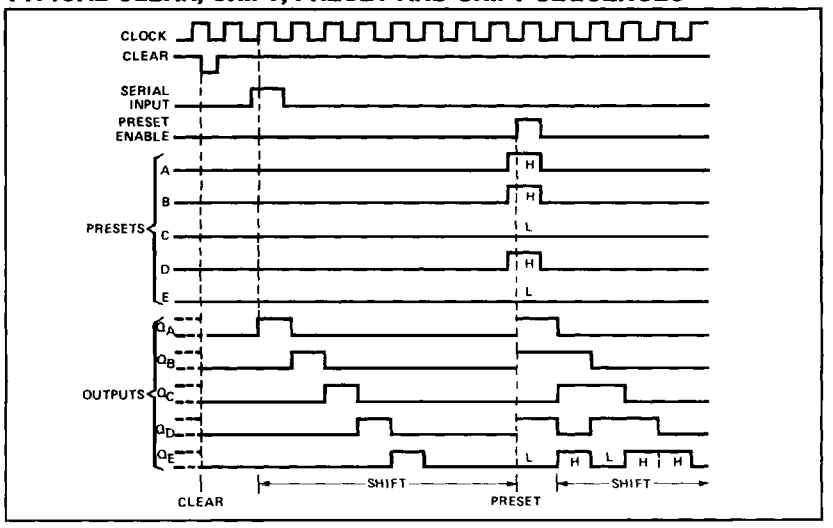
B,F,W PACKAGE



FUNCTIONAL BLOCK DIAGRAM



TYPICAL CLEAR, SHIFT, PRESET AND SHIFT SEQUENCES

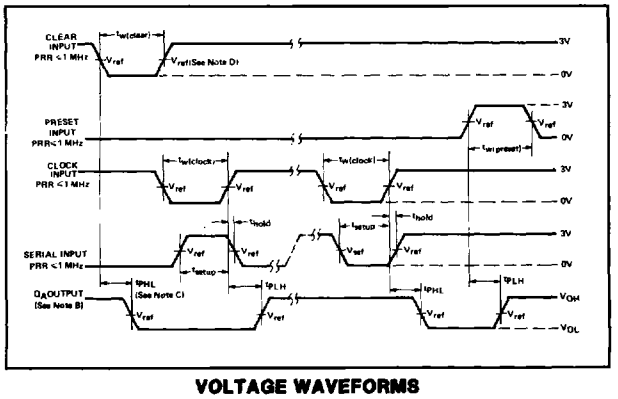


FUNCTION TABLE

INPUTS									OUTPUTS				
		PRESET											
CLEAR	PRESET ENABLE	A	B	C	D	E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	↑	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	↑	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	↑	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most recent ↑ transition of the clock.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
B. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift squence.
C. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
D. V_{ref} = 1.3V
Load circuit shown at front of book (totem pole outputs.)

LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

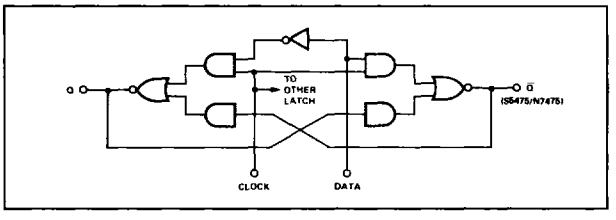
TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			10			10			MHz
$t_{w(Clock)}$	Width of clock pulse			35			35			ns
$t_{w(Preset\ \&\ Clear)}$	Width preset & clear pulse			30			30			ns
t_{Setup}	Input setup time			30			30↑			ns
t_{Hold}	Input hold time			0			0↑			ns
Propagation delay time										
t_{PLH}	Low-to-high	Clock			25	40		25	40	ns
t_{PHL}	High-to-low				25	40		25	40	
t_{PLH}	Low-to-high	Preset				35				
t_{PHL}	High-to-low				28	40				
t_{PLH}	Low-to-high	Preset, Preset Enable						28	35	
t_{PHL}	High-to-low	Clear				55			55	

4-BIT BISTABLE LATCH 54/74100

SPEED/PACKAGE AVAILABILITY

54 Q,F 74 N,F

LOGIC DIAGRAM



TRUTH TABLE

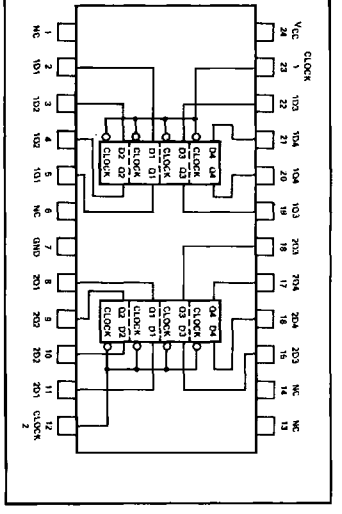
(Each Latch)	
t_n	t_n+1
D	Q
1	1
0	0

NOTES:
1. t_n = bit time before clock negative going transition.
2. t_n+1 = bit time after clock negative-going transition.

NC — No internal connection.

PIN CONFIGURATION

F,Q,N PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
t_w	Width of Pulse			20			ns
t_{Setup}	Input setup time			20			ns
Propagation delay time							
t_{PLH}	Low-to-high	D	Q		16	30	ns
t_{PHL}	High-to-low				14	25	
t_{PLH}	Low-to-high	C	Q		16	30	
t_{PHL}	High-to-low				7	15	

Load circuit and typical waveforms are shown at the front of section.

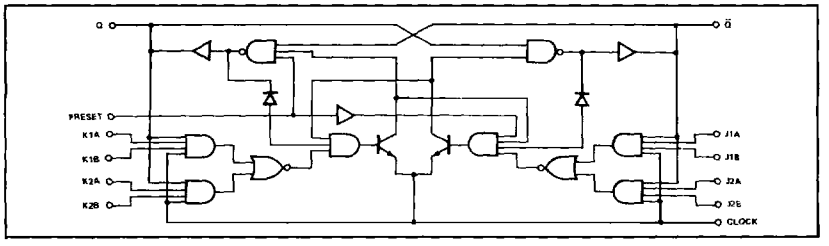
J-K EDGE-TRIGGERED FLIP-FLOP 54/74101

LOGIC

SPEED/PACKAGE AVAILABILITY

54H F,W 74H A,F

LOGIC DIAGRAM



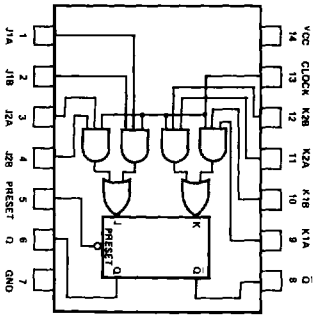
TRUTH TABLE

t_n t_{n+1}		
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

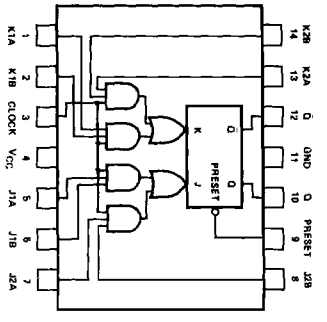
NOTES:
1. J=(J1A•J1B)+(J2A•J2B)
2. K=(K1A•K1B)+(K2A•K2B)
3. t_n=Bit time before clock pulse
4. t_{n+1}=Bit time after clock pulse

PIN CONFIGURATION

AF PACKAGE



W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=25pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			40	50		MHz
$t_{w(Clock)}$	Width of clock pulse						
	High level			10			ns
	Low level			15			
$t_{w(Clear)}$	Width of clear pulse			16			ns
t_{Setup}	Input setup time						
	Data high			10			ns
	Data low			13			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Preset			8	12	ns
t_{PHL}	High-to-low						
t_{PHL}	Clock low				23	35	
	Clock high				15	20	
t_{PLH}	Low-to-high	Clock		5	10	15	
t_{PHL}	High-to-low			8	16	20	

Load circuit and typical waveforms are shown at the front of section.

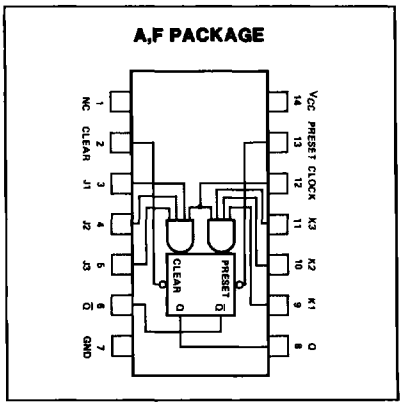
J-K EDGE-TRIGGERED FLIP-FLOP WITH AND INPUTS — 54/74102

SPEED/PACKAGE AVAILABILITY

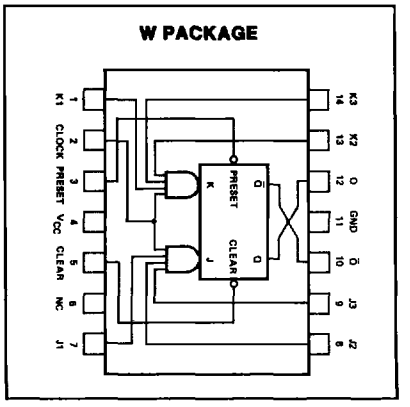
54H F,W 74H A,F

PIN CONFIGURATION

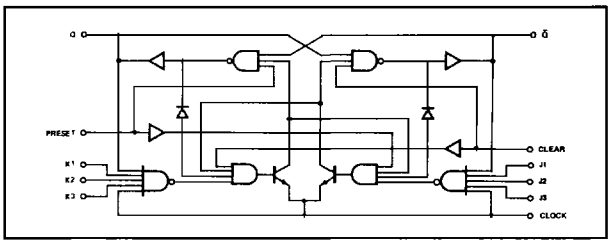
A,F PACKAGE



W PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse.
4. t_n+1 = bit time after clock pulse.
5. NC – no internal connection.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=25pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			40	50		MHz
$t_{w(Clock)}$	Width of clock pulse						
	High level			10			ns
	Low level			15			
$t_{w(Clear)}$	Width of clear pulse			15			ns
t_{Setup}	Input setup time						
	Data high			10			ns
	Data low			13			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Preset			8	12	ns
t_{PHL}	High-to-low						
	Clock Low				23	35	
	Clock high				15	20	
t_{PLH}	Low-to-high	Clock		5	10	15	
t_{PHL}	High-to-low			8	16	20	

Load circuit and typical waveforms are shown at the front of section.