

DIGITAL INTEGRATED CIRCUITS



T. T. L. SERIES

T. T. L. LOW POWER SCHOTTKY

β 74LS00	β 74LS20	β 74LS55	β 74LS161
β 74LS02	β 74LS21	β 74LS74	β 74LS162
β 74LS03	β 74LS22	β 74LS86	β 74LS163
β 74LS04	β 74LS27	β 74LS123	β 74LS174
β 74LS05	β 74LS28	β 74LS125	β 74LS175
β 74LS08	β 74LS30	β 74LS126	β 74LS241
β 74LS09	β 74LS32	β 74LS132	β 74LS253
β 74LS10	β 74LS33	β 74LS136	β 74LS257
β 74LS11	β 74LS37	β 74LS138	β 74LS258
β 74LS12	β 74LS38	β 74LS153	β 74LS266
β 74LS13	β 74LS40	β 74LS157	β 74LS386
β 74LS14	β 74LS51	β 74LS158	
β 74LS15	β 74LS54	β 74LS160	

T. T. L. STANDARD

β 5400 (CDB 400EM)	β 5454 (CDB 454EM)	β 7400 (CDB 400E)	β 7454 (CDB 454E)
β 5402 (CDB 402EM)	β 5460 (CDB 460EM)	β 7402 (CDB 402E)	β 7460 (CDB 460E)
β 5403 (CDB 403EM)	β 5472 (CDB 472EM)	β 7403 (CDB 403E)	β 7472 (CDB 472E)
β 5404 (CDB 404EM)	β 5473 (CDB 473EM)	β 7404 (CDB 404E)	β 7473 (CDB 473E)
β 5405 (CDB 405EM)	β 5474 (CDB 474EM)	β 7405 (CDB 405E)	β 7474 (CDB 474E)
β 5406 (CDB 406EM)	β 5475 (CDB 475EM)	β 7406 (CDB 406E)	β 7475 (CDB 475E)
β 5407 (CDB 407EM)	β 5476 (CDB 476EM)	β 7407 (CDB 407E)	β 7476 (CDB 476E)
β 5408 (CDB 408EM)	β 5481 (CDB 481EM)	β 7408 (CDB 408E)	β 7481 (CDB 481E)
β 5409 (CDB 409EM)	β 5483 (CDB 483EM)	β 7409 (CDB 409E)	β 7483 (CDB 483E)
β 5410 (CDB 410EM)	β 5486 (CDB 486EM)	β 7410 (CDB 410E)	β 7486 (CDB 486E)
β 5413 (CDB 413EM)	β 5490 (CDB 490EM)	β 7413 (CDB 413E)	β 7490 (CDB 490E)
β 5416 (CDB 416EM)	β 5492 (CDB 492EM)	β 7416 (CDB 416E)	β 7492 (CDB 492E)
β 5417 (CDB 417EM)	β 5493 (CDB 493EM)	β 7417 (CDB 417E)	β 7493 (CDB 493E)
β 5420 (CDB 420EM)	β 5495 (CDB 495EM)	β 7420 (CDB 420E)	β 7495 (CDB 495E)
β 5430 (CDB 430EM)	β 54121 (CDB 4121EM)	β 7430 (CDB 430E)	β 74121 (CDB 4121E)
β 5432 (CDB 432EM)	β 54123 (CDB 4123EM)	β 7432 (CDB 432E)	β 74123 (CDB 4123E)
β 5437 (CDB 437EM)	β 54151 (CDB 4151EM)	β 7437 (CDB 437E)	β 74151 (CDB 4151E)
β 5438 (CDB 438EM)	β 54153 (CDB 4153EM)	β 7438 (CDB 438E)	β 74153 (CDB 4153E)
β 5440 (CDB 440EM)	β 54157 (CDB 4157EM)	β 7440 (CDB 440E)	β 74157 (CDB 4157E)
β 5442 (CDB 442EM)	β 54180 (CDB 4180EM)	β 7442 (CDB 442E)	β 74180 (CDB 4180E)
β 5446 (CDB 446EM)	β 54192 (CDB 4192EM)	β 7446 (CDB 446E)	β 74192 (CDB 4192E)
β 5447 (CDB 447EM)	β 54193 (CDB 4193EM)	β 7447 (CDB 447E)	β 74193 (CDB 4193E)
β 5450 (CDB 450EM)	β 5837 (CDB 837EM)	β 7450 (CDB 450E)	β 7837 (CDB 837E)
β 5451 (CDB 451EM)	β 5838 (CDB 838EM)	β 7451 (CDB 451E)	β 7838 (CDB 838E)
β 5453 (CDB 453EM)		β 7453 (CDB 453E)	β 78136 (CDB 8136E)

T. T. L. HIGH SPEED

β 54H00 (CDB 400HEM)	β 54H40 (CDB 440HEM)	β 74H00 (CDB 400HE)	β 74H40 (CDB 440HE)
β 54H10 (CDB 410HEM)	β 54H51 (CDB 451HEM)	β 74H10 (CDB 410HE)	β 74H51 (CDB 451HE)
β 54H11 (CDB 411HEM)	β 54H54 (CDB 454HEM)	β 74H11 (CDB 411HE)	β 74H54 (CDB 454HE)
β 54H30 (CDB 430HEM)		β 74H30 (CDB 430HE)	

Family	Operating Temperature Range	Power Supply range
β 74...	0 °C ... + 70 °C	4.75 V ... 5.25 V
β 54...	-55 °C ... +125 °C	4.50 V ... 5.50 V

Basic Characteristics per NAND Gate @ V_{CC} = 5 V , T_A = 25 °C

Parameter	Value			Unit
	74LS...	54/74...	54H/74H...	
V _{IH} min	2	2	2	V
V _{IL} max	0.7/0.8	0.8	0.8	V
V _{IK} max @ 10 mA	1.5	1.8	1.8	V
I _{IH} max	20	40	50	uA
I _{IL} max	0.4	1.6	2	mA
V _{OL} max	0.4/0.5	0.4	0.4	V
V _{OH} min	2.5/2.7	2.4	2.4	V
I _{OL} max	4 / 8	16	20	mA
I _{OH} max	0.4	0.8	1.0	mA
I _{OS}	15 ... 100	18 ... 55	40 ... 100	mA
I _{CC} typ @ V _{OL}	0.6	3.0	6.5	mA
I _{CC} typ @ V _{OH}	0.2	1.0	2.5	mA
P _d medium	2	10	22	mW
t _{pLH} typ	9	12	6	ns
t _{pHL} typ	10	8	6.5	ns

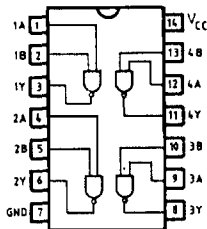
QUAD 2-INPUT NAND GATES

Function : $Y = \overline{A \cdot B}$

β 74LS00

β 7400 (CDB 400E)
β 5400 (CDB 400EM)

β 74H00 (CDB 400HE)
β 54H00 (CDB 400HEM)

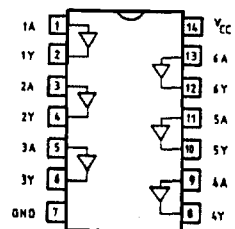


PACKAGE TO-116

HEX BUFFERS WITH 30V OPEN-COLLECTOR

Function : $Y = A$

β 7407 (CDB 407E)
β 5407 (CDB 407EM)



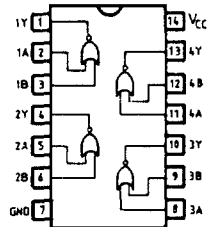
PACKAGE TO-116

QUAD 2-INPUT NOR GATES

Function : $Y = \overline{A + B}$

β 74LS02

β 7402 (CDB 402E)
β 5402 (CDB 402EM)



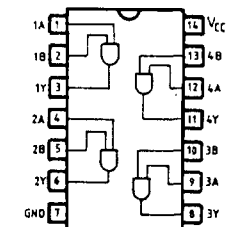
PACKAGE TO-116

QUAD 2-INPUT AND GATES

Function : $Y = A \cdot B$

β 74LS08

β 7408 (CDB 408E)
β 5408 (CDB 408EM)



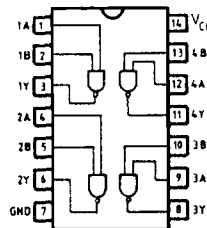
PACKAGE TO-116

QUAD 2-INPUT NAND GATES WITH OPEN-COLLECTOR

Function : $Y = \overline{A \cdot B}$

β 74LS03

β 7403 (CDB 403E)
β 5403 (CDB 403EM)



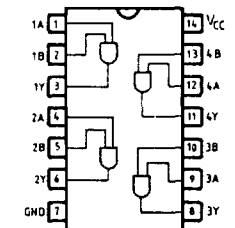
PACKAGE TO-116

QUAD 2-INPUT AND GATES WITH OPEN-COLLECTOR

Function : $Y = A \cdot B$

β 74LS09

β 7409 (CDB 409E)
β 5409 (CDB 409EM)



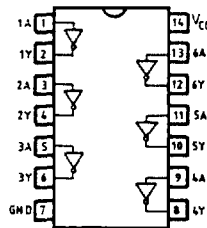
PACKAGE TO-116

HEX INVERTERS

Function : $Y = \overline{A}$

β 74LS04

β 7404 (CDB 404E)
β 5404 (CDB 404EM)



PACKAGE TO-116

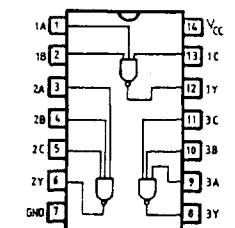
TRIPLE 3-INPUT NAND GATES

Function : $Y = \overline{A \cdot B \cdot C}$

β 74LS10

β 7410 (CDB 410E)
β 5410 (CDB 410EM)

β 74H10 (CDB 410HE)
β 54H10 (CDB 410HEM)



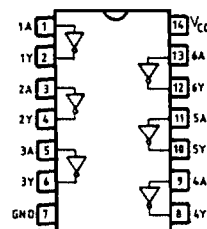
PACKAGE TO-116

HEX INVERTERS WITH OPEN-COLLECTOR

Function : $Y = \overline{A}$

β 74LS05

β 7405 (CDB 405E)
β 5405 (CDB 405EM)



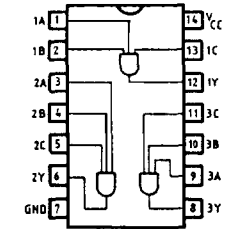
PACKAGE TO-116

TRIPLE 3-INPUT AND GATES

Function : $Y = A \cdot B \cdot C$

β 74LS11

β 74H11 (CDB 411HE)
β 54H11 (CDB 411HEM)

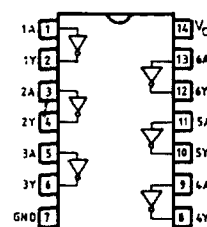


PACKAGE TO-116

HEX INVERTER BUFFERS WITH 30V OPEN COLLECTOR

Function : $Y = \overline{A}$

β 7406 (CDB 406E)
β 5406 (CDB 406EM)

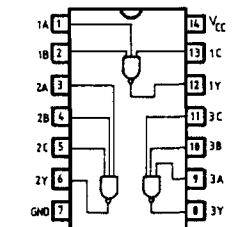


PACKAGE TO-116

TRIPLE 3-INPUT NAND GATES WITH OPEN-COLLECTOR

Function : $Y = \overline{A \cdot B \cdot C}$

β 74LS12



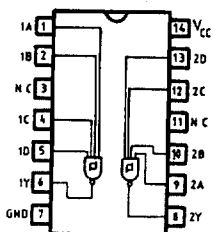
PACKAGE TO-116

DUAL 4-INPUT NAND SCHMITT-TRIGGERS

Function : $Y = \overline{A.B.C.D}$

β 74LS13

β 7413 (CDB 413E)
β 5413 (CDB 413EM)

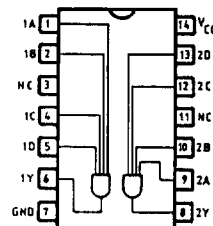


PACKAGE TO-116

DUAL 4-INPUT AND GATES

Function : $Y = A.B.C.D$

β 74LS21

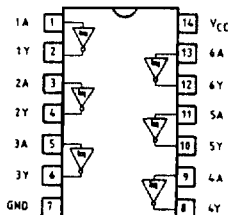


PACKAGE TO-116

HEX SCHMITT-TRIGGER INVERTERS

Function : $Y = \overline{A}$

β 74LS14

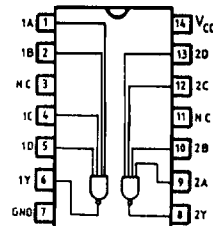


PACKAGE TO-116

DUAL 4-INPUT NAND GATES WITH OPEN-COLLECTOR

Function : $Y = \overline{A.B.C.D}$

β 74LS22

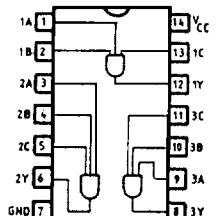


PACKAGE TO-116

TRIPLE 3-INPUT AND GATES WITH OPEN-COLLECTOR

Function : $Y = A . B . C$

β 74LS15

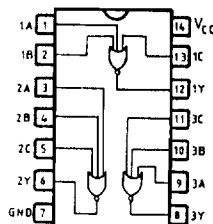


PACKAGE TO-116

TRIPLE 3-INPUT NOR GATES

Function : $Y = \overline{A + B + C}$

β 74LS27

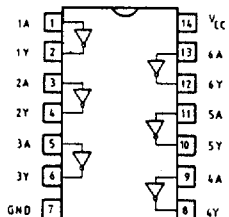


PACKAGE TO-116

HEX INVERTER BUFFERS WITH 15V OPEN-COLLECTOR

Function : $Y = A$

β 7416 (CDB 416E)
β 5416 (CDB 416EM)

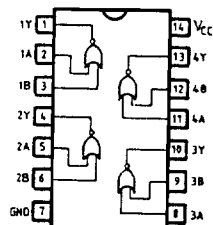


PACKAGE TO-116

QUAD 2-INPUT NOR BUFFERS

Function : $Y = \overline{A + B}$

β 74LS28

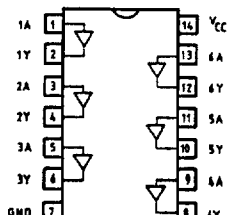


PACKAGE TO-116

HEX BUFFERS WITH 15V OPEN-COLLECTOR

Function : $Y = A$

β 7417 (CDB 417E)
β 5417 (CDB 417EM)



PACKAGE TO-116

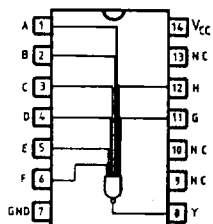
8-INPUT NAND GATES

Function: $Y = \overline{A.B.C.D.E.F.G.H}$

β 74LS30

β 7430 (CDB 430E)
β 5430 (CDB 430EM)

β 74H30 (CDB 430HE)
β 54H30 (CDB 430HEM)



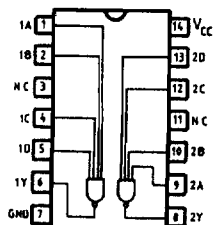
PACKAGE TO-116

DUAL 4-INPUT NAND GATES

Function : $Y = \overline{A.B.C.D}$

β 74LS20

β 7420 (CDB 420E)
β 5420 (CDB 420EM)



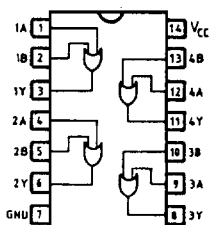
PACKAGE TO-116

QUAD 2-INPUT OR GATES

Function : $Y = A + B$

β 74LS32

β 7432 (CDB 432E)
β 5432 (CDB 432EM)



PACKAGE TO-116

DIGITAL INTEGRATED CIRCUITS

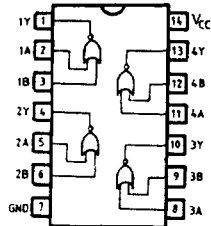
T.T.L. SERIES



QUAD 2-INPUT NOR BUFFERS WITH OPEN-COLLECTOR

Function : $Y = \overline{A + B}$

β 74LS33



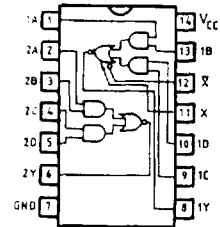
PACKAGE TO-116

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES, ONE EXPANDABLE

Function : $Y = \overline{A \cdot B + C \cdot D + X}$

β 7450 (CDB 450E)
β 5450 (CDB 450EM)

X inputs are compatible with the outputs of β 7460/β 5460.



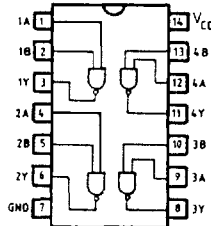
PACKAGE TO-116

QUAD 2-INPUT NAND BUFFERS

Function : $Y = \overline{A \cdot B}$

β 74LS37

β 7437 (CDB 437E)
β 5437 (CDB 437EM)



PACKAGE TO-116

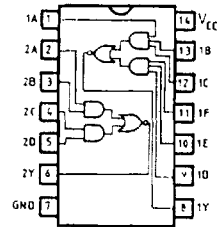
DUAL 2-WIDE, 3-INPUT AND 2-INPUT AND-OR-INVERT GATES

Functions :

$1Y = \overline{1A \cdot 1B \cdot 1C + 1D \cdot 1E \cdot 1F}$

$2Y = \overline{2A \cdot 2B + 2C \cdot 2D}$

β 74LS51



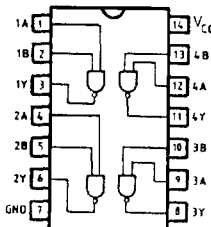
PACKAGE TO-116

QUAD 2-INPUT NAND BUFFERS WITH OPEN-COLLECTOR

Function : $Y = \overline{A \cdot B}$

β 74LS38

β 7438 (CDB 438E)
β 5438 (CDB 438EM)



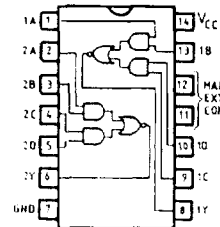
PACKAGE TO-116

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

Function : $Y = \overline{A \cdot B + C \cdot D}$

β 7451 (CDB 451E)
β 5451 (CDB 451EM)

β 74H51 (CDB 451HE)
β 54H51 (CDB 451HEM)



PACKAGE TO-116

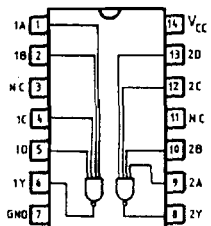
QUAD 2-INPUT NAND BUFFERS

Function : $Y = \overline{A \cdot B}$

β 74LS40

β 7440 (CDB 440E)
β 5440 (CDB 440EM)

β 74H40 (CDB 440HE)
β 54H40 (CDB 440HEM)



PACKAGE TO-116

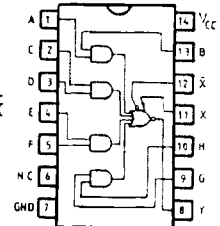
EXPANDABLE 4-WIDE AND-OR-INVERT GATES

Function :

$Y = \overline{A \cdot B + C \cdot D + E \cdot F + G \cdot H + X}$

β 7453 (CDB 453E)
β 5453 (CDB 453EM)

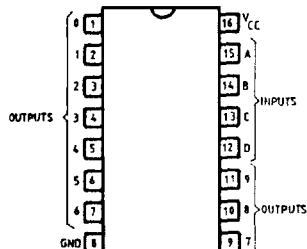
X inputs are compatible with the outputs of β 7460/β 5460.



PACKAGE TO-116

4-TO-10 LINE DECODER (BCD-TO-DECIMAL)

β 7442 (CDB 442E)
β 5442 (CDB 442EM)



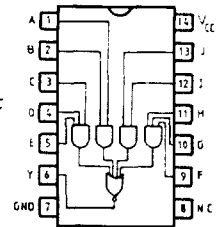
PACKAGE MP-117

4-WIDE 2- & 3-INPUT AND-OR-INVERT GATE

Function :

$Y = \overline{A \cdot B + C \cdot D \cdot E + F \cdot G \cdot H + I \cdot J}$

β 74LS54



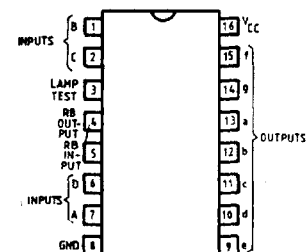
PACKAGE TO-116

BCD-TO-7-SEGMENT DECODERS = WITH 30V OPEN-COLLECTOR

β 7446 (CDB 446E)
β 5446 (CDB 446EM)

= WITH 15V OPEN-COLLECTOR

β 7447 (CDB 447E)
β 5447 (CDB 447EM)



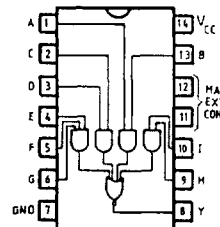
PACKAGE MP-117

4-WIDE 2-INPUT AND-OR-INVERT GATES

Function :

$Y = \overline{A \cdot B + C \cdot D + E \cdot F + G \cdot H}$

β 7454 (CDB 454E)
β 5454 (CDB 454EM)



PACKAGE TO-116

E
E
D
W
B
B
Pr

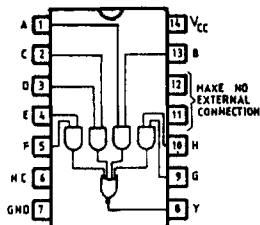


4-WIDE 2- AND 3-INPUT
AND-OR-INVERT GATES

Function :

$$Y = A.B + C.D + E.F.G + H.I$$

β 74H54 (CDB 454HE)
β 54H54 (CDB 454HEM)



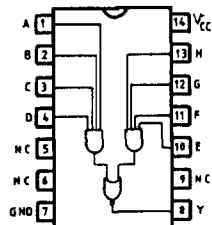
PACKAGE TO-116

2-WIDE 4-INPUT
AND-OR-INVERT GATES

Function :

$$Y = A.B.C.D + E.F.G.H$$

β 74LS55



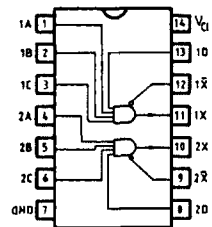
PACKAGE TO-116

DUAL 4-INPUT EXPANDERS

Function : X = A.B.C.D

β 7460 (CDB 460E)
β 5460 (CDB 460EM)

X outputs are compatible with
the inputs of β 7450, β 7453.

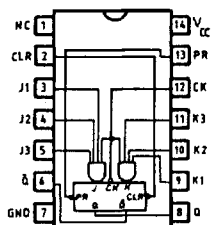


PACKAGE TO-116

AND-GATED J-K MASTER-SLAVE
FLIP-FLOPS, PRESET & CLEAR

β 7472 (CDB 472E)
β 5472 (CDB 472EM)

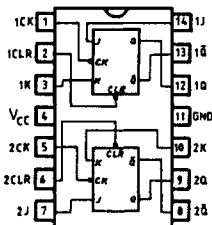
J=J1, J2, J3 ; K=K1, K2, K3



PACKAGE TO-116

DUAL J-K FLIP-FLOPS
WITH CLEAR

β 7473 (CDB 473E)
β 5473 (CDB 473EM)

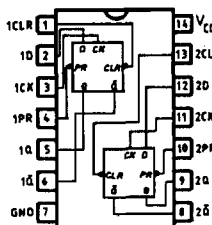


PACKAGE TO-116

DUAL D-TYPE FLIP-FLOPS
WITH PRESET AND CLEAR

β 74LS74

β 7474 (CDB 474E)
β 5474 (CDB 474EM)



PACKAGE TO-116

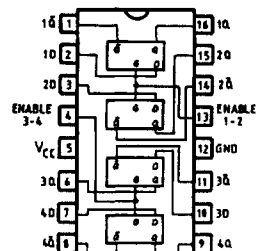
Preset and Clear are active low. PACKAGE TO-116

4-BIT BISTABLE LATCHES

Function table/latch

Inputs		Outputs	
D	G	Q	Q
0	1	0	1
1	1	1	0
x	0	Q	Q

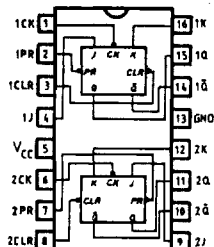
β 7475 (CDB 475E)
β 5475 (CDB 475EM)



PACKAGE MP-117

DUAL J-K FLIP-FLOPS
WITH PRESET AND CLEAR

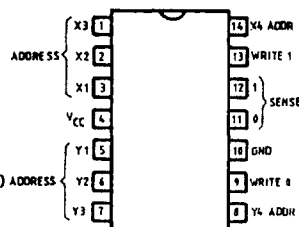
β 7476 (CDB 476E)
β 5476 (CDB 476EM)



PACKAGE MP-117

16-BIT RANDOM-ACCESS
MEMORIES

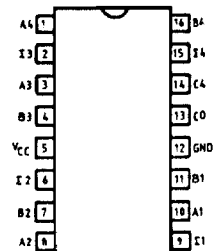
β 7481 (CDB 481E)
β 5481 (CDB 481EM)



PACKAGE TO-116

4-BIT BINARY FULL ADDERS
WITH FAST CARRY

β 7483 (CDB 483E)
β 5483 (CDB 483EM)

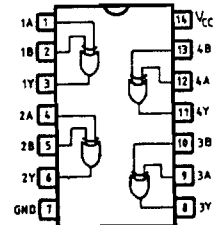


PACKAGE MP-117

QUAD 2-INPUT
EXCLUSIVE-OR GATES

Function : Y = A ⊕ B

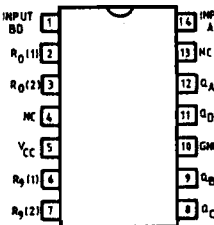
β 74LS86
β 7486 (CDB 486E)
β 5486 (CDB 486EM)



PACKAGE TO-116

DECADE COUNTERS
(DIVIDE-BY-2 AND BY-5)

β 7490 (CDB 490E)
β 5490 (CDB 490EM)



PACKAGE TO-116

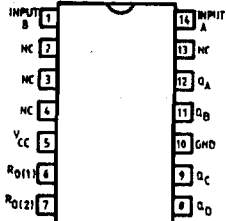
DIGITAL INTEGRATED CIRCUITS

T. T. L. SERIES



DIVIDE-BY-12 COUNTERS
(DIVIDE-BY-2 AND BY-6)

- β 7492 (CDB 492E)
- β 5492 (CDB 492EM)



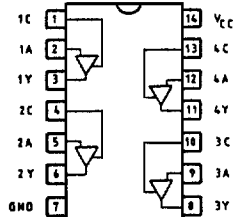
PACKAGE TO-116

QUAD 3-STATE BUFFERS
(DIRECT HI-Z CONTROL)

Function : $Y = A$

- β 74LS126

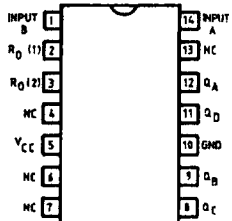
Output is disabled when C is LOW.



PACKAGE TO-116

4-BIT BINARY COUNTERS
(DIVIDE-BY-2 AND BY-8)

- β 7493 (CDB 493E)
- β 5493 (CDB 493EM)

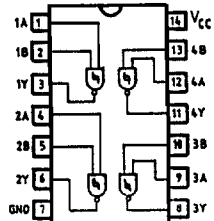


PACKAGE TO-116

QUAD 2-INPUT NAND
SCHMITT-TRIGGERS

Function : $Y = \overline{A \cdot B}$

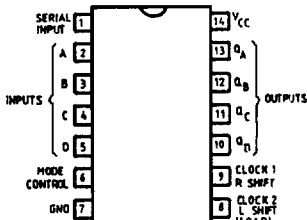
- β 74LS132



PACKAGE TO-116

4-BIT SHIFT REGISTERS
(PARALLEL IN/OUT, OR
SHIFT L/R SERIAL IN)

- β 7495 (CDB 495E)
- β 5495 (CDB 495EM)

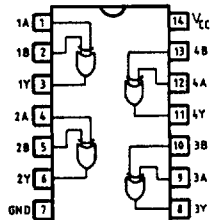


PACKAGE TO-116

QUAD 2-INPUT EX-OR GATES
WITH OPEN COLLECTOR

Function : $Y = A \oplus B$

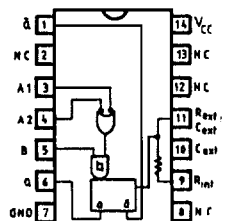
- β 74LS136



PACKAGE TO-116

MONOSTABLE ICs

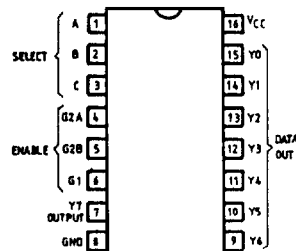
- β 74121 (CDB 4121E)
- β 54121 (CDB 4121EM)



PACKAGE TO-116

3-TO-8 LINE DECODERS /
MULTIPLEXERS

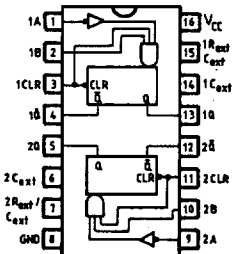
- β 74LS138



PACKAGE MP-117

DUAL RETRIGGERABLE
MONOSTABLES WITH CLEAR

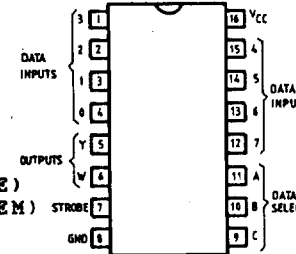
- β 74LS123
- β 74123 (CDB 4123E)
- β 54123 (CDB 4123EM)



PACKAGE MP-117

1-OF-8 DATA SELECTORS /
MULTIPLEXERS

- β 74151 (CDB 4151E)
- β 54151 (CDB 4151EM)



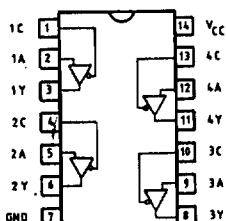
PACKAGE MP-117

QUAD 3-STATE BUFFERS
(INVERTED HI-Z CONTROL)

Function : $Y = \overline{A}$

- β 74LS125

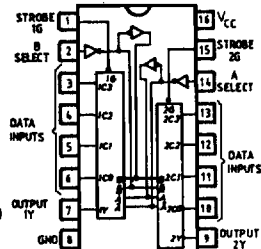
Output is disabled when C is HIGH



PACKAGE TO-116

DUAL 4-TO-1 LINE DATA
SELECTORS / MULTIPLEXERS

- β 74LS153
- β 74153 (CDB 4153E)
- β 54153 (CDB 4153EM)

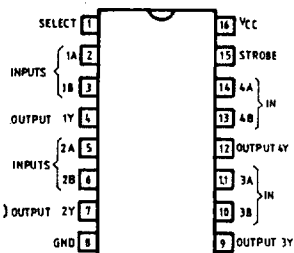


PACKAGE MP-117

QUAD 2-TO-1 DATA MULTIPLEXERS WITH DIRECT DATA OUTPUTS

β 74LS157

β 74157 (CDB 4157E)
β 54157 (CDB 4157EM)



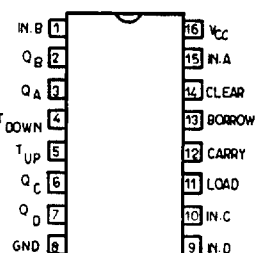
PACKAGE MP-117

SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS WITH CLEAR = DECADE COUNTERS

β 74192 (CDB 4192E)
β 54192 (CDB 4192EM)

= BINARY COUNTERS

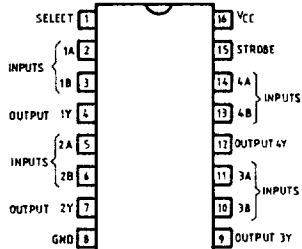
β 74193 (CDB 4193E)
β 54193 (CDB 4193EM)



PACKAGE MP-117

QUAD 2-TO-1 LINE DATA MULTIPLEXERS WITH INVERTED DATA OUTPUTS

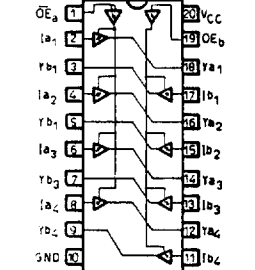
β 74LS158



PACKAGE MP-117

OCTAL NON-INVERTING BUS DRIVER

β 74LS241



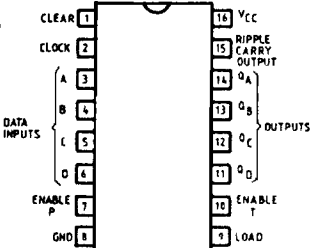
PACKAGE DIL-20

SYNCHRONOUS 4-BIT COUNTERS = WITH DIRECT CLEAR

β 74LS160 (DECADE)
β 74LS161 (BINARY)

= WITH SYNCHRONOUS CLEAR

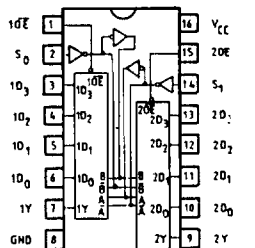
β 74LS162 (DECADE)
β 54LS163 (BINARY)



PACKAGE MP-117

DUAL 4-TO-1 LINE DATA MULTIPLEXERS WITH DIRECT 3-STATE OUTPUTS

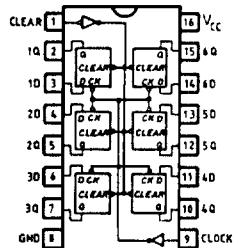
β 74LS253



PACKAGE MP-117

HEX D-TYPE FLIP-FLOPS (SINGLE RAIL OUTPUTS AND DIRECT CLEAR)

β 74LS174



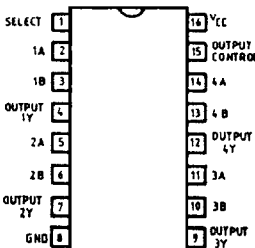
PACKAGE MP-117

QUAD 2-TO-1 DATA MULTIPLEXERS, 3-STATE = DIRECT OUTPUTS

β 74LS257

= INVERTED OUTPUTS

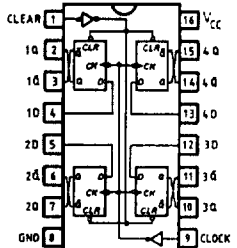
β 74LS258.



PACKAGE MP-117

QUAD D-TYPE FLIP-FLOPS (COMPLEMENTARY OUTPUTS AND DIRECT CLEAR)

β 74LS175

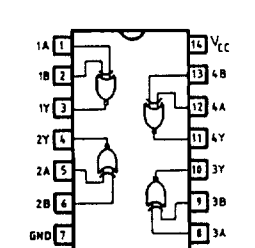


PACKAGE MP-117

QUAD 2-INPUT EX-NOR GATES WITH OPEN-COLLECTOR

Function : $Y = A \oplus B$

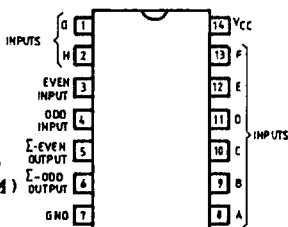
β 74LS266



PACKAGE TO-116

8-BIT ODD/EVEN PARITY GENERATORS / CHECKERS

β 74180 (CDB 4180E)
β 54180 (CDB 4180EM)

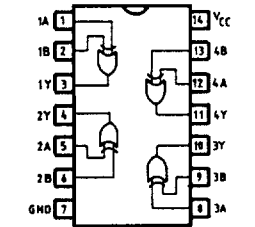


PACKAGE TO-116

QUAD 2-INPUT EXCLUSIVE-OR GATES

Function : $Y = A \oplus B$

β 74LS386



PACKAGE TO-116

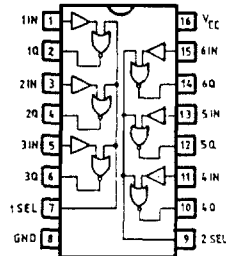
DIGITAL INTEGRATED CIRCUITS

T. T. L. SERIES



HEX UNIFIED
BUS RECEIVERS

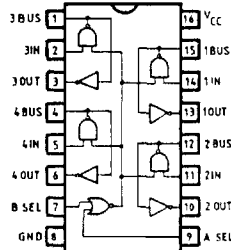
⊗ 7837 (CDB 837E)
⊗ 5837 (CDB 837EM)



PACKAGE MP-117

QUAD UNIFIED
BUS TRANSCEIVERS

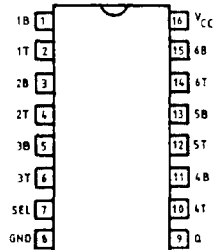
⊗ 7838 (CDB 838E)
⊗ 5838 (CDB 838EM)



PACKAGE MP-117

6-BIT LATCHED COMPARATOR
WITH OPEN COLLECTOR

⊗ 78136 (CDB 8136E)



PACKAGE MP-117