

CMOS DUAL D-TYPE FLIP-FLOP

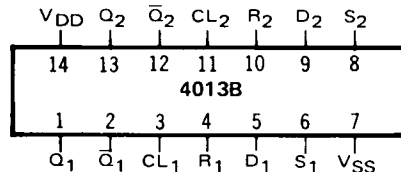
FEATURES

- ◆ Independent Set and Reset Controls
- ◆ Static Operation
- ◆ Logic Edge-Clocked Design
- ◆ 16MHz Toggle Rate @ 10Vdc

DESCRIPTION

The 4013B consists of two identical, independent D-type Flip-Flops. These devices can be used for shift register applications, and, by connecting the \bar{Q} output to the Data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the Clock pulse. Setting or resetting is independent of the Clock and is accomplished by a high level on the Set or Reset line, respectively.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

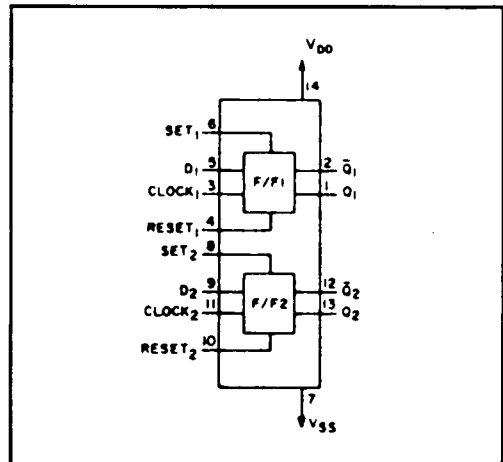
TRUTH TABLE

CL Δ	D	R	S	Q	\bar{Q}
	0	0	0	0	1
	1	0	0	1	0
	x	0	0	Q	\bar{Q}
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

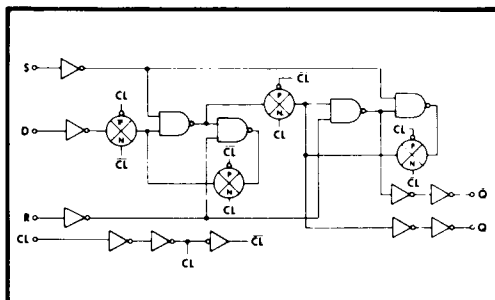
NO CHANGE

Δ = Level Change
x = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	-	1.0	-	0.005	1.0	-	30	μA _{dc}
			-	2.0	-	0.01	2.0	-	60	
			-	4.0	-	0.02	4.0	-	120	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications."

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

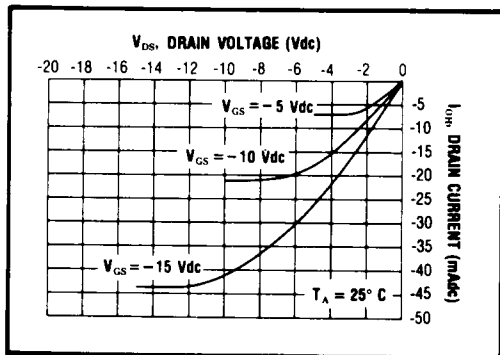
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

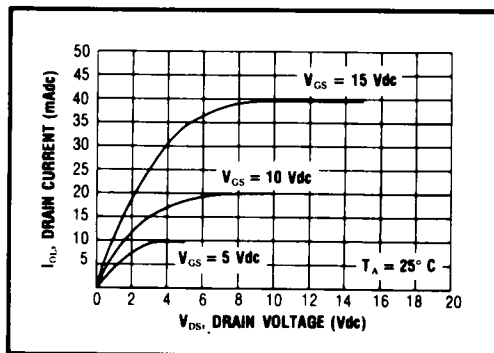
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION					
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	-	125	250
		10	-	65	130
		15	-	45	90
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	-	100	200
		10	-	50	100
		15	-	40	80
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	-	70	140
		10	-	30	60
		15	-	20	40
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	4.0	7.0	-
		10	8.0	16	-
		15	12.5	25	-
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	-	-
		10	10	-	-
		15	5	-	-
MINIMUM SETUP TIME	t _{setup}	5	-	25	50
		10	-	10	20
		15	-	7.5	15
MINIMUM HOLD TIME	t _{hold}	5	-	-25	0
		10	-	-10	0
		15	-	-5	0
SET AND RESET OPERATIONS					
PROPAGATION DELAY TIME S to Q, R to Q̄	t _{PLH}	5	-	125	250
		10	-	65	130
		15	-	45	90
MINIMUM SET AND RESET PULSE WIDTH	PW _S , PW _R	5	-	65	130
		10	-	30	60
		15	-	25	50
SET AND RESET REMOVAL TIME	t _{rem}	5	-	0	25
		10	-	0	10
		15	-	0	5

¹When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics