# 3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

**IDT74ALVCH162543**
***ADVANCE INFORMATION***

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.40mm pitch TVSOP package
- Extended commercial range of – 40°C to +85°C
- $V_{CC}$ = 3.3V ±0.3V, Normal Range
- $V_{CC}$ = 2.7V to 3.6V, Extended Range
- $V_{CC}$ = 2.5V ±0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

**Drive Features for ALVC162543:**

- Balanced Output Drivers: ±12mA
- Low switching noise

## APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

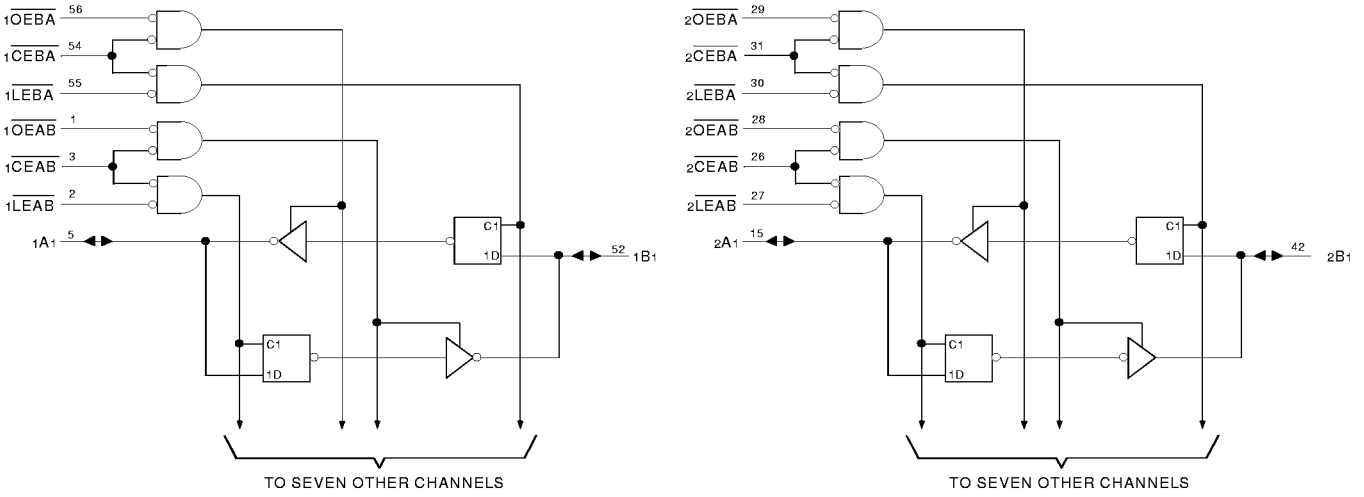
## DESCRIPTION:

This 16-bit registered transceiver is built using advanced dual metal CMOS technology. The ALVCH162543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow. The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

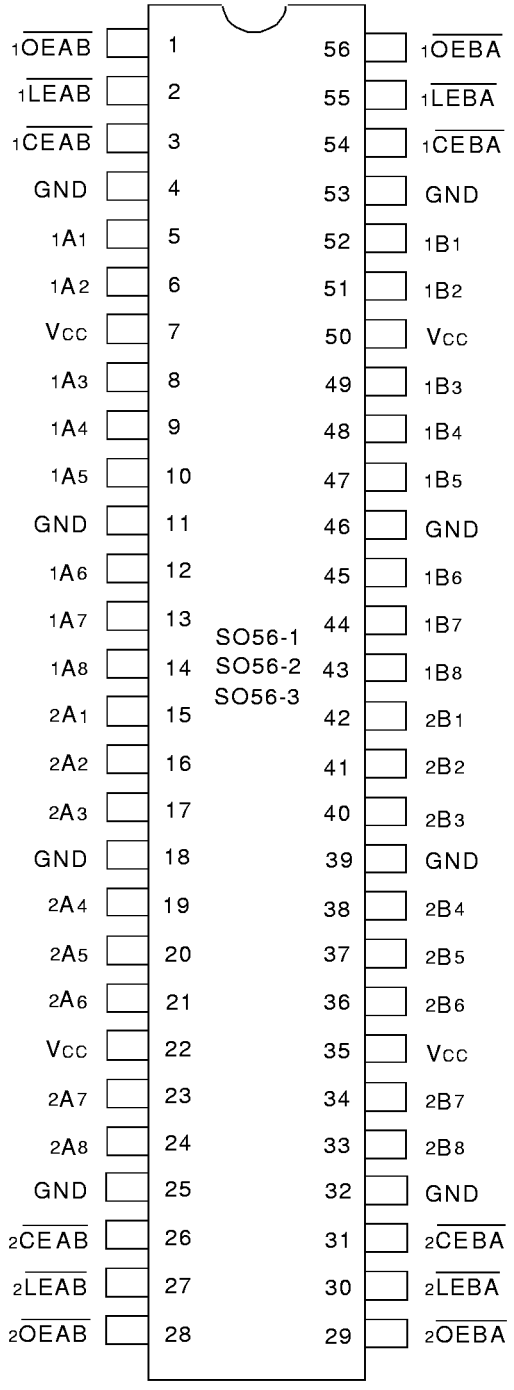
The ALVCH162543 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

The ALVCH162543 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## Functional Block Diagram



## PIN CONFIGURATION




**SSOP/**
**TSSOP/TVSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATING (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | – 0.5 to + 4.6 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | – 0.5 to $V_{CC}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | – 65 to + 150 | °C |
| $I_{OUT}$ | DC Output Current | – 50 to + 50 | mA |
| $I_{IK}$ | Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$ | ± 50 | mA |
| $I_{OK}$ | Continuous Clamp Current, $V_O < 0$ | – 50 | mA |
| $I_{CC}$ $I_{SS}$ | Continuous Current through each $V_{CC}$ or GND | ±100 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{CC}$ terminals.
3. All terminals except $V_{CC}$.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7 | 9 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 7 | 9 | pF |

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**NOTE:**
1. As applicable to the device type.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| $\overline{xOEAB}$ | A-to-B Output Enable Inputs (Active LOW) |
| $\overline{xOEBA}$ | B-to-A Output Enable Inputs (Active LOW) |
| $\overline{xCEAB}$ | A-to-B Enable Inputs (Active LOW) |
| $\overline{xCEBA}$ | B-to-A Enable Inputs (Active LOW) |
| $\overline{xLEAB}$ | A-to-B Latch Enable Inputs (Active LOW) |
| $\overline{xLEBA}$ | B-to-A Latch Enable Inputs (Active LOW) |
| xAx | A-to-B Data Inputs or B-to-A 3-State Outputs (1) |
| xBx | B-to-A Data Inputs or A-to-B 3-State Outputs (1) |

**NOTE:**
1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE(1)

| Inputs | | | | Outputs |
|---|---|---|---|---|
| xCEAB | xLEAB | xOEAB | xAx | xBx |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | $B_0$ |
| L | L | L | L | L |
| L | L | L | H | H |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**

**Operating Condition: TA = – 40°C to +85°C**

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = 3.6V | $V_I$ = $V_{CC}$ | — | — | ± 5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = 3.6V | $V_I$ = GND | — | — | ± 5 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = 3.6V | $V_O$ = $V_{CC}$ | — | — | ± 10 | µA |
| $I_{OZL}$ | (3-State Output pins) | | $V_O$ = GND | — | — | ± 10 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = – 18mA | | — | – 0.7 | – 1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V<br>$V_{IN}$ = GND or $V_{CC}$ | | — | 0.1 | 40 | µA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ – 0.6V, other inputs at $V_{CC}$ or GND | | — | — | 750 | µA |

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**NOTE:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## BUS-HOLD CHARACTERISTICS

| Symbol | Parameter[1] | Test Conditions | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3.0V | $V_I$ = 2.0V | – 75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | – 45 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | 45 | — | — | |
| $I_{BHHO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ± 500 | µA |
| $I_{BHLO}$ | | | | | | | |

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**NOTES:**
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 4mA | 1.9 | — | |
| | | | $I_{OH}$ = – 6mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | $I_{OH}$ = – 4mA | 2.2 | — | |
| | | | $I_{OH}$ = – 8mA | 2 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = – 6mA | 2.4 | — | |
| | | | $I_{OH}$ = – 12mA | 2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 4mA | — | 0.4 | |
| | | | $I_{OL}$ = 6mA | — | 0.55 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 4mA | — | 0.4 | |
| | | | $I_{OL}$ = 8mA | — | 0.6 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 6mA | — | 0.55 | |
| | | | $I_{OL}$ = 12mA | — | 0.8 | |

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**NOTE:**
1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to + 85°C.

## OPERATING CHARACTERISTICS, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Vcc = 2.5V ± 0.2V | Vcc = 3.3V ± 0.3V | Unit |
|---|---|---|---|---|---|
| | | | Typical | Typical | |
| $C_{PD}$ | Power Dissipation Capacitance Outputs enabled | $C_L$ = 0pF, f = 10Mhz | — | — | pF |
| $C_{PD}$ | Power Dissipation Capacitance Outputs disabled | | — | — | pF |

## SWITCHING CHARACTERISTICS(1)

| Symbol | Parameter | Vcc = 2.5V ± 0.2V | | Vcc = 2.7V | | Vcc = 3.3V ± 0.3V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay xAx to xBx or xBx to xAx | 1 | 6.2 | — | 5.5 | 1 | 4.9 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay x$\overline{LEAB}$ to xBx or x$\overline{LEBA}$ to xAx | 1.1 | 7.6 | — | 6.9 | 1.1 | 5.6 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{CEAB}$ to xBx or x$\overline{CEBA}$ to xAx | 1 | 8.2 | — | 7.6 | 1 | 6.2 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{CEAB}$, to xBx or x$\overline{CEBA}$ to xAx | 2 | 6.8 | — | 6.7 | 1.5 | 5.6 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OEAB}$ to xBx or x$\overline{OEBA}$ to xAx | 1 | 7.8 | — | 7 | 1 | 5.9 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OEAB}$ to xBx or x$\overline{OEBA}$ to xAx | 1.6 | 6.4 | — | 5.3 | 1.1 | 5.1 | ns |
| $t_{SU}$ | Setup Time, data before $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$ | 1.2 | — | 1.5 | — | 1.2 | — | ns |
| $t_H$ | Hold Time, data after $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$ | 1.2 | — | 0.8 | — | 1.2 | — | ns |
| $t_W$ | Pulse Duration, $\overline{LE}$ or $\overline{CE}$ LOW | 3.3 | — | 3.3 | — | 3.3 | — | ns |
| $t_{SK(o)}$ | Output Skew(2) | — | — | — | — | — | 500 | ps |

**NOTES:**
1. See test circuits and waveforms. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS:

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$= 3.3V±0.3V | $V_{CC}^{(1)}$= 2.7V | $V_{CC}^{(2)}$= 2.5V±0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |

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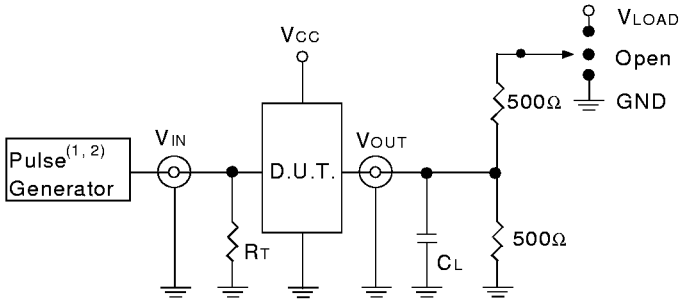
## TEST CIRCUITS FOR ALL OUTPUTS




ALVC Link

**DEFINITIONS:**

$C_L$= Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

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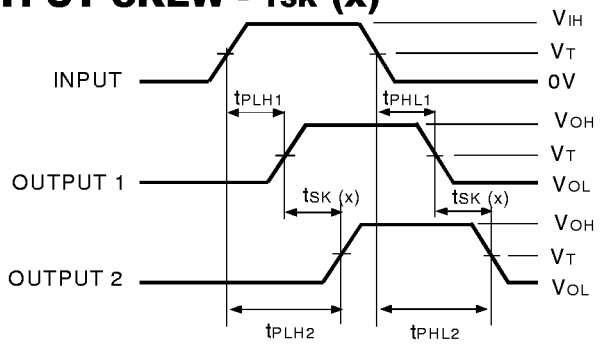
## OUTPUT SKEW - $t_{SK}$ (x)



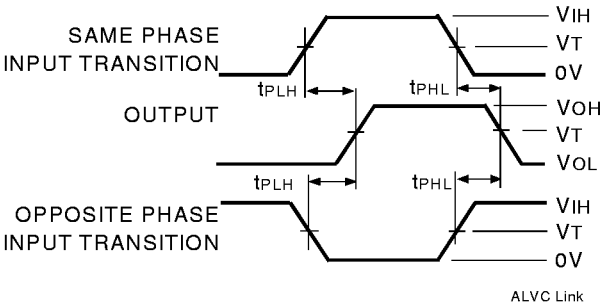

$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

ALVC Link

**NOTES:**

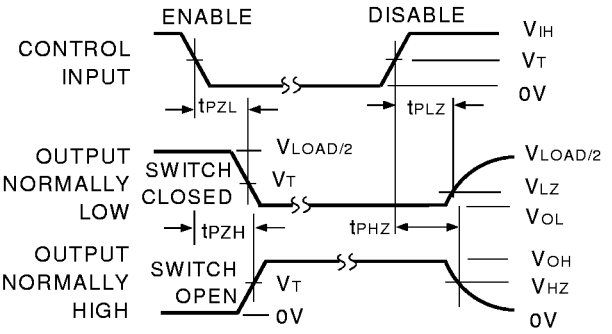
1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.

## PROPAGATION DELAY




ALVC Link

## ENABLE AND DISABLE TIMES

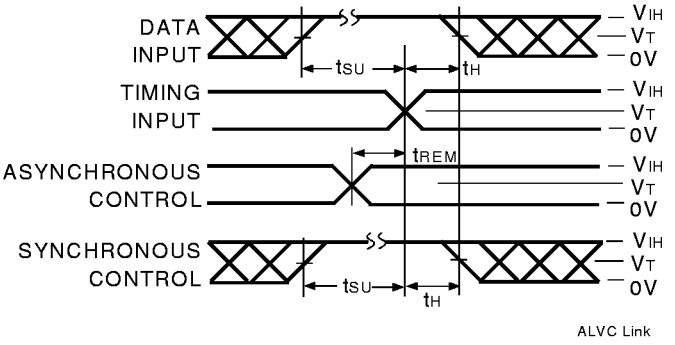



ALVC Link

**NOTE:**

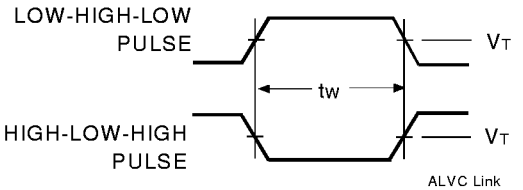
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

## SET-UP, HOLD, AND RELEASE TIMES



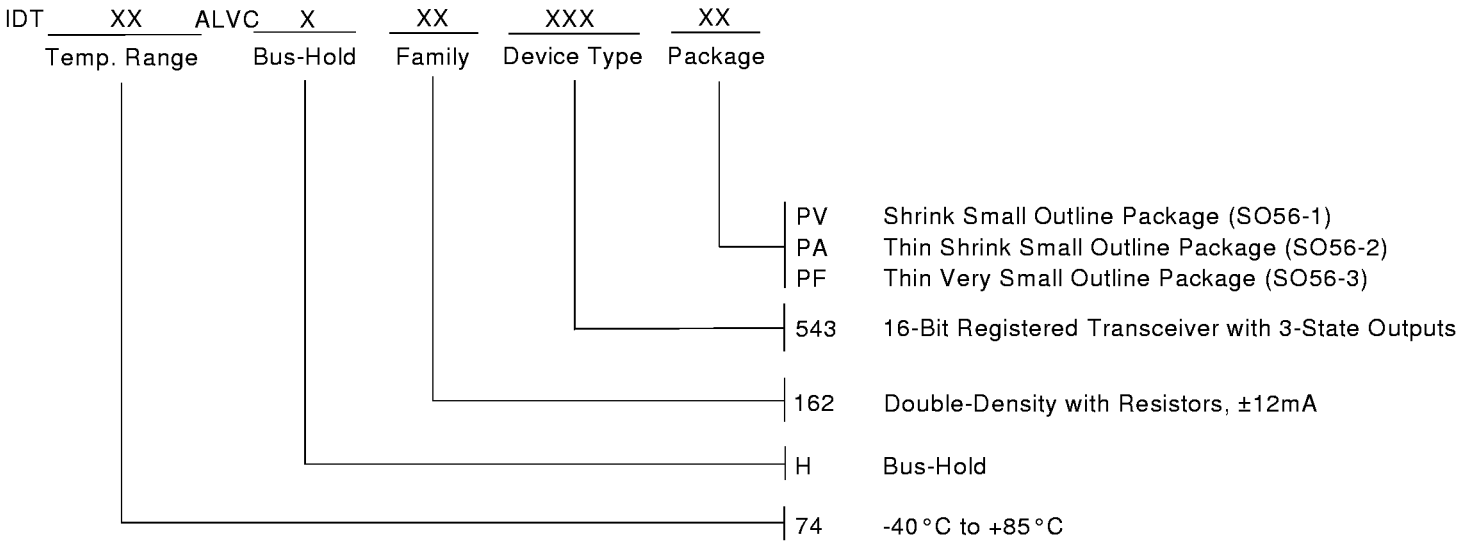

ALVC Link

## PULSE WIDTH




ALVC Link

# ORDERING INFORMATION




***CORPORATE HEADQUARTERS***
2975 Stender Way
Santa Clara, CA 95054

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fax: 408-492-8674
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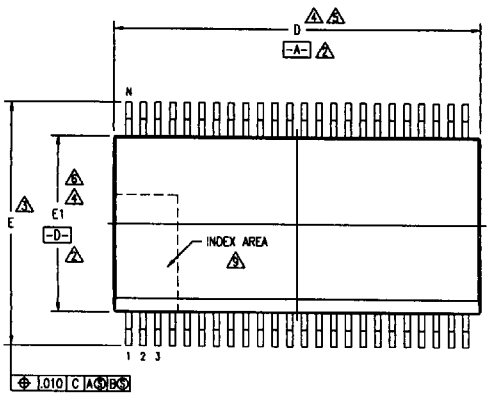
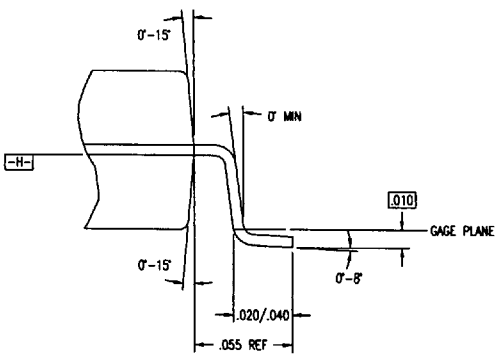
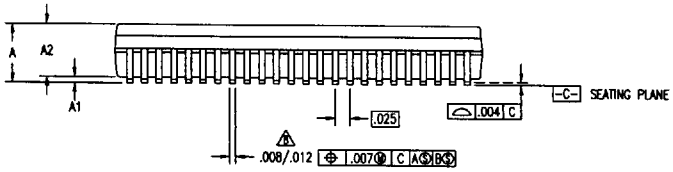
## SSOP

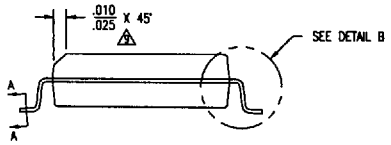
| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 17893 | 00 | INITIAL RELEASE | 07/15/90 | A. FUNCELL |
| 22377 | 01 | REMOVE CHAMFER FROM PACKAGE | 04/15/92 | T. VU |
| 27492 | 02 | REDRAW TO JEDEC FORMAT | 02/01/95 | |

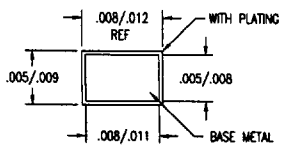



DETAIL B




SECTION A-A

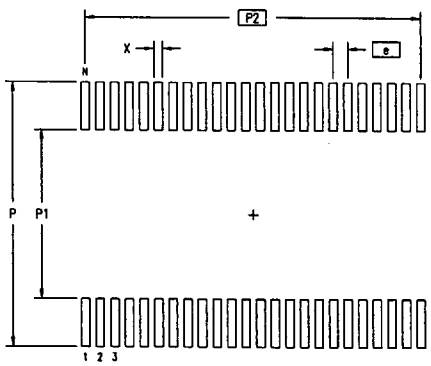
| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
|---|---|---|---|
| DECIMAL XX± XXX± XXXX± | ANGULAR ± | | |
| APPROVALS | DATE | TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH | |
| DRAWN AA | 08/15/90 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4029 REV 02 |
| | | DO NOT SCALE DRAWING | |

## SSOP (Continued)

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 17893 | 00 | INITIAL RELEASE | 07/15/90 | A. FUNCELL |
| 22377 | 01 | REMOVE CHAMFER FROM PACKAGE | 04/15/92 | T. VU |
| 27492 | 02 | REDRAW TO JEDEC FORMAT | 02/01/95 | |

| DWG # | | S048-1 | | | DWG # | | S056-1 | | |
|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION AA | | | NOTE | JEDEC VARIATION AB | | | NOTE |
| | MIN | NOM | MAX | | MIN | NOM | MAX | |
| A | .095 | .102 | .110 | | .095 | .102 | .110 | |
| A1 | .008 | .012 | .016 | | .008 | .012 | .016 | |
| A2 | .088 | .090 | .092 | | .088 | .090 | .092 | |
| D | .620 | .625 | .630 | 4,5 | .720 | .725 | .730 | 4,5 |
| E | .395 | .405 | .420 | 3 | .395 | .405 | .420 | 3 |
| E1 | .291 | .295 | .299 | 4,6 | .291 | .295 | .299 | 4,6 |
| N | 48 | | | | 56 | | | |

### LAND PATTERN DIMENSIONS




| | MIN | MAX | MIN | MAX |
|---|---|---|---|---|
| P | .450 | .458 | .450 | .458 |
| P1 | .282 | .290 | .282 | .290 |
| P2 | .575 BSC | | .675 BSC | |
| X | .010 | .018 | .010 | .018 |
| e | .025 BSC | | .025 BSC | |
| N | 48 | | 56 | |

### NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

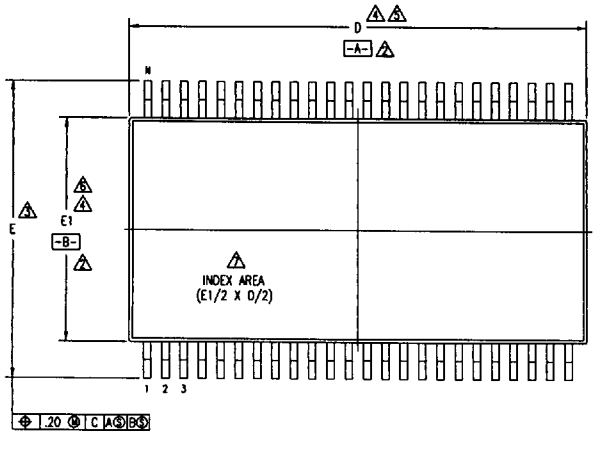
10 ALL DIMENSIONS ARE IN INCHES

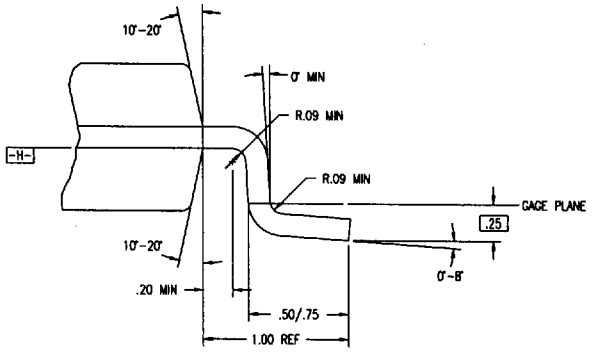
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARATION AA & AB

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. |
|---|---|---|
| DECIMAL XX± XXX± XXXX± | ANGULAR ± | 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 |
| APPROVALS | DATE | TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH |
| DRAWN AA | 05/15/90 | |
| CHECKED | | SIZE C DRAWING No. PSC-4029 REV 02 |
| | | DO NOT SCALE DRAWING |

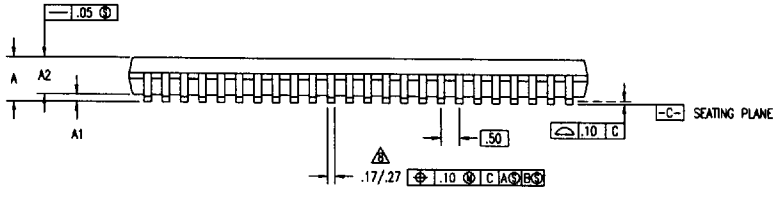
## TSSOP

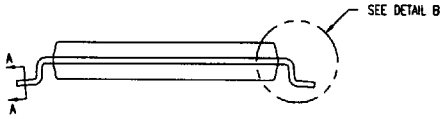
| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 23757 | 00 | INITIAL RELEASE | 02/15/93 | T. VU |
| 26315 | 01 | CHANGE DIMS A1 & A2 | 05/18/94 | DG |
| 25490 | 02 | CHANGE DIM A1 | 07/21/94 | T. VU |
| 27494 | 03 | REDRAW TO JEDEC FORMAT | 03/08/95 | |

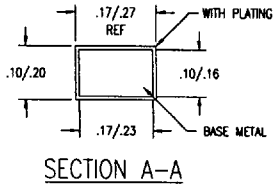



DETAIL B




SECTION A-A

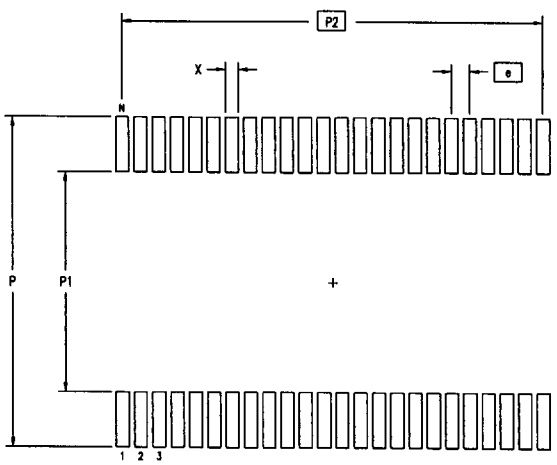
| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
|---|---|---|---|
| DECIMAL | ANGULAR | | |
| XX± | ± | | |
| XXX± | | | |
| XXXX± | | | |
| APPROVALS | DATE | TITLE | PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH |
| DRAWN dd | 01/15/93 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4039 REV 03 |
| | | DO NOT SCALE DRAWING | |

## TSSOP (Continued)

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 23757 | 00 | INITIAL RELEASE | 02/15/93 | T. VU |
| 26315 | 01 | CHANGE DIMS A1 & A2 | 05/18/94 | DG |
| 26490 | 02 | CHANGE DIM A1 | 07/21/94 | T. VU |
| 27494 | 03 | REDRAW TO JEDEC FORMAT | 03/08/95 | |

| DWG # | | | S048-2 | | DWG # | | | S056-2 | |
|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION ED | | | NOTE | JEDEC VARIATION EE | | | NOTE |
| | MIN | NOM | MAX | | MIN | NOM | MAX | |
| A | – | – | 1.10 | | – | – | 1.10 | |
| A1 | .05 | – | .15 | | .05 | – | .15 | |
| A2 | .85 | 1.00 | 1.05 | | .85 | 1.00 | 1.05 | |
| D | 12.40 | 12.50 | 12.60 | 4,5 | 13.90 | 14.00 | 14.10 | 4,5 |
| E | 7.95 | 8.10 | 8.25 | 3 | 7.95 | 8.10 | 8.25 | 3 |
| E1 | 6.00 | 6.10 | 6.20 | 4,6 | 6.00 | 6.10 | 6.20 | 4,6 |
| N | 48 | | | | 56 | | | |

### LAND PATTERN DIMENSIONS



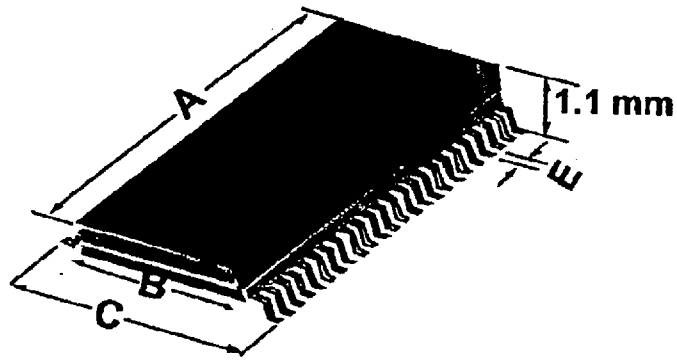

| | MIN | MAX | MIN | MAX |
|---|---|---|---|---|
| P | 8.90 | 9.10 | 8.90 | 9.10 |
| P1 | 5.90 | 6.10 | 5.90 | 6.10 |
| P2 | 11.50 BSC | | 13.50 BSC | |
| X | .30 | .40 | .30 | .40 |
| e | .50 BSC | | .50 BSC | |
| N | 48 | | 56 | |

### NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION ED & EE

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. |
|---|---|---|
| DECIMAL ANGULAR | | 2975 Stender Way, Santa Clara, CA 95054 |
| XX± ± | | PHONE: (408) 727-6116 |
| XXX± | | FAX: (408) 492-8674 TWX: 910-338-2070 |
| XXXX± | | |
| APPROVALS | DATE | TITLE PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH |
| DRAWN AA | 01/13/93 | |
| CHECKED | | SIZE C DRAWING No. PSC-4039 REV 03 |
| | | DO NOT SCALE DRAWING |

# TVSOP
# The Most Compact Double Density Package




| TVSOP Package | Typical Dimensions (in mm) | | | | Area (mm2) |
|---|---|---|---|---|---|
| | A | B | C | E | |
| 48 Pin | 9.80 | 4.40 | 6.40 | 0.40 | 63.00 |
| 56 Pin | 11.30 | 4.40 | 6.40 | 0.40 | 72.30 |
| 80 Pin | 17.00 | 6.10 | 8.10 | 0.40 | 137.80 |
| 100 Pin | 20.80 | 6.10 | 8.10 | 0.40 | 168.50 |

# Double Density Packaging

## 48-Pin


16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²


9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

## 56-Pin


18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²


14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²


11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

| TVSOP | Area ($mm^2$) | %Smaller Than SSOP | %Smaller Than TSSOP |
|---|---|---|---|
| 48 pin | 63.00 | 61.9 | 38.0 |
| 56 pin | 72.30 | 62.2 | 36.0 |