National Semiconductor

PRELIMINARY

74VHC126
Quad Buffer with TRI-STATE® Outputs

General Description

The VHC126 contains four independent non-inverting buffers with TRI-STATE outputs and is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

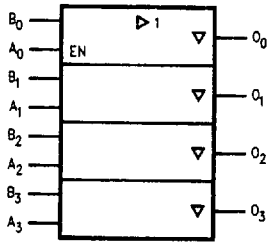
Features

- High speed
- Lower power dissipation: I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range: V_{CC} (opr) = 2V ~ 5.5V
- Low noise: V_{OLP} = 0.8V (max)
- Pin and function compatible with 74HC126
- Logic high output enables

Ordering Code: See Section 5

Logic Symbol

IEEE/IEC



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Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

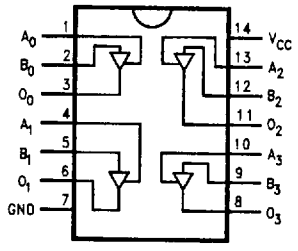
Function Table

Inputs		Output
A_n	B_n	O_n
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

Connection Diagram

Pin Assignment for SSOP and SOIC



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC					Units	Conditions	
			T_A = 25°C			T_A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		V		
		3.0–5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50	V		
		3.0–5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL}; V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Typ	74VHC $T_A = 25°C$ Limits	74VHC $T_A = -40°C$ to $+85°C$ Limits	Units	Conditions	Fig. No.
V_{OLP}**	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8		V	C_L = 50 pF	2-11, 12
V_{OLV}**	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.8		V	C_L = 50 pF	2-11, 12
V_{IHD}**	Minimum High Level Dynamic Input Voltage	5.0		3.5		V	C_L = 50 pF	2-11, 12
V_{ILD}**	Maximum High Level Dynamic Input Voltage	5.0		1.5		V	C_L = 50 pF	2-11, 12

**Parameter guaranteed by design

AC Electrical Characteristics for 'VHC Family Devices: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Min	Typ	Max	74VHC $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions		Fig. No.
t_{PLH}, t_{PHL}	Propagation Delay Time	3.3 ±0.3						ns		C_L = 15 pF	2-5
										C_L = 50 pF	
		5.0 ±0.5						ns		C_L = 15 pF	
										C_L = 50 pF	
t_{PZL}, t_{PZH}	TRI-STATE Output Enable Time	3.3 ±0.3						ns	R_L = 1 kΩ	C_L = 15 pF	2-7, 8
										C_L = 50 pF	
		5.0 ±0.5						ns		C_L = 15 pF	
										C_L = 50 pF	
t_{PLZ}, t_{PHZ}	TRI-STATE Output Disable Time	3.3 ±0.3						ns	R_L = 1 kΩ	C_L = 50 pF	2-7, 8
		5.0 ±0.5								C_L = 50 pF	
t_{OSLH}, t_{OSHL}	Output to Output Skew	3.3 ±0.3			1.5		1.5	ns	(Note 1)	C_L = 50 pF	
		5.0 ±0.5			1.0		1.0			C_L = 50 pF	
C_{IN}	Input Capacitance							pF	V_{CC} = Open		
C_{OUT}	Output Capacitance							pF	V_{CC} = 5.0V		
C_{PD}	Power Dissipation Capacitance							pF	(Note 2)		

Note 1: Parameter guaranteed by design $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$, $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation I_{CC} (OPR) = C_{PD} * V_{CC} * f_{IN} + $I_{CC}/4$ (per bit)