mosaic

512K x 8 SRAM

MSM8512 - 020/025/35

Issue 1.1 :April 2001

Description

The MSM8512 is a 4Mbit monolithic SRAM organised as 512K x 8 with access times from 20ns to 35ns available. The device is available in a 32 pin ceramic surface mount packages. The device has a low power standby version which supports data retention mode and is directly TTL compatible.

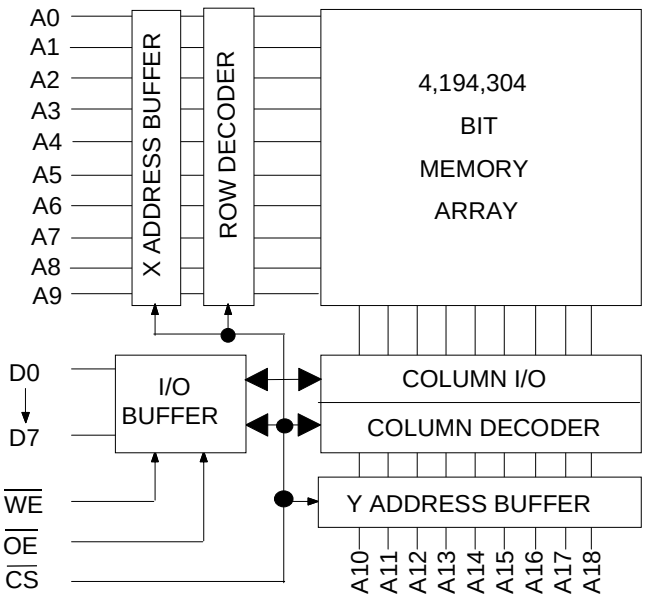
All versions can be screened in accordance with MIL-STD-883C.

524,288 x 8 CMOS Static RAM

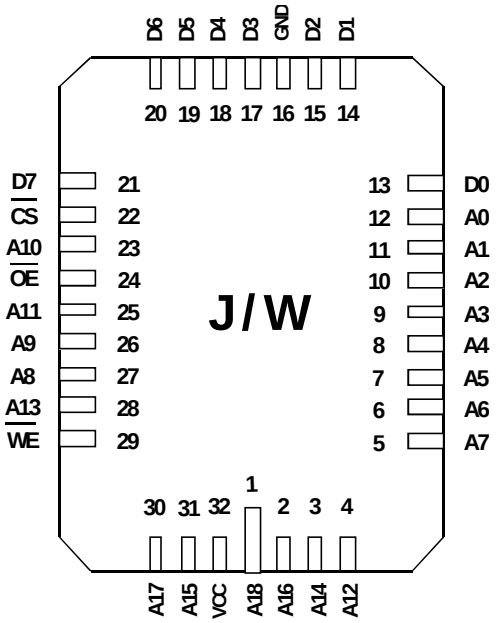
Features

- Fast Access Times of 020/025/35 ns
- High Density Packages.
- Operating Power 950 mW (nom)
- Standby Power 75 mW (nom) -L version
- Completely Static Operation
- Directly TTL compatible
- May be processed in accordance with MIL-STD-883C

Block Diagram



Pin Definition



Package Details

Pin Count	Descripion	Package Type
32	JLCC Package	J

Pin Functions

A0~A18	Address Inputs
D0~7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{cc}	Power (+5V)
GND	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5	to	+7.0	V
Power Dissipation	P_T		1		W
Storage Temperature	T_{STG}	-55	to	+150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	6.0	V	
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	
Operating Temperature	T_A	0	-	70	°C	
	T_{AI}	-40	-	85	°C	(I suffix)
	T_{AM}	-55	-	125	°C	(M, MB suffix)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-2	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V to V_{CC}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	-2	-	2	µA
Operating Supply Current	I_{CC1}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}				
		$I_{I/O}$=0mA, min cycle, duty=100%	-	-	185	mA
Standby Supply Current	I_{SB}	Min Cycle, $\overline{CS}$=V_{IH}	-	-	65	mA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Capacitance (V_{CC}=5V±10%,T_A=25°C)

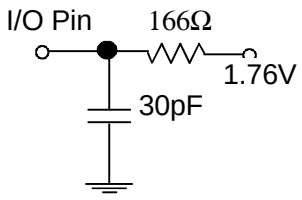
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN} = 0V	-	8	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$= 0V	-	8	pF

Note : This parameter is sampled and not 100% tested.

AC Test Conditions

* Input pulse levels : 0V to 3.0V
* Input rise and fall times : 3ns
* Input and Output timing reference levels: 1.5V
* Output load: See Load Diagram
* V_{cc}=5V±10%

Output Load



AC OPERATING CONDITIONS

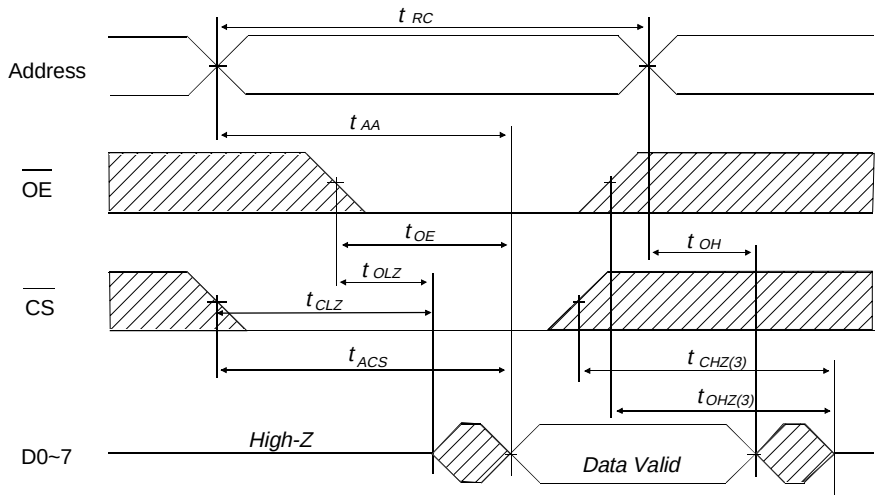
Read Cycle

Parameter	Symbol	20 min	20 max	25 min	25 max	35 min	35 max	Units
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Select Access Time	t_{ACS}	-	20	-	25	-	35	ns
Output Enable to Output Valid	t_{OE}	-	10	-	15	-	15	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z(3)	t_{CHZ}	-	10	0	10	0	10	ns
Output Disable to Output in High Z(3)	t_{OHZ}	0	10	0	10	0	10	ns

Write Cycle

Parameter	Symbol	20 min	20 max	25 min	25 max	35 min	35 max	Unit
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns
Chip Selection to End of Write	t_{CW}	15	-	15	-	15	-	ns
Address Valid to End of Write	t_{AW}	15	-	15	-	15	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	15	-	15	-	15	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	10	0	10	0	10	ns
Data to Write Time Overlap	t_{DW}	10	-	10	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Read Cycle Timing Waveform (1,2)



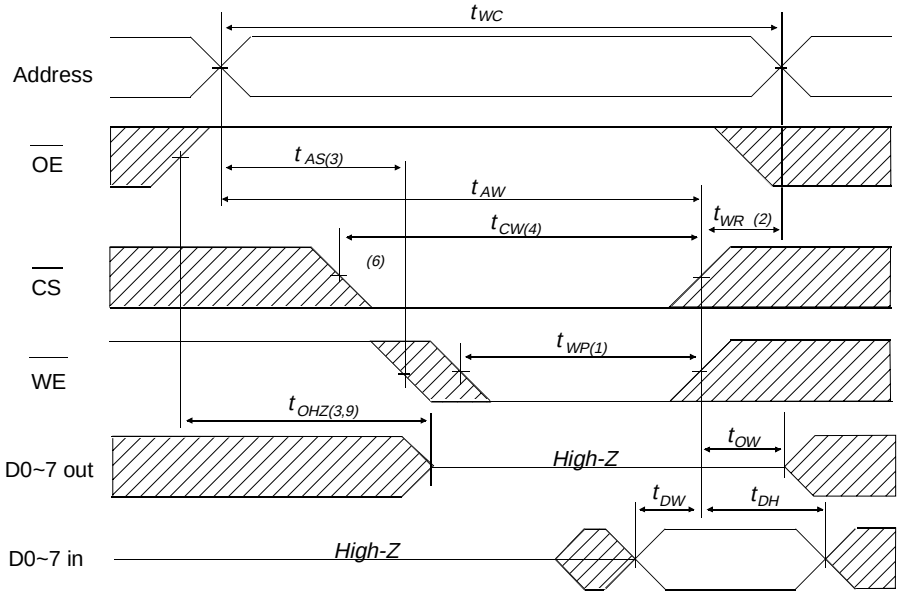
Notes:

(1) During the Read Cycle, $\overline{WE}$ is high.

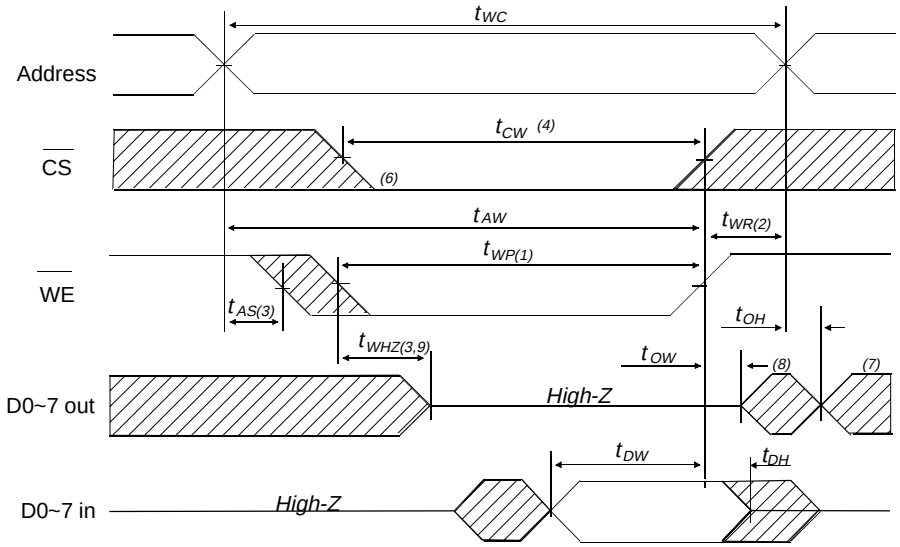
(2) Address valid prior to or coincident with $\overline{CS}$ transition Low.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})

(6) D_{OUT} is in the same phase as written data of this write cycle.

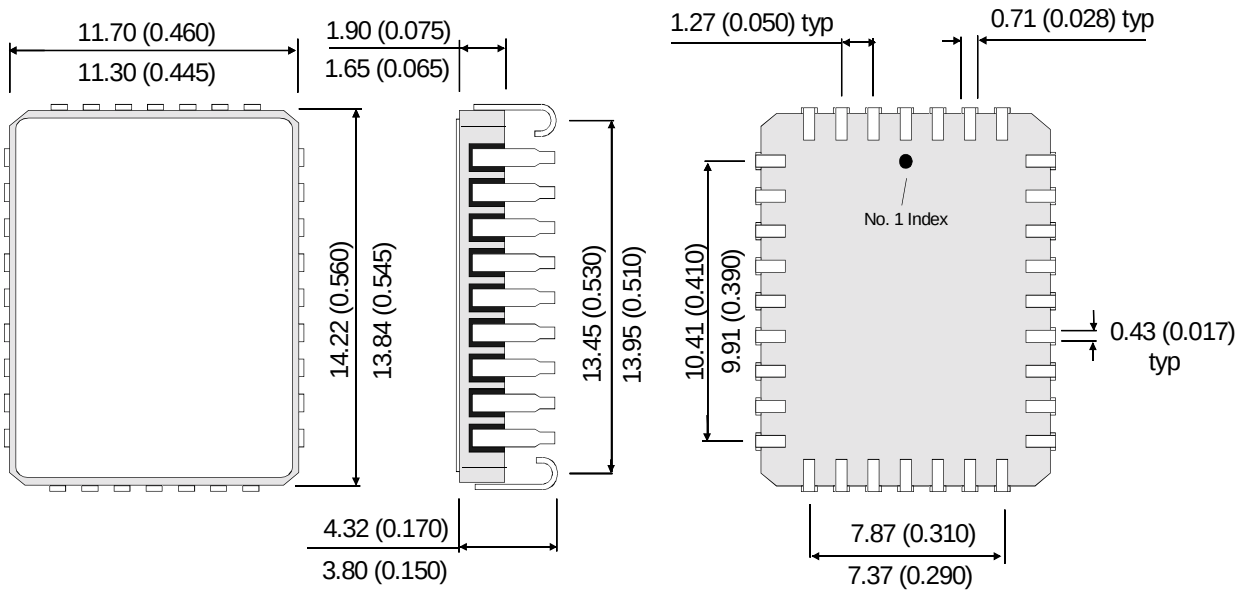
(7) D_{OUT} is the read data of next address.

(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Package Details

32 pin J Leaded Chip Carrier - 'J' Package



All dimensions in mm (inches).

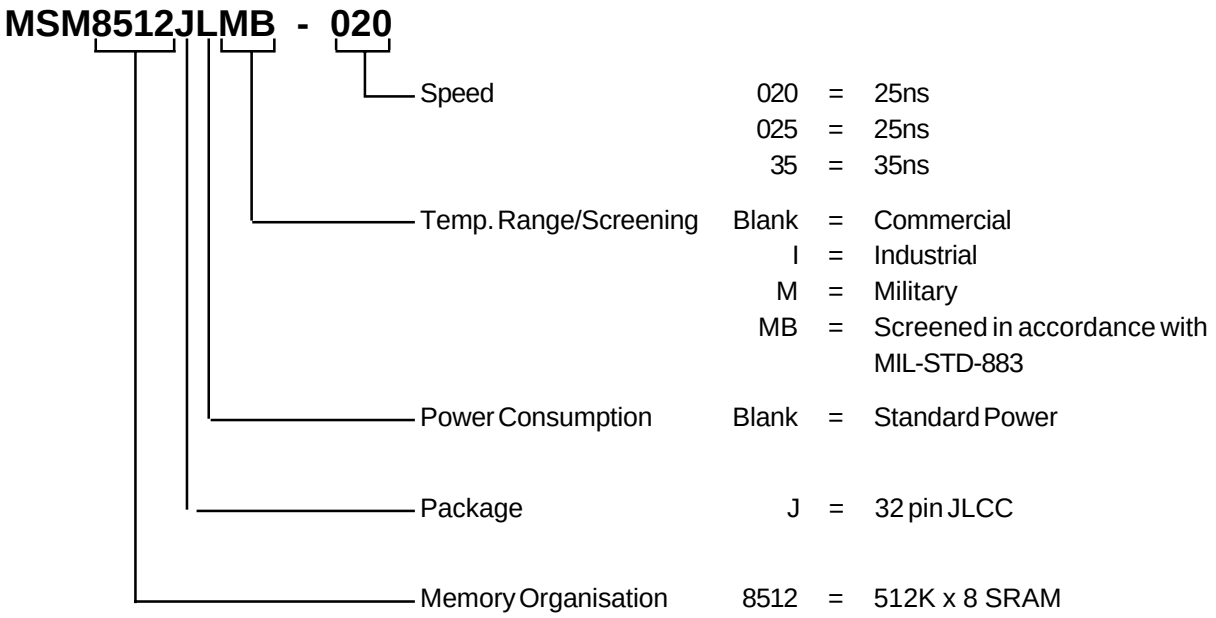
Military Screening Procedure

Screening Flow for high reliability product in accordance with MIL-STD-883 method 5004 is shown below.

MB COMPONENT SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65˚C to +150˚C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25˚C	100%
Burn-in	Method 1015,Condition D,T_A=+125˚C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25˚C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information



Note :
Although this data is believed to be accurate, the information contained herein, is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.
Our products are subject to a constant process of development. Data may be changed at any time without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.