Advance Information
16M CMOS Wide DRAM Family
EDO, 1M x 16, 1K, and 4K Refresh

The family of 16M Dynamic RAMs is fabricated using 0.50µ CMOS high–speed silicon–gate process technology. It includes devices organized as 1,048,576 sixteen–bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The x16 with 4096 cycle refresh (MCM516165BV) require 12 address lines (12 rows, 8 columns), while the x16 device with 1024 cycle refresh (MCM518165BV) require only 10 address lines (10 rows, 10 columns).

These devices are packaged in a standard 400 mil J–lead small outline package (SOJ) and a standard 400 mil thin–small–outline package (TSOP).

- Single 3.3 V ± 10% Power Supply
- Three–State Data Outputs, x16 Configuration
- Extended Data Out (EDO)
- TTL–Compatible Inputs and Outputs
- $\overline{RAS}$–Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 4096 Cycle Refresh:
  MCM516165BV = 64 ms
- 1024 Cycle Refresh:
  MCM518165BV = 16 ms
- Fast Access Time (t_{RAC}):
  MCM51xxxxBV–70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM516165BV–70 = 270 mW (Max)
  MCM518165BV–70 = 522 mW (Max)
- Low Standby Power Dissipation:
  All Devices = 3.6 mW (Max, TTL Levels)
  All Devices = 1.8 mW (Max, CMOS Levels)

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1M x 16

MCM516165BV
EDO
4096 Cycle Refresh

MCM518165BV
EDO
1024 Cycle Refresh

J PACKAGE
400 MIL SOJ

T PACKAGE
400 MIL TSOP II
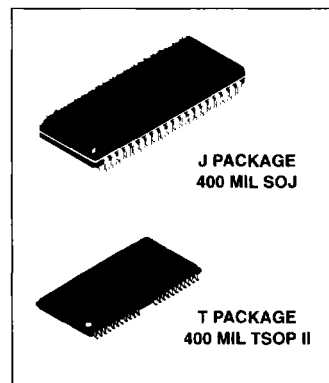
SAMPLE PAGE FOR MCM516165BV
AND MCM518165BV

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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