

SM73302

*SM73302 88 MHz, Precision, Low Noise, 1.8V CMOS Input, Decompensated
Operational Amplifier*



Literature Number: SNOSB93

SM73302

88 MHz, Precision, Low Noise, 1.8V CMOS Input, Decompensated Operational Amplifier

General Description

The SM73302 low noise, CMOS input operational amplifier offers a low input voltage noise density of 5.8 nV/√Hz while consuming only 1.15 mA of quiescent current. The SM73302 is stable at a gain of 10 and has a gain bandwidth (GBW) product of 88 MHz. The SM73302 has a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The SM73302 features a rail-to-rail output stage, and is part of the precision amplifier family and is ideal for a variety of instrumentation applications.

The SM73302 provides optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femtoamperes, and an input common mode voltage range, which includes ground, makes the SM73302 ideal for low power sensor applications where high speeds are needed.

The SM73302 is manufactured using National's advanced VIP50 process. The SM73302 is offered in a 5-Pin SOT-23 package.

Features

(Typical 5V supply, unless otherwise noted)

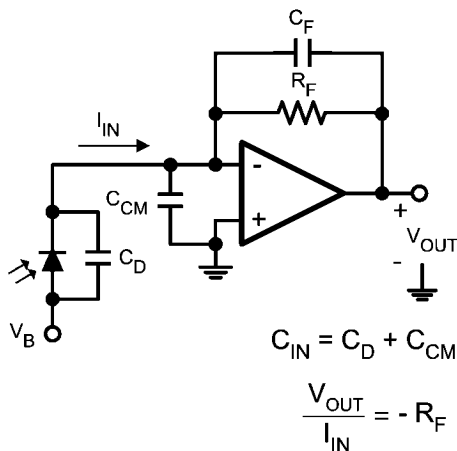
- Renewable Energy Grade
- Input offset voltage ±150 μV (max)
- Input referred voltage noise 5.8 nV/√Hz
- Input bias current 100 fA
- Gain bandwidth product 88 MHz
- Supply voltage range 1.8V to 5.5V
- Supply current 1.15mA
- Rail-to-Rail output swing
 - @ 10 kΩ load 25 mV from rail
 - @ 2 kΩ load 45 mV from rail
- Guaranteed 2.5V and 5.0V performance
- Total harmonic distortion 0.04% @ 1 kHz, 600Ω
- Temperature range -40°C to 125°C

Applications

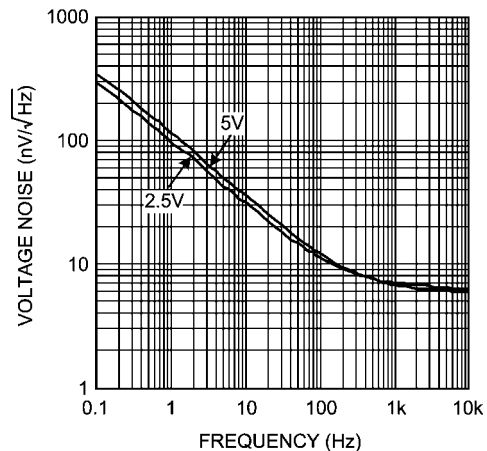
- ADC interface
- Photodiode amplifiers
- Active filters and buffers
- Low noise signal processing
- Medical instrumentation
- Sensor interface applications



Typical Application



30157769
Photodiode Transimpedance Amplifier



30157739
Input Referred Voltage Noise vs. Frequency

Absolute Maximum Ratings *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance *(Note 2)*

Human Body Model	2000V
Machine Model	200V
Charge-Device Model	1000V
V_{IN} Differential	$\pm 0.3V$
Supply Voltage ($V^+ - V^-$)	6.0V
Input/Output Pin Voltage	$V^+ + 0.3V, V^- - 0.3V$
Storage Temperature Range	$-65^\circ C$ to $150^\circ C$
Junction Temperature <i>(Note 3)</i>	$+150^\circ C$

For soldering specifications:

see product folder at www.national.com and
www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings *(Note 1)*

Temperature Range <i>(Note 3)</i>	$-40^\circ C$ to $125^\circ C$
Supply Voltage ($V^+ - V^-$)	$2.0V$ to $5.5V$
$-40^\circ C \leq T_A \leq 125^\circ C$	$2.0V$ to $5.5V$
$0^\circ C \leq T_A \leq 125^\circ C$	$1.8V$ to $5.5V$
Package Thermal Resistance (θ_{JA} <i>(Note 3)</i>)	$180^\circ C/W$
5-Pin SOT-23	

2.5V Electrical Characteristics *(Note 4)*

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ C$, $V^+ = 2.5V$, $V^- = 0V$, $V_{CM} = V^+/2 = V_O$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <i>(Note 6)</i>	Typ <i>(Note 5)</i>	Max <i>(Note 6)</i>	Units
V_{OS}	Input Offset Voltage			± 20	± 180 ± 480	μV
TC V_{OS}	Input Offset Voltage Temperature Drift <i>(Note 7, Note 9)</i>			-1.0	± 4	$\mu V/^\circ C$
I_B	Input Bias Current	$V_{CM} = 1.0V$ <i>(Note 8, Note 9)</i>	$-40^\circ C \leq T_A \leq 85^\circ C$	0.05	1 25	pA
			$-40^\circ C \leq T_A \leq 125^\circ C$	0.05	1 100	
I_{OS}	Input Offset Current	$V_{CM} = 1.0V$ <i>(Note 9)</i>		.006	0.5 50	pA
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 1.4V$	83 80	94		dB
PSRR	Power Supply Rejection Ratio	$2.0V \leq V^+ \leq 5.5V, V_{CM} = 0V$	85 80	100		dB
		$1.8V \leq V^+ \leq 5.5V, V_{CM} = 0V$	85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB	-0.3 -0.3		1.5 1.5	V
A_{VOL}	Open Loop Voltage Gain	$V_{OUT} = 0.15V$ to $2.2V$, $R_L = 2$ k Ω to $V^+/2$	88 82	98		dB
		$V_{OUT} = 0.15V$ to $2.2V$, $R_L = 10$ k Ω to $V^+/2$	92 88	110		
V_{OUT}	Output Voltage Swing High	$R_L = 2$ k Ω to $V^+/2$		25	70 77	mV from either rail
		$R_L = 10$ k Ω to $V^+/2$		20	60 66	
	Output Voltage Swing Low	$R_L = 2$ k Ω to $V^+/2$		30	70 73	
		$R_L = 10$ k Ω to $V^+/2$		15	60 62	
I_{OUT}	Output Current	Sourcing to V^- $V_{IN} = 200$ mV <i>(Note 10)</i>	36 30	47		mA
		Sinking to V^+ $V_{IN} = -200$ mV <i>(Note 10)</i>	7.5 5	15		

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_S	Supply Current			0.95	1.30 1.65	mA
SR	Slew Rate	$A_V = +10$, Rising (10% to 90%)		32		V/ μ s
		$A_V = +10$, Falling (90% to 10%)		24		
GBW	Gain Bandwidth	$A_V = +10$, $R_L = 10\text{ k}\Omega$		88		MHz
e_n	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$		6.2		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise Density	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD+N	Total Harmonic Distortion + Noise	$f = 1\text{ kHz}$, $A_V = 1$, $R_L = 600\Omega$		0.01		%

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2 = V_O$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			± 10	± 150 ± 450	μV
TC V_{OS}	Input Offset Voltage Temperature Drift (Note 7, Note 9)			-1.0	± 4	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{CM} = 2.0\text{V}$ (Note 8, Note 9)	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.1	1 25	pA
			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	0.1	1 100	
I_{OS}	Input Offset Current	$V_{CM} = 2.0\text{V}$ (Note 9)		.01	0.5 50	pA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 3.7\text{V}$	85 80	100		dB
PSRR	Power Supply Rejection Ratio	$2.0\text{V} \leq V^+ \leq 5.5\text{V}$, $V_{CM} = 0\text{V}$	85 80	100		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$, $V_{CM} = 0\text{V}$	85	98		
CMVR	Common Mode Voltage Range	CMRR $\geq 60\text{ dB}$ CMRR $\geq 55\text{ dB}$	-0.3 -0.3		4 4	V
A_{VOL}	Open Loop Voltage Gain	$V_{OUT} = 0.3\text{V to } 4.7\text{V}$, $R_L = 2\text{ k}\Omega$ to $V^+/2$	88 82	107		dB
		$V_{OUT} = 0.3\text{V to } 4.7\text{V}$, $R_L = 10\text{ k}\Omega$ to $V^+/2$	92 88	110		
V_{OUT}	Output Voltage Swing High	$R_L = 2\text{ k}\Omega$ to $V^+/2$		35	70 77	mV from either rail
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		25	60 66	
	Output Voltage Swing Low	$R_L = 2\text{ k}\Omega$ to $V^+/2$		42	70 73	
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		25	60 66	
I_{OUT}	Output Short Circuit Current	Sourcing to V^- $V_{IN} = 200\text{ mV}$ (Note 10)	46 38	60		mA
		Sinking to V^+ $V_{IN} = -200\text{ mV}$ (Note 10)	10.5 6.5	21		
I_S	Supply Current			1.15	1.40 1.75	mA

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	$A_V = +10$, Rising (10% to 90%)		35		V/ μ s
		$A_V = +10$, Falling (90% to 10%)		28		
GBW	Gain Bandwidth	$A_V = +10$, $R_L = 10 \text{ k}\Omega$		88		MHz
e_n	Input Referred Voltage Noise Density	$f = 1 \text{ kHz}$		5.8		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise Density	$f = 1 \text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD+N	Total Harmonic Distortion + Noise	$f = 1 \text{ kHz}$, $A_V = 1$, $R_L = 600\Omega$		0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(\text{MAX})}$, θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{MAX})} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the statistical quality control (SQC) method.

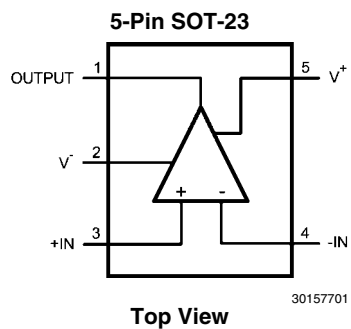
Note 7: Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.

Note 8: Positive current corresponds to current flowing into the device.

Note 9: Parameter is guaranteed by design and/or characterization and is not test in production.

Note 10: The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

Connection Diagram



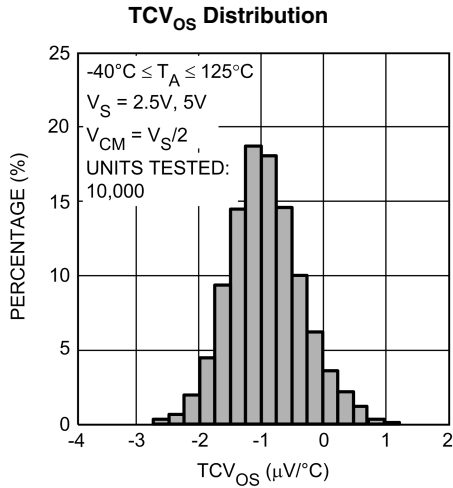
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	SM73302MF	SC3B	1k Units Tape and Reel	MF05A
	SM73302MFE		250 Units Tape and Reel	
	SM73302MFX		3k Units Tape and Reel	

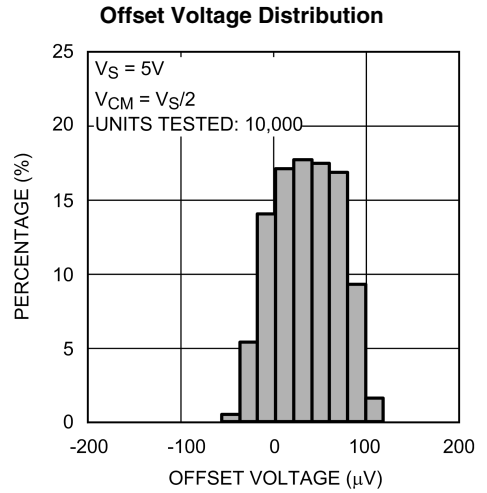
Typical Performance Characteristics

Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V^- = 0$, $V^+ = 5\text{V}$,

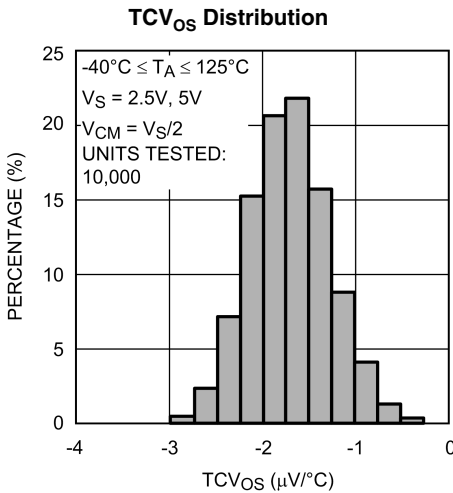
$V_S = V^+ - V^-$, $V_{CM} = V_S/2$.



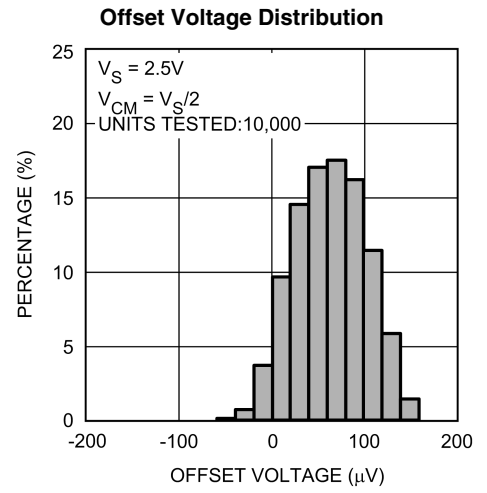
30157790



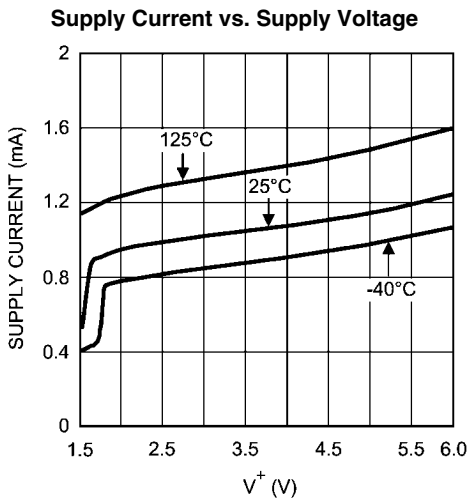
30157791



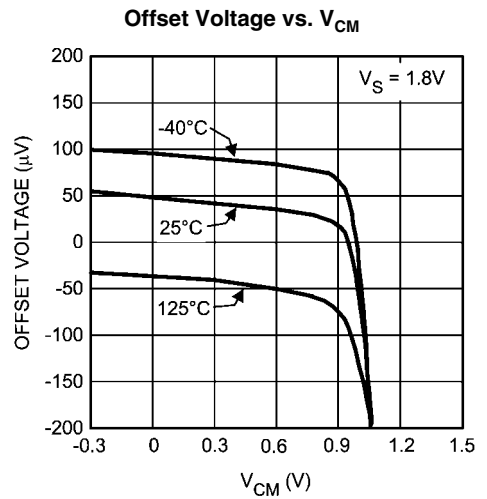
30157792



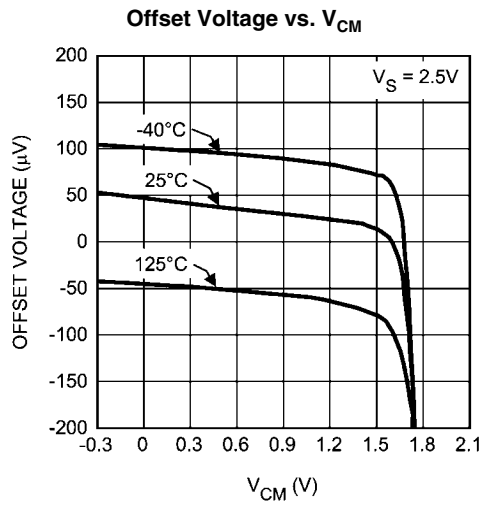
30157793



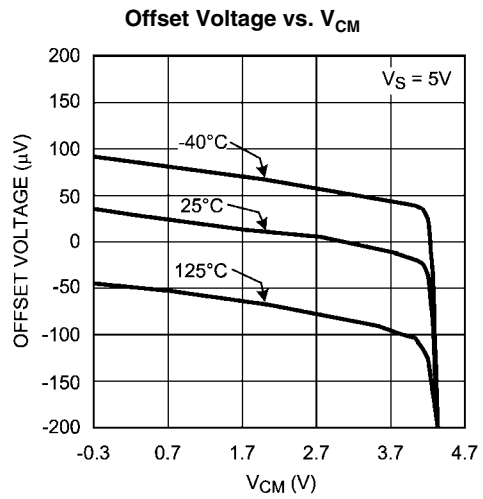
30157705



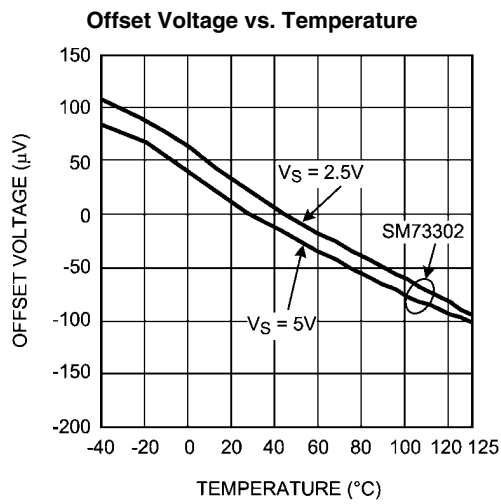
30157709



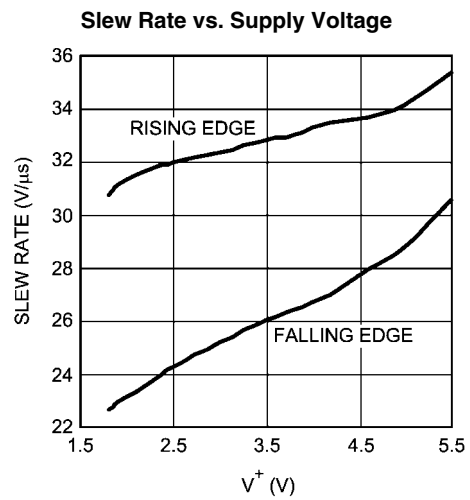
30157751



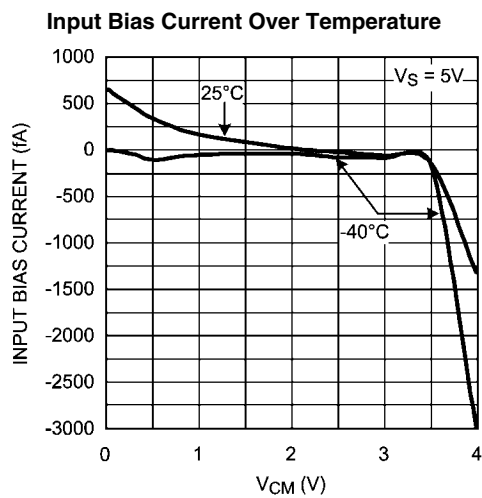
30157711



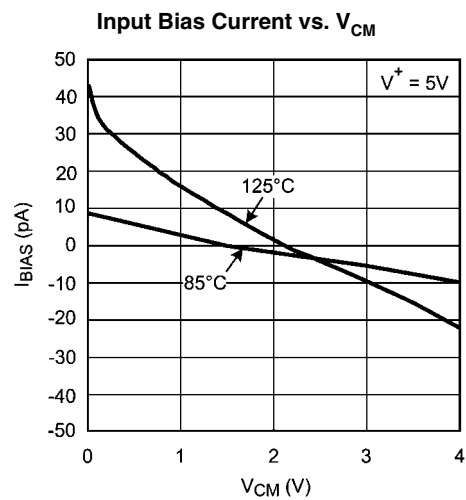
30157712



30157752

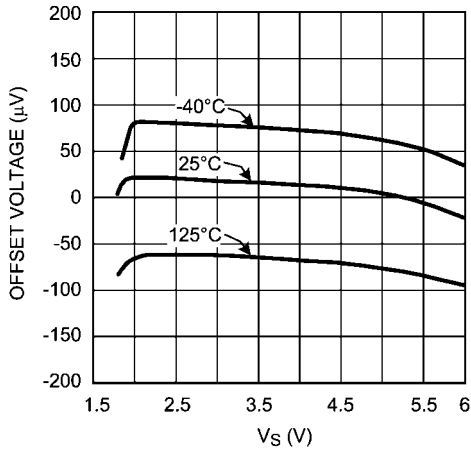


30157762



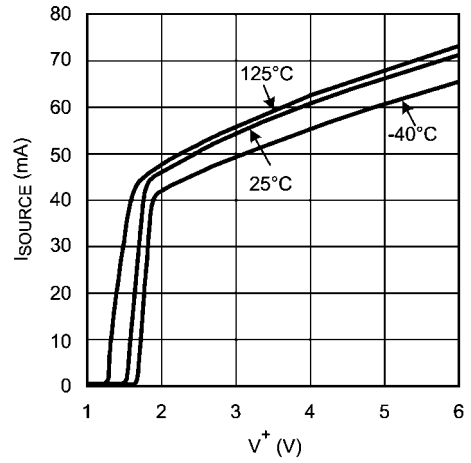
30157787

Offset Voltage vs. Supply Voltage



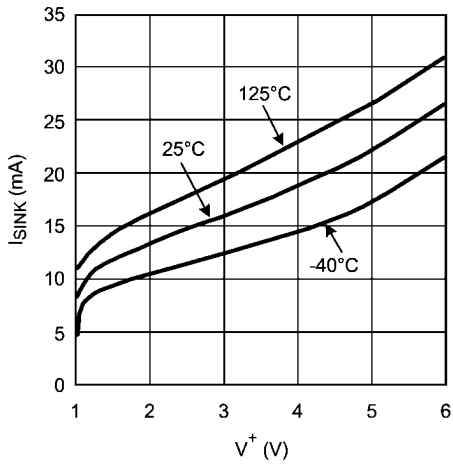
30157727

Sourcing Current vs. Supply Voltage



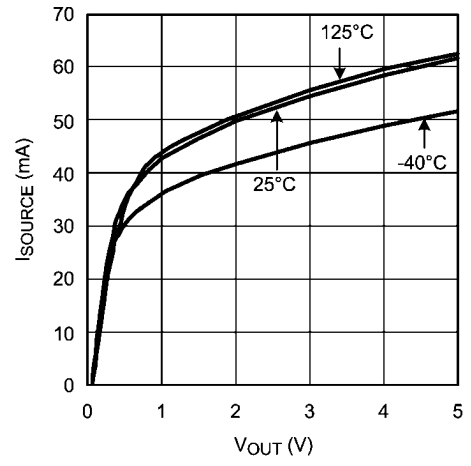
30157720

Sinking Current vs. Supply Voltage



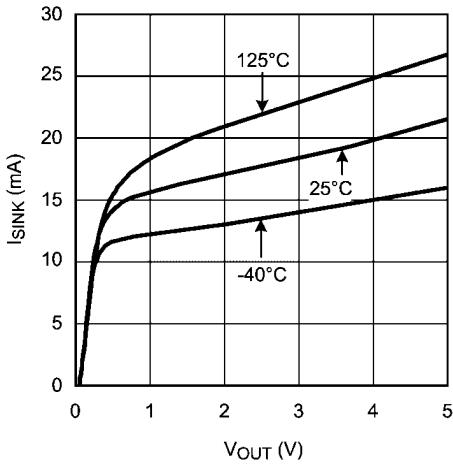
30157719

Sourcing Current vs. Output Voltage



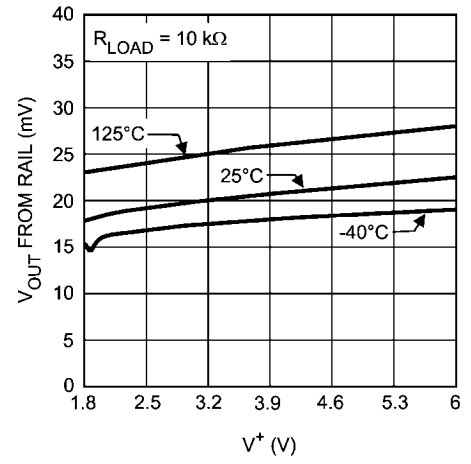
30157750

Sinking Current vs. Output Voltage



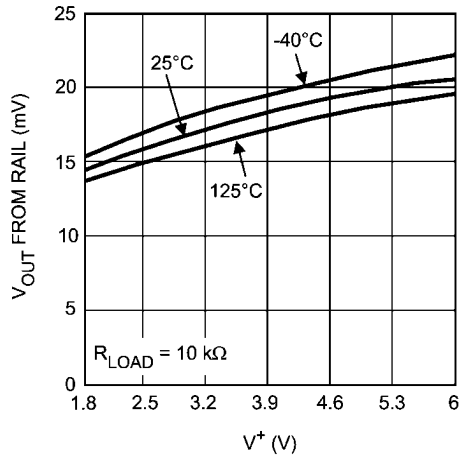
30157754

Positive Output Swing vs. Supply Voltage



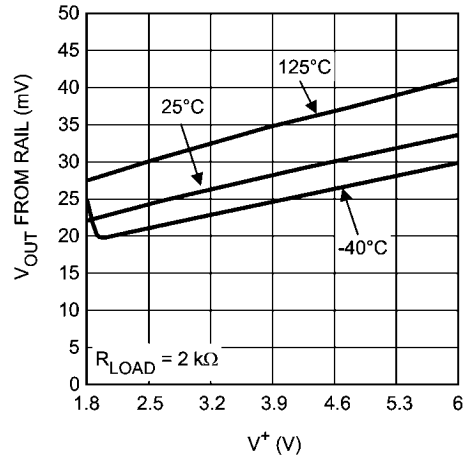
30157717

Negative Output Swing vs. Supply Voltage



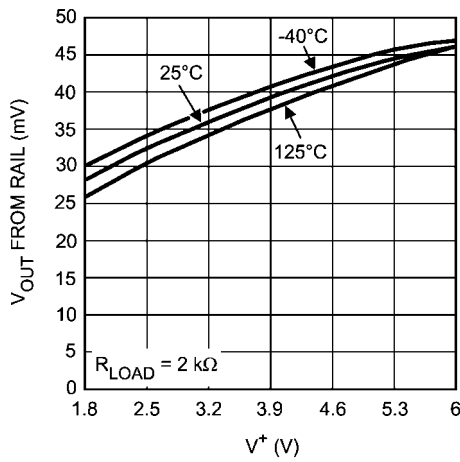
30157715

Positive Output Swing vs. Supply Voltage



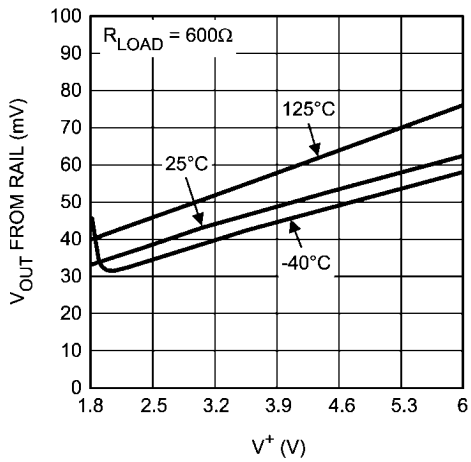
30157716

Negative Output Swing vs. Supply Voltage



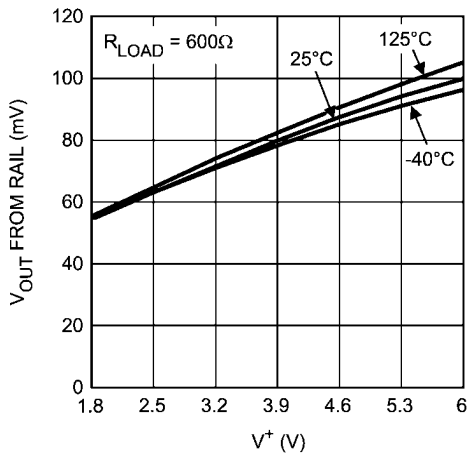
30157714

Positive Output Swing vs. Supply Voltage



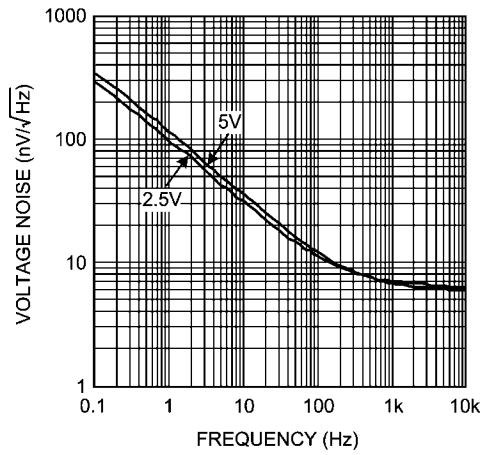
30157718

Negative Output Swing vs. Supply Voltage



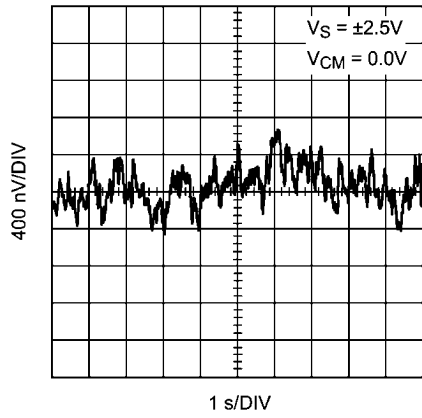
30157713

Input Referred Voltage Noise vs. Frequency



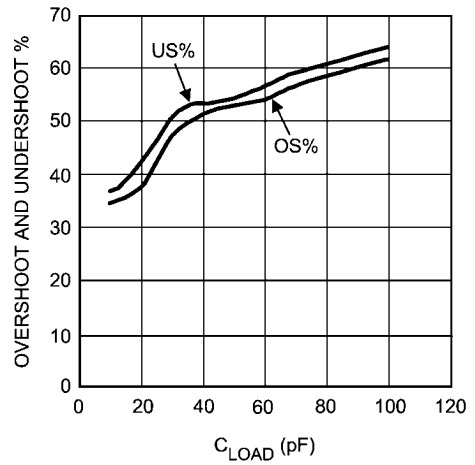
30157739

Time Domain Voltage Noise



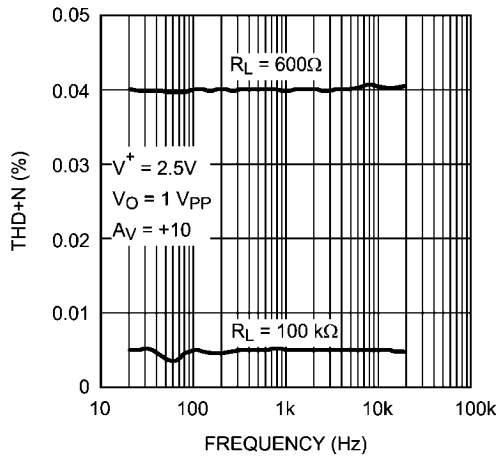
30157781

Overshoot and Undershoot vs. C_{LOAD}



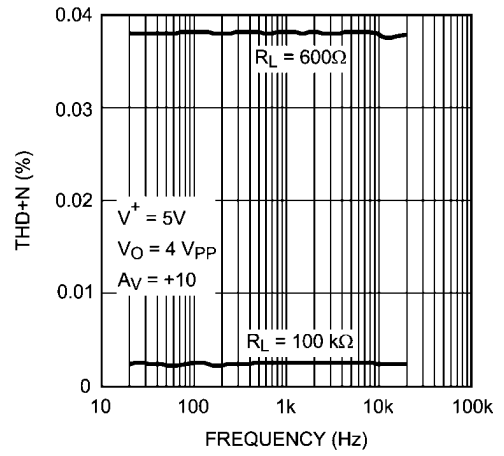
30157730

THD+N vs. Frequency



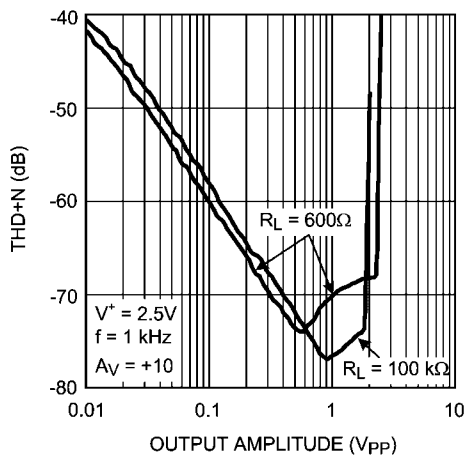
30157726

THD+N vs. Frequency



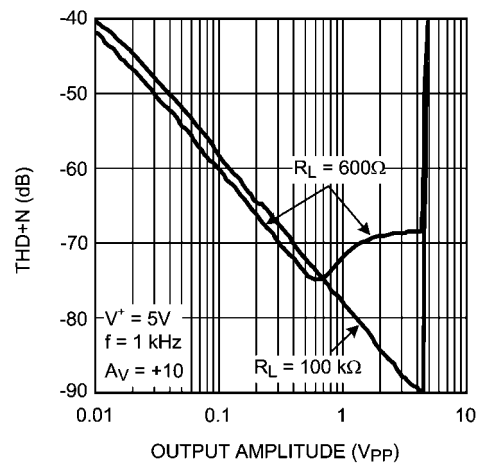
30157704

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})



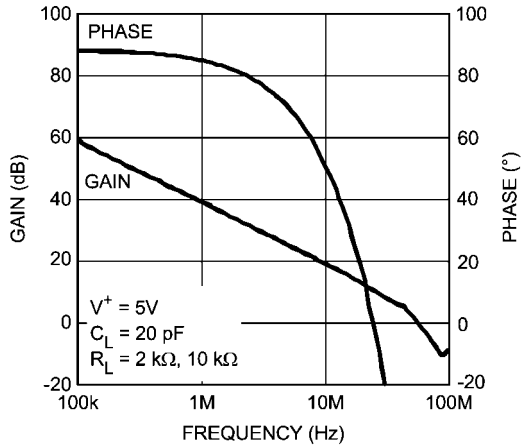
30157774

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})



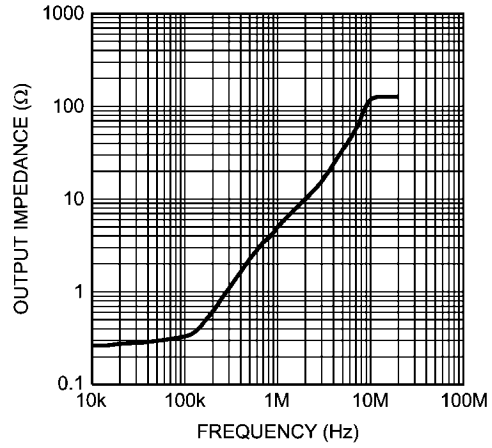
30157775

Open Loop Gain and Phase



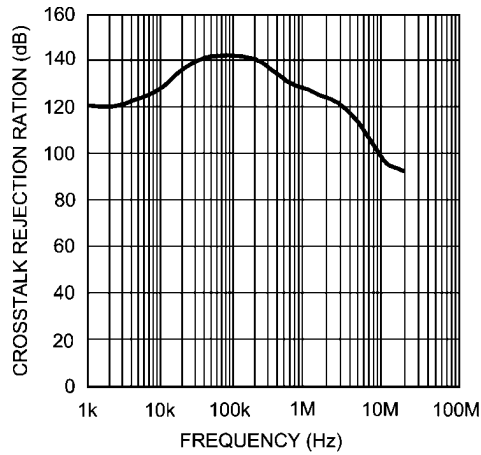
30157706

Closed Loop Output Impedance vs. Frequency



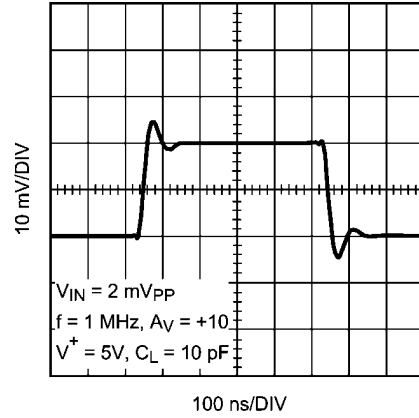
30157732

Crosstalk Rejection



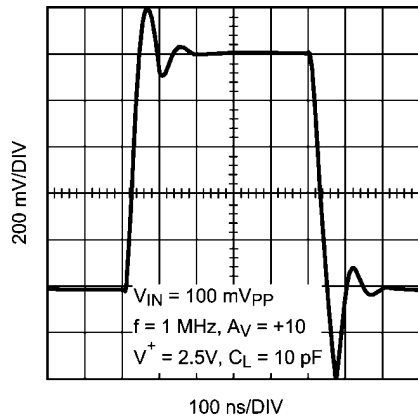
30157780

Small Signal Transient Response, $A_V = +10$



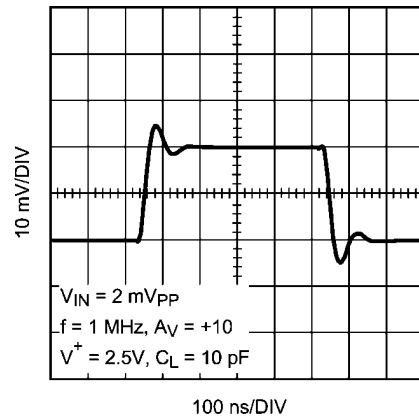
30157753

Large Signal Transient Response, $A_V = +10$



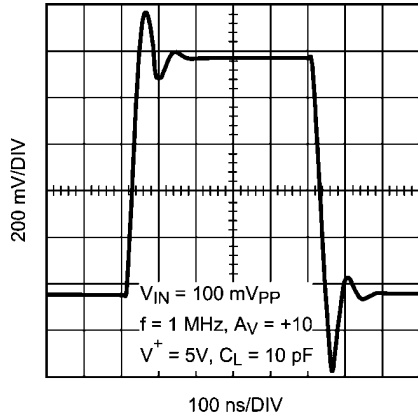
30157755

Small Signal Transient Response, $A_V = +10$



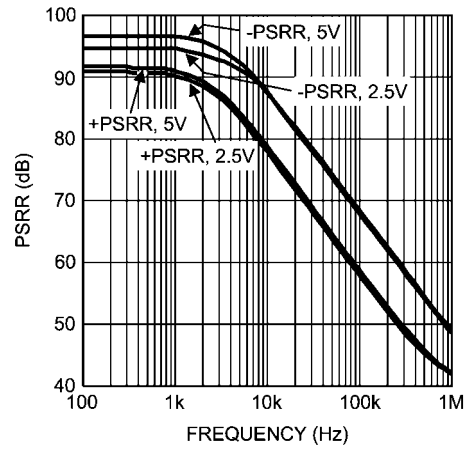
30157757

Large Signal Transient Response, $A_V = +10$



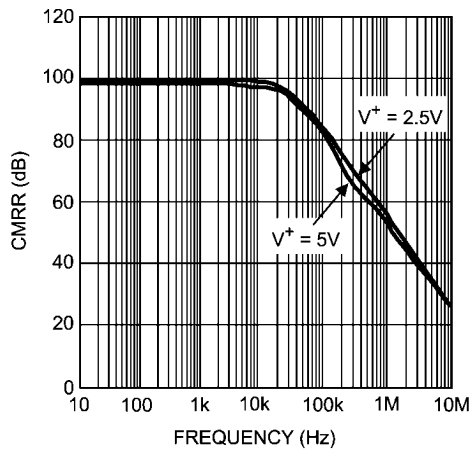
30157763

PSRR vs. Frequency



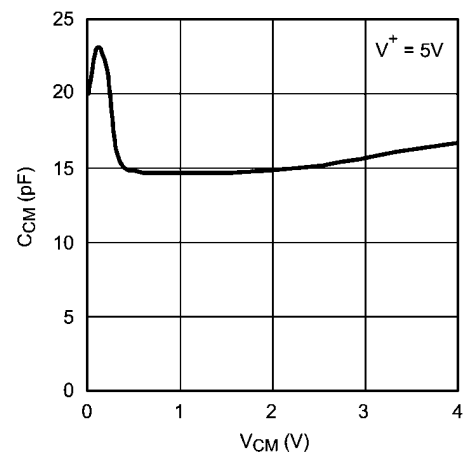
30157770

CMRR vs. Frequency



30157756

Input Common Mode Capacitance vs. V_{CM}



30157776

Application Information

ADVANTAGES OF THE SM73302

Wide Bandwidth at Low Supply Current

The SM73302 is a high performance op amp that provides a GBW of 88 MHz with a gain of 10 while drawing a low supply current of 1.15 mA. This makes it ideal for providing wideband amplification in data acquisition applications.

With the proper external compensation, the SM73302 can be operated at gains of ± 1 and still maintain much faster slew rates than comparable unity gain stable amplifiers. The increase in bandwidth and slew rate is obtained without any additional power consumption over the LMP7715.

Low Input Referred Noise and Low Input Bias Current

The SM73302 has a very low input referred voltage noise density (5.8 nV/ $\sqrt{\text{Hz}}$ at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise (0.01 pA/ $\sqrt{\text{Hz}}$). This is very helpful in maintaining signal integrity, and makes the SM73302 ideal for audio and sensor based applications.

Low Supply Voltage

The SM73302 has performance guaranteed at 2.5V and 5V supply. This part is guaranteed to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from -40°C to 125°C , thus utilizing the entire battery lifetime. The SM73302 is also guaranteed to be operational at 1.8V supply voltage, for temperatures between 0°C and 125°C optimizing their usage in low-voltage applications.

RRO and Ground Sensing

Rail-to-Rail output (RRO) swing provides the maximum possible dynamic range. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the SM73302 to source more than 40 mA of current at 1.8V supply. This also limits the performance of this part as a comparator, and hence the usage of the SM73302 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

Small Size

The small footprint of the SM73302 package saves space on printed circuit boards, and enables the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the op amp make the signal path more susceptible to noise pick up.

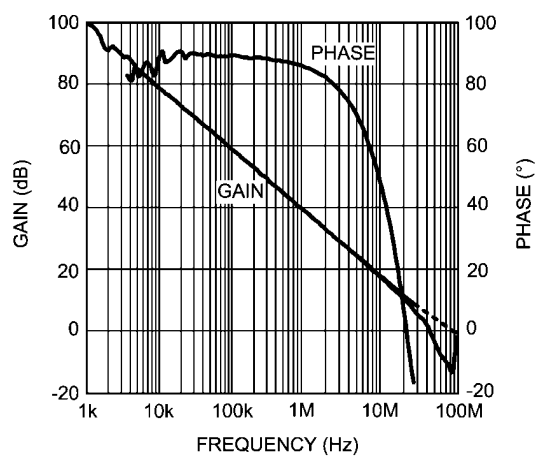
The physically smaller SM73302 allows the op amp to be placed closer to the signal source, thus reducing noise pickup and maintaining signal integrity.

USING THE DECOMPENSATED SM73302

Advantages of Decompensated Op Amp

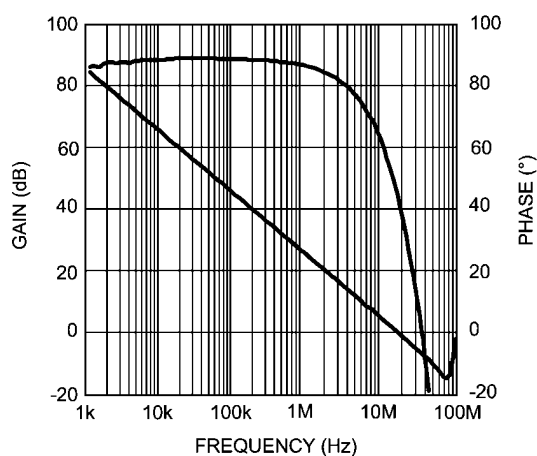
A unity gain stable op amp, which is fully compensated, is designed to operate with good stability down to gains of ± 1 . The large amount of compensation does provide an op amp that is relatively easy to use; however, a decompensated op amp is designed to maximize the bandwidth and slew rate without any additional power consumption. This can be very advantageous.

The SM73302 requires a gain of ± 10 to be stable. However, with an external compensation network (a simple RC network) these parts can be stable with gains of ± 1 and still maintain the higher slew rate. Looking at the Bode plots for the SM73302 and its closest equivalent unity gain stable op amp, the LMP7715, one can clearly see the increased bandwidth of the SM73302. Both plots are taken with a parallel combination of 20 pF and 10 k Ω for the output load.



30157722

FIGURE 1. SM73302 A_{VOL} vs. Frequency



30157723

FIGURE 2. LMP7715 A_{VOL} vs. Frequency

Figure 1 shows the much larger 88 MHz bandwidth of the SM73302 as compared to the 17 MHz bandwidth of the LMP7715 shown in Figure 2. The decompensated SM73302 has five times the bandwidth of the LMP7715.

What is a Decompensated Op Amp?

The differences between the unity gain stable op amp and the decompensated op amp are shown in *Figure 3*. This Bode plot assumes an ideal two pole system. The dominant pole of the decompensated op amp is at a higher frequency, f_1 , as compared to the unity gain stable op amp which is at f_d as shown in *Figure 3*. This is done in order to increase the speed capability of the op amp while maintaining the same power dissipation of the unity gain stable op amp. The SM73302 has a dominant pole at 1.6 kHz. The unity gain stable LMP7715/LMP7716 have their dominant pole at 300 Hz.

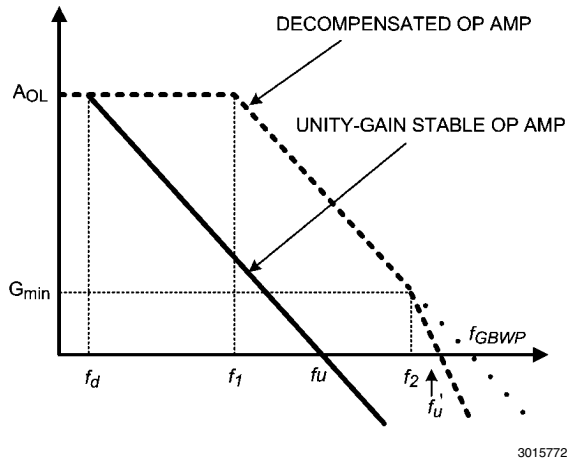


FIGURE 3. Open Loop Gain for Unity Gain Stable Op Amp and Decompensated Op Amp

Having a higher frequency for the dominate pole will result in:

1. The DC open loop gain (A_{VOL}) extending to a higher frequency.
2. A wider closed loop bandwidth.
3. Better slew rate due to reduced compensation capacitance within the op amp.

The second open loop pole (f_2) for the SM73302 occurs at 45 MHz. The unity gain (f_u') occurs after the second pole at 51 MHz. An ideal two pole system would give a phase margin of 45° at the location of the second pole. The SM73302 has parasitic poles close to the second pole, giving a phase margin closer to 0° . Therefore it is necessary to operate the SM73302 at a closed loop gain of 10 or higher, or to add external compensation in order to assure stability.

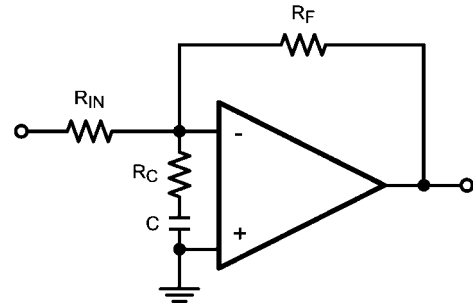
For the LMP7715, the gain bandwidth product occurs at 17 MHz. The curve is constant from f_d to f_u which occurs before the second pole.

For the SM73302 the GBW = 88 MHz and is constant between f_1 and f_2 . The second pole at f_2 occurs before $A_{VOL} = 1$. Therefore f_u' occurs at 51 MHz, well before the GBW frequency of 88 MHz. For decompensated op amps the unity gain frequency and the GBW are no longer equal. G_{min} is the minimum gain for stability and for the SM73302 this is a gain of 18 to 20 dB.

Input Lead-Lag Compensation

The recommended technique which allows the user to compensate the SM73302 for stable operation at any gain is lead-lag compensation. The compensation components added to the circuit allow the user to shape the feedback function to make sure there is sufficient phase margin when the loop gain is as low as 0 dB and still maintain the advantages over the

unity gain op amp. *Figure 4* shows the lead-lag configuration. Only R_C and C are added for the necessary compensation.



30157725

FIGURE 4. SM73302 with Lead-Lag Compensation for Inverting Configuration

To cover how to calculate the compensation network values it is necessary to introduce the term called the feedback factor or F. The feedback factor F is the feedback voltage $V_A - V_B$ across the op amp input terminals relative to the op amp output voltage V_{OUT} .

$$F = \frac{V_A - V_B}{V_{OUT}}$$

From feedback theory the classic form of the feedback equation for op amps is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + AF}$$

A is the open loop gain of the amplifier and AF is the loop gain. Both are highly important in analyzing op amps. Normally $AF \gg 1$ and so the above equation reduces to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{F}$$

Deriving the equations for the lead-lag compensation is beyond the scope of this datasheet. The derivation is based on the feedback equations that have just been covered. The inverse of feedback factor for the circuit in *Figure 4* is:

$$\frac{1}{F} = \left(1 + \frac{R_F}{R_{IN}} \right) \left(\frac{1 + s(R_C + R_{IN} \parallel R_F) C}{1 + sR_C C} \right) \quad (1)$$

where $1/F$'s pole is located at

$$f_p = \frac{1}{2\pi R_C C} \quad (2)$$

$1/F$'s zero is located at

$$f_z = \frac{1}{2\pi(R_C + R_{IN} \parallel R_F) C} \quad (3)$$

$$\frac{1}{F} \Big|_{f=0} = 1 + \frac{R_F}{R_{IN}} \quad (4)$$

The circuit gain for [Figure 4](#) at low frequencies is $-R_F/R_{IN}$, but F , the feedback factor is not equal to the circuit gain. The feedback factor is derived from feedback theory and is the same for both inverting and non-inverting configurations. Yes, the feedback factor at low frequencies is equal to the gain for the non-inverting configuration.

$$\frac{1}{F} \Big|_{f=\infty} = \left(1 + \frac{R_F}{R_{IN}}\right) \left(1 + \frac{R_{IN} \parallel R_F}{R_C}\right) \quad (5)$$

From this formula, we can see that

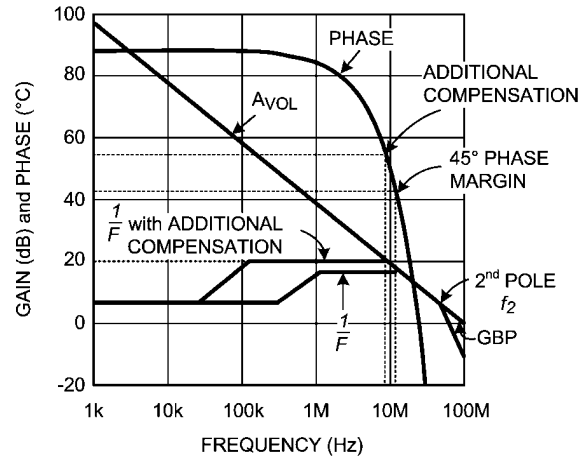
- $1/F$'s zero is located at a lower frequency compared with $1/F$'s pole.
- $1/F$'s value at low frequency is $1 + R_F/R_{IN}$.
- This method creates one additional pole and one additional zero.
- This pole-zero pair will serve two purposes:
 - To raise the $1/F$ value at higher frequencies prior to its intercept with A , the open loop gain curve, in order to meet the $G_{min} = 10$ requirement. For the SM73302 some overcompensation will be necessary for good stability.
 - To achieve the previous purpose above with no additional loop phase delay.

Please note the constraint $1/F \geq G_{min}$ needs to be satisfied only in the vicinity where the open loop gain A and $1/F$ intersect; $1/F$ can be shaped elsewhere as needed. The $1/F$ pole must occur before the intersection with the open loop gain A . In order to have adequate phase margin, it is desirable to follow these two rules:

- Rule 1 $1/F$ and the open loop gain A should intersect at the frequency where there is a minimum of 45° of phase margin. When over-compensation is required the intersection point of A and $1/F$ is set at a frequency where the phase margin is above 45° , therefore increasing the stability of the circuit.
- Rule 2 $1/F$'s pole should be set at least one decade below the intersection with the open loop gain A in order to take advantage of the full 90° of phase lead brought by $1/F$'s pole which is F 's zero. This ensures that the effect of the zero is fully neutralized when the $1/F$ and A plots intersect each other.

Calculating Lead-Lag Compensation for SM73302

[Figure 5](#) is the same plot as [Figure 1](#), but the A_{VOL} and phase curves have been redrawn as smooth lines to more readily show the concepts covered, and to clearly show the key parameters used in the calculations for lead-lag compensation.



30157748

FIGURE 5. SM73302 Simplified Bode Plot

To obtain stable operation with gains under 10 V/V the open loop gain margin must be reduced at high frequencies to where there is a 45° phase margin when the gain margin of the circuit with the external compensation is 0 dB. The pole and zero in F , the feedback factor, control the gain margin at the higher frequencies. The distance between F and A_{VOL} is the gain margin; therefore, the unity gain point (0 dB) is where F crosses the A_{VOL} curve.

For the example being used $R_{IN} = R_F$ for a gain of -1 . Therefore $F = 6$ dB at low frequencies. At the higher frequencies the minimum value for F is 18 dB for 45° phase margin. From [Equation 5](#) we have the following relationship:

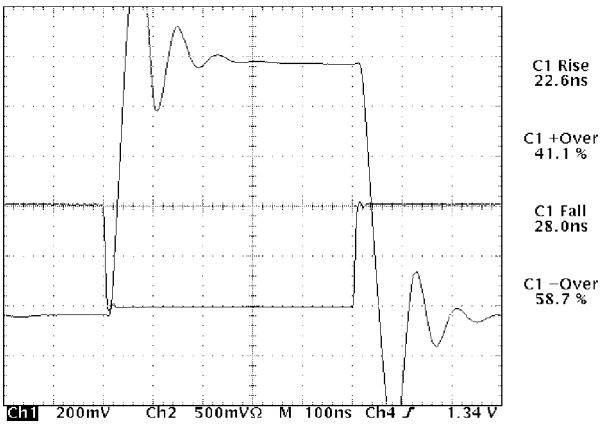
$$\left(1 + \frac{R_F}{R_{IN}}\right) \left(1 + \frac{R_{IN} \parallel R_F}{R_C}\right) = 18 \text{ dB} = 7.9$$

Now set $R_F = R_{IN} = R$. With these values and solving for R_C we have $R_C = R/5.9$. Note that the value of C does not affect the ratio between the resistors. Once the value of the resistors is set, then the position of the pole in F must be set. A 2 k Ω resistor is used for R_F and R_{IN} in this design. Therefore the value for R_C is set at 330 Ω , the closest standard value for 2 k $\Omega/5.9$.

Rewriting [Equation 2](#) to solve for the minimum capacitor value gives the following equation:

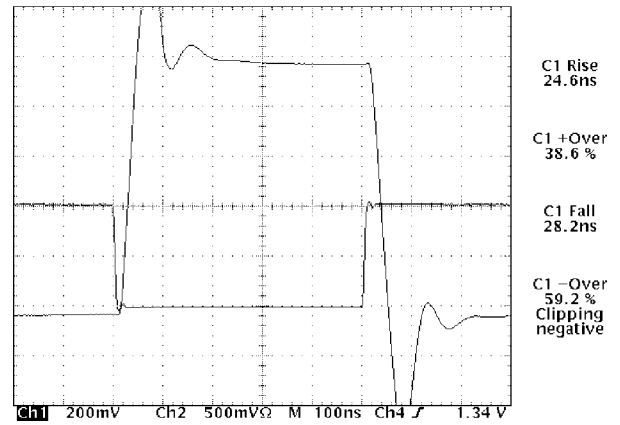
$$C = 1/(2\pi f_p R_C)$$

The feedback factor curve, F , intersects the A_{VOL} curve at about 12 MHz. Therefore the pole of F should not be any larger than 1.2 MHz. Using this value and $R_C = 330\Omega$ the minimum value for C is 390 pF. [Figure 6](#) shows that there is too much overshoot, but the part is stable. Increasing C to 2.2 nF did not improve the ringing, as shown in [Figure 7](#).

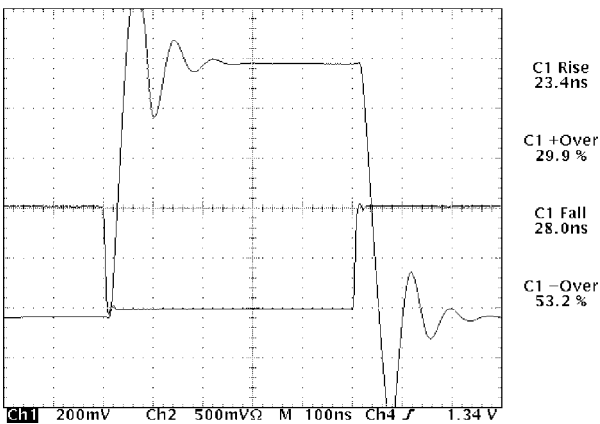


30157703

FIGURE 6. First Try at Compensation, Gain = -1

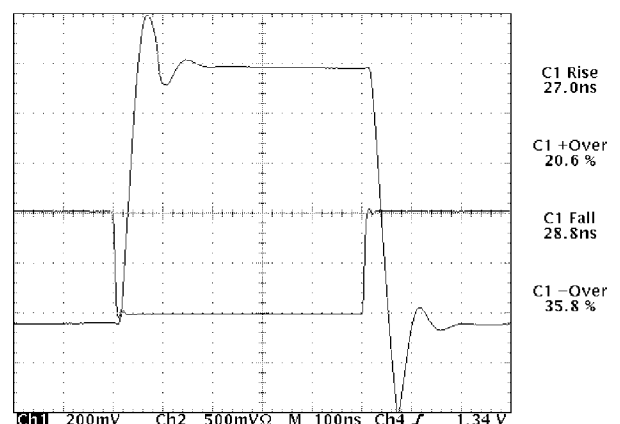


30157708

FIGURE 8. $R_C = 240\Omega$ and $C = 390$ pF, Gain = -1

30157707

FIGURE 7. C Increased to 2.2 nF, Gain = -1



30157710

FIGURE 9. $R_C = 240\Omega$ and $C = 2.2$ nF, Gain = -1

Some over-compensation appears to be needed for the desired overshoot characteristics. Instead of intersecting the A_{VOL} curve at 18 dB, 2 dB of over-compensation will be used, and the A_{VOL} curve will be intersected at 20 dB. Using Equation 5 for 20 dB, or 10 V/V, the closest standard value of R_C is 240Ω. The following two waveforms show the new resistor value with $C = 390$ pF and 2.2 nF. Figure 9 shows the final compensation and a very good response for the 1 MHz square wave.

To summarize, the following steps were taken to compensate the SM73302 for a gain of -1:

1. Values for R_C and C were calculated from the Bode plot to give an expected phase margin of 45°. The values were based on $R_{IN} = R_F = 2$ kΩ. These calculations gave $R_C = 330\Omega$ and $C = 390$ pF.
2. To reduce the ringing C was increased to 2.2 nF which moved the pole of F , the feedback factor, farther away from the A_{VOL} curve.
3. There was still too much ringing so 2 dB of over-compensation was added to F . This was done by decreasing R_C to 240Ω.

The LMP7715 is the fully compensated part (without the Renewable Energy Grade), which is comparable to the SM73302. Using the LMP7715 in the same setup, but removing the compensation network, provided the response shown in Figure 10.

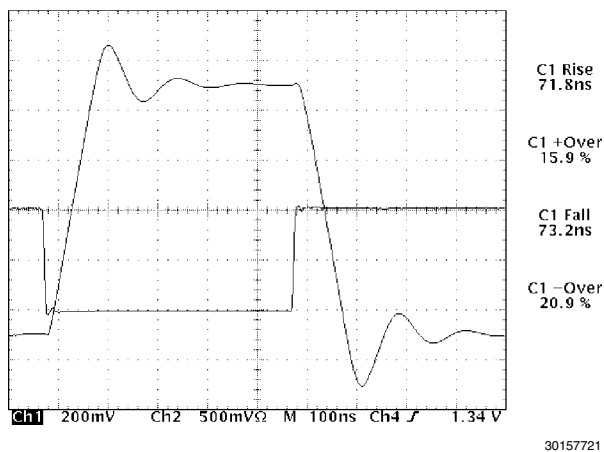


FIGURE 10. LMP7715 Response

For large signal response the rise and fall times are dominated by the slew rate of the op amps. Even though both parts are quite similar the SM73302 will give rise and fall times about 2.5 times faster than the LMP7715. This is possible because the SM73302 is a decompensated op amp and even though it is being used at a gain of -1 , the speed is preserved by using a good technique for external compensation.

Non-Inverting Compensation

For the non-inverting amp the same theory applies for establishing the needed compensation. When setting the inverting configuration for a gain of -1 , F has a value of 2. For the non-inverting configuration both F and the actual gain are the same, making the non-inverting configuration more difficult to compensate. Using the same circuit as shown in [Figure 4](#), but setting up the circuit for non-inverting operation (gain of $+2$) results in similar performance as the inverting configuration with the inputs set to half the amplitude to compensate for the additional gain. [Figure 11](#) below shows the results.

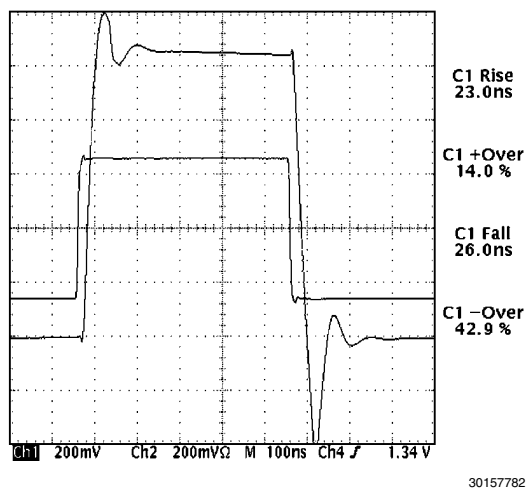


FIGURE 11. $R_C = 240\Omega$ and $C = 2.2$ nF, Gain = $+2$

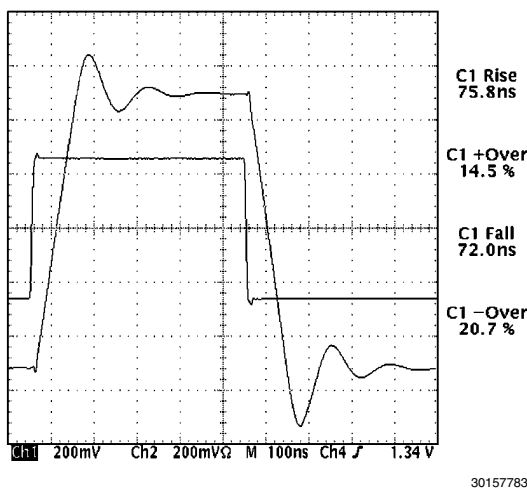


FIGURE 12. LMP7715 Response Gain = $+2$

The response shown in [Figure 11](#) is close to the response shown in [Figure 9](#). The part is actually slightly faster in the non-inverting configuration. Decreasing the value of R_C to around 200Ω can decrease the negative overshoot but will have slightly longer rise and fall times. The other option is to add a small resistor in series with the input signal. [Figure 12](#) shows the performance of the LMP7715 with no compensation. Again the decompensated parts are almost 2.5 times faster than the fully compensated op amp.

The most difficult op amp configuration to stabilize is the gain of $+1$. With proper compensation the SM73302 can be used in this configuration and still maintain higher speeds than the

fully compensated parts. *Figure 13* shows the gain = 1, or the buffer configuration, for these parts.

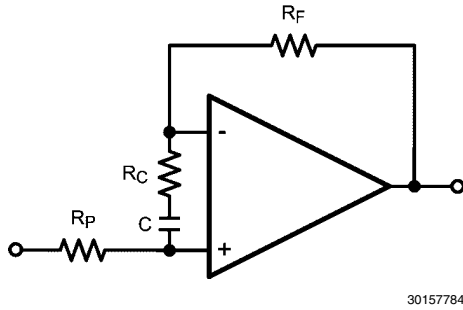


FIGURE 13. SM73302 with Lead-Lag Compensation for Non-Inverting Configuration

Figure 13 is the result of using *Equation 5* and additional experimentation in the lab. R_p is not part of *Equation 5*, but it is necessary to introduce another pole at the input stage for good performance at gain = +1. *Equation 5* is shown below with $R_{IN} = \infty$.

$$\left(1 + \frac{R_F}{R_C}\right) = 18 \text{ dB} = 7.9$$

Using 2 kΩ for R_F and solving for R_C gives $R_C = 2000/6.9 = 290\Omega$. The closest standard value for R_C is 300Ω. After some fine tuning in the lab $R_C = 330\Omega$ and $R_p = 1.5 \text{ k}\Omega$ were chosen as the optimum values. R_p together with the input capacitance at the non-inverting pin inserts another pole into the compensation for the SM73302. Adding this pole and slightly reducing the compensation for 1/F (using a slightly higher resistor value for R_C) gives the optimum response for a gain of +1. *Figure 14* is the response of the circuit shown in *Figure 13*. *Figure 15* shows the response of the LMP7715 in the buffer configuration with no compensation and $R_p = R_f = 0$.

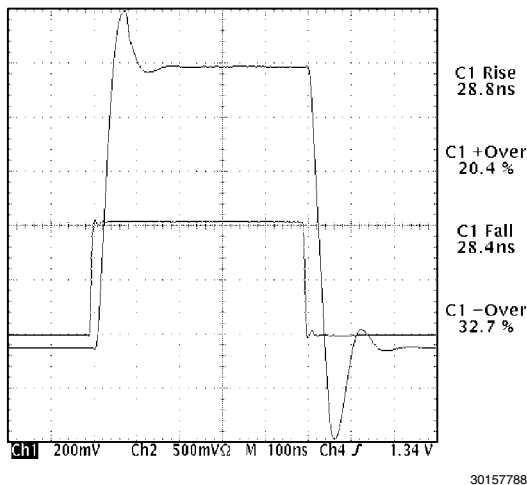


FIGURE 14. $R_C = 330\Omega$ and $C = 10 \text{ nF}$, Gain = +1

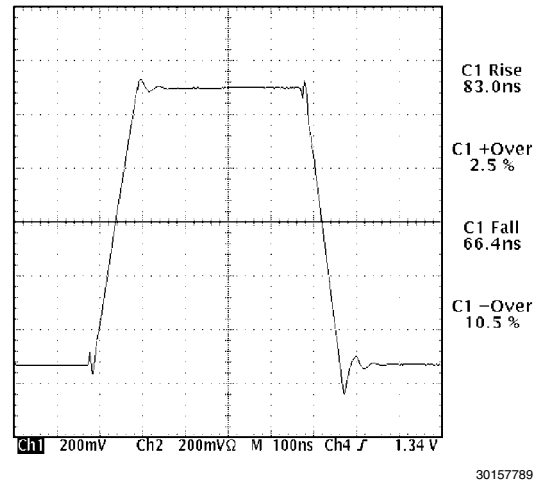


FIGURE 15. LMP7715 Response Gain = +1

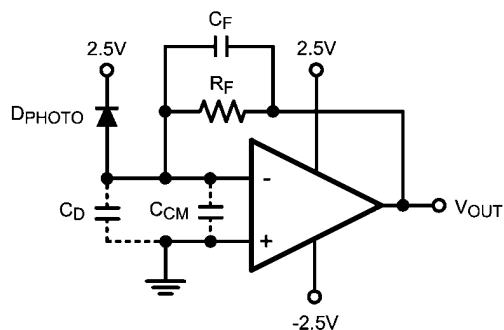
With no increase in power consumption the decompensated op amp offers faster speed than the compensated equivalent part. These examples used $R_F = 2 \text{ k}\Omega$. This value is high enough to be easily driven by the SM73302, yet small enough to minimize the effects from the parasitic capacitance of both the PCB and the op amp.

Note: When using the SM73302, proper high frequency PCB layout must be followed. The GBW of these parts is 88 MHz, making the PCB layout significantly more critical than when using the compensated counterparts which have a GBW of 17 MHz.

TRANSIMPEDANCE AMPLIFIER

An excellent application for the SM73302 is as a transimpedance amplifier. With a GBW product of 88 MHz this part is ideal for high speed data transmission by light. The circuit shown on the front page of the datasheet is the circuit used to test the SM73302 as a transimpedance amplifier. The only change is that V_B is tied to the V_{CC} of the part, thus the direction of the diode is reversed from the circuit shown on the front page.

Very high speed components were used in testing to check the limits of the SM73302 in a transimpedance configuration. The photodiode part number is PIN-HR040 from OSI Optoelectronics. The diode capacitance for this part is only about 7 pF for the 2.5V bias used (V_{CC} to virtual ground). The rise time for this diode is 1 nsec. A laser diode was used for the light source. Laser diodes have on and off times under 5 nsec. The speed of the selected optical components allowed an accurate evaluation of the SM73302 as a transimpedance amplifier. Nationals evaluation board for decompensated op amps, PN 551013271-001 A, was used and only minor modifications were necessary and no traces had to be cut.

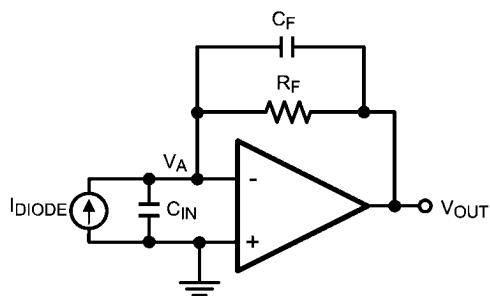


30157761

FIGURE 16. Transimpedance Amplifier

Figure 16 is the complete schematic for a transimpedance amplifier. Only the supply bypass capacitors are not shown. C_D represents the photodiode capacitance which is given on its datasheet. C_{CM} is the input common mode capacitance of the op amp and, for the SM73302 it is shown in the last graph of the Typical Performance Characteristics section of this datasheet. In Figure 16 the inverting input pin of the SM73302 is kept at virtual ground. Even though the diode is connected to the 2.5V line, a power supply line is AC ground, thus C_D is connected to ground.

Figure 17 shows the schematic needed to derive F, the feedback factor, for a transimpedance amplifier. In this figure $C_D + C_{CM} = C_{IN}$. Therefore it is critical that the designer knows the diode capacitance and the op amp input capacitance. The photodiode is close to an ideal current source once its capacitance is included in the model. What kind of circuit is this? Without C_F there is only an input capacitor and a feedback resistor. This circuit is a differentiator! Remember, differentiator circuits are inherently unstable and must be compensated. In this case C_F compensates the circuit.



30157764

FIGURE 17. Transimpedance Feedback Model

Using feedback theory, $F = V_A/V_{OUT}$, this becomes a voltage divider giving the following equation:

$$F = \frac{1 + sC_F R_F}{1 + sR_F (C_F + C_{IN})}$$

The noise gain is $1/F$. Because this is a differentiator circuit, a zero must be inserted. The location of the zero is given by:

$$f_z = \frac{1}{1 + sR_F (C_F + C_{IN})}$$

C_F has been added for stability. The addition of this part adds a pole to the circuit. The pole is located at:

$$f_p = \frac{1}{1 + sC_F R_F}$$

To attain maximum bandwidth and still have good stability the pole is to be located on the open loop gain curve which is A. If additional compensation is required one can always increase the value of C_F , but this will also reduce the bandwidth of the circuit. Therefore $A = 1/F$, or $AF = 1$. For A the equation is:

$$A = \frac{\omega_{GBW}}{\omega} = \frac{f_{GBW}}{f}$$

The expression f_{GBW} is the gain bandwidth product of the part. For a unity gain stable part this is the frequency where $A = 1$. For the SM73302 $f_{GBW} = 88$ MHz. Multiplying A and F results in the following equation:

$$AF|_{f_p} = \frac{f_{GBW}}{f} \times \frac{1 + sC_F R_F}{1 + sR_F (C_F + C_{IN})} =$$

$$\frac{f_{GBW}}{f} \times \frac{\sqrt{1 + \left(\frac{C_F R_F}{C_F R_F}\right)^2}}{\sqrt{1 + \left(\frac{R_F (C_F + C_{IN})}{C_F R_F}\right)^2}} = 1$$

For the above equation $s = j\omega$. To find the actual amplitude of the equation the square root of the square of the real and imaginary parts are calculated. At the intersection of F and A, we have:

$$\omega = \frac{1}{C_F R_F}$$

After a bit of algebraic manipulation the above equation reduces to:

$$1 + \left(\frac{C_F + C_{IN}}{C_F} \right)^2 = 8\pi^2 f_{GBW}^2 R_F^2 C_F^2$$

In the above equation the only unknown is C_F . In trying to solve this equation the fourth power of C_F must be dealt with. An excel spread sheet with this equation can be used and all the known values entered. Then through iteration, the value of C_F when both sides are equal will be found. That is the correct value for C_F and of course the closest standard value is used for C_F .

Before moving to the lab, the transfer function of the transimpedance amplifier must be found and the units must be in Ohms.

$$V_{OUT} = \frac{-R_F}{1 + sC_F R_F} \times I_{DIODE}$$

The SM73302 was evaluated for $R_F = 10\text{ k}\Omega$ and $100\text{ k}\Omega$, representing a somewhat lower gain configuration and with the $100\text{ k}\Omega$ feedback resistor a fairly high gain configuration. The $R_F = 10\text{ k}\Omega$ is covered first. Looking at the *Input Common Mode Capacitance vs. V_{CM}* chart for C_{CM} for the operating point selected $C_{CM} = 15\text{ pF}$. Note that for split supplies $V_{CM} = 2.5\text{V}$, $C_{IN} = 22\text{ pF}$ and $f_{GBW} = 88\text{ MHz}$. Solving for C_F the calculated value is 1.75 pF , so 1.8 pF is selected for use. Checking the frequency of the pole finds that it is at 8.8 MHz , which is right at the minimum gain recommended for this part. Some over compensation was necessary for stability and the final selected value for C_F is 2.7 pF . This moves the pole to 5.9 MHz . *Figure 18* and *Figure 19* show the rise and fall times obtained in the lab with a 1V output swing. The laser diode was difficult to drive due to thermal effects making the starting and ending point of the pulse quite different, therefore the two separate scope pictures.

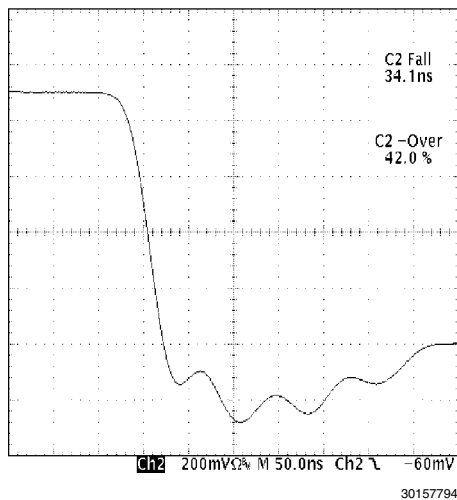


FIGURE 18. Fall Time

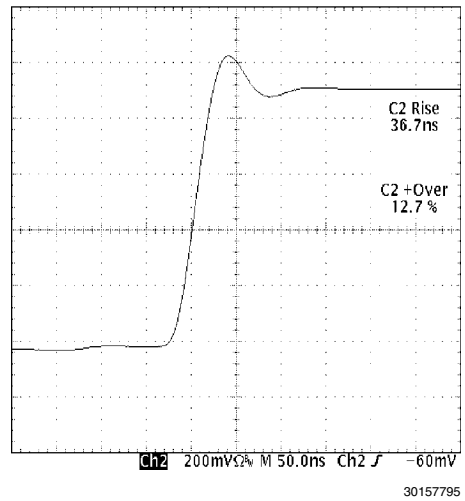


FIGURE 19. Rise Time

In *Figure 18* the ringing and the hump during the on time is from the laser. The higher drive levels for the laser gave ringing in the light source as well as light changing from the thermal characteristics. The hump is due to the thermal characteristics.

Solving for C_F using a $100\text{ k}\Omega$ feedback resistor, the calculated value is 0.54 pF . One of the problems with more gain is the very small value for C_F . A 0.5 pF capacitor was used, its measured value being 0.64 pF . For the 0.64 pF location the pole is at 2.5 MHz . *Figure 20* shows the response for a 1V output.

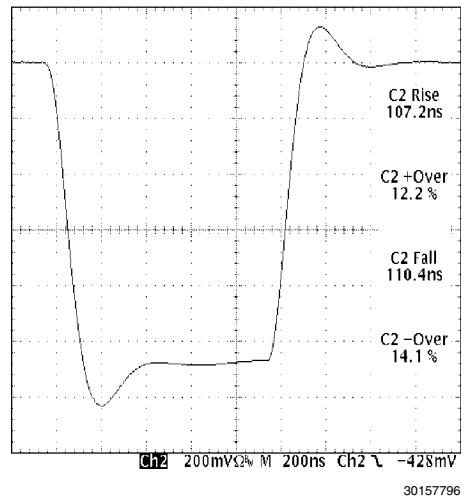
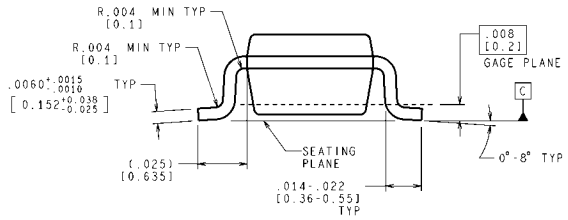
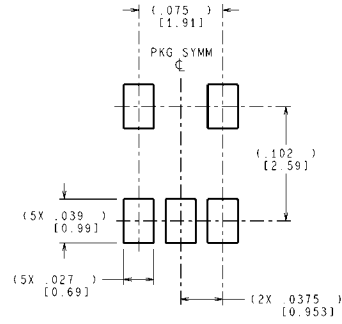
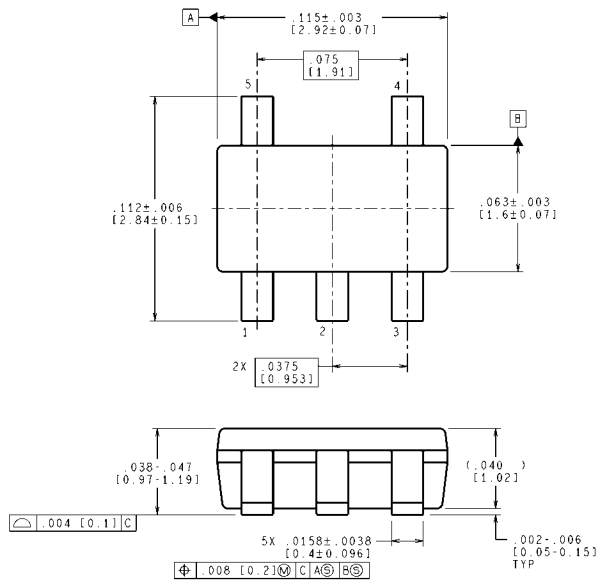


FIGURE 20. High Gain Response

A transimpedance amplifier is an excellent application for the SM73302. Even with the high gain using a $100\text{ k}\Omega$ feedback resistor, the bandwidth is still well over 1 MHz . Other than a little over compensation for the $10\text{ k}\Omega$ feedback resistor configuration using the SM73302 was quite easy. Of course a very good board layout was also used for this test.

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
 VALUES IN [] ARE MILLIMETERS
 DIMENSIONS IN () FOR REFERENCE ONLY

5-Pin SOT23
NS Package Number MF05A

MF05A (Rev D)

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2011 National Semiconductor Corporation
 For the most current product information visit us at www.national.com

 <p>National Semiconductor Americas Technical Support Center Email: support@nsc.com Tel: 1-800-272-9959</p>	<p>National Semiconductor Europe Technical Support Center Email: europe.support@nsc.com</p>	<p>National Semiconductor Asia Pacific Technical Support Center Email: ap.support@nsc.com</p>	<p>National Semiconductor Japan Technical Support Center Email: jpn.feedback@nsc.com</p>
--	---	---	--

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated