



Presetable BCD/Decade UP/Down Counter

ELECTRICALLY TESTED PER:
MIL-M-38510/31507

The 54LS192 is an UP/DOWN BCD Decade (8421) Counter and the 54LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

- Low Power . . . 95 mW Typical Dissipation
- High-Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High-Speed Termination Effects

Military 54LS192



AVAILABLE AS:

- 1) JAN: JM38510/31507BXA
- 2) SMD: 7603601
- 3) 883: 54LS192/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
P ₁	1	1	2	VCC
Q ₁	2	2	3	VCC
Q ₀	3	3	4	VCC
CP _D	4	4	5	VCC
CP _U	5	5	7	VCC
Q ₂	6	6	8	VCC
Q ₃	7	7	9	VCC
GND	8	8	10	GND
P ₃	9	9	12	VCC
P ₂	10	10	13	VCC
PL	11	11	14	GND
TC _U	12	12	15	OPEN
TC _D	13	13	17	VCC
MR	14	14	18	GND
P ₀	15	15	19	VCC
VCC	16	16	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

MR	PL	CP _U	CP _D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	┌	H	Count Up
L	H	└	└	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
┌ = LOW-to-HIGH Clock Transition

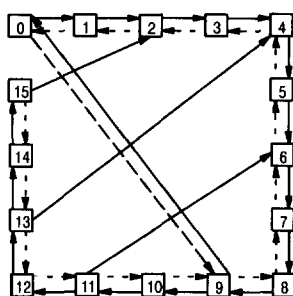
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Pin Names	Loading (Note a)	
	HIGH	LOW
CP _U	Count UP Clock Pulse Input	0.5 U.L. / 0.25 U.L.
CP _D	Count Down Clock Pulse Input	0.5 U.L. / 0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L. / 0.25 U.L.
PL	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L. / 0.25 U.L.
P _n	Parallel Data Inputs	0.5 U.L. / 0.25 U.L.
Q _n	Flip-Flop Outputs (Note b)	10 U.L. / 5(2.5) U.L.
TC _D	Terminal Count Down (Borrow) Output (Note b)	10 U.L. / 5(2.5) U.L.
TC _U	Terminal Count Up (Carry) Output (Note b)	10 U.L. / 5(2.5) U.L.

NOTES:

- One TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

STATE DIAGRAM



LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$TC_U = Q_0 \cdot Q_3 \cdot \overline{CP_U}$$

$$TC_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_D}$$

FUNCTIONAL DESCRIPTION

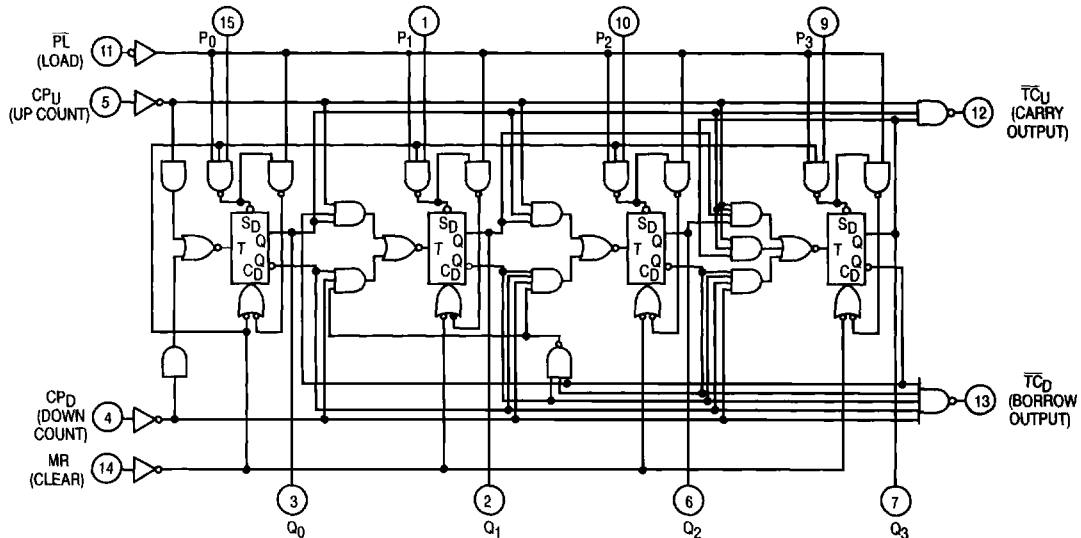
The 'LS192 and 'LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversible) Counters. The operating modes of the 'LS192 decade counter and 'LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the 'LS192, 15 for the 'LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

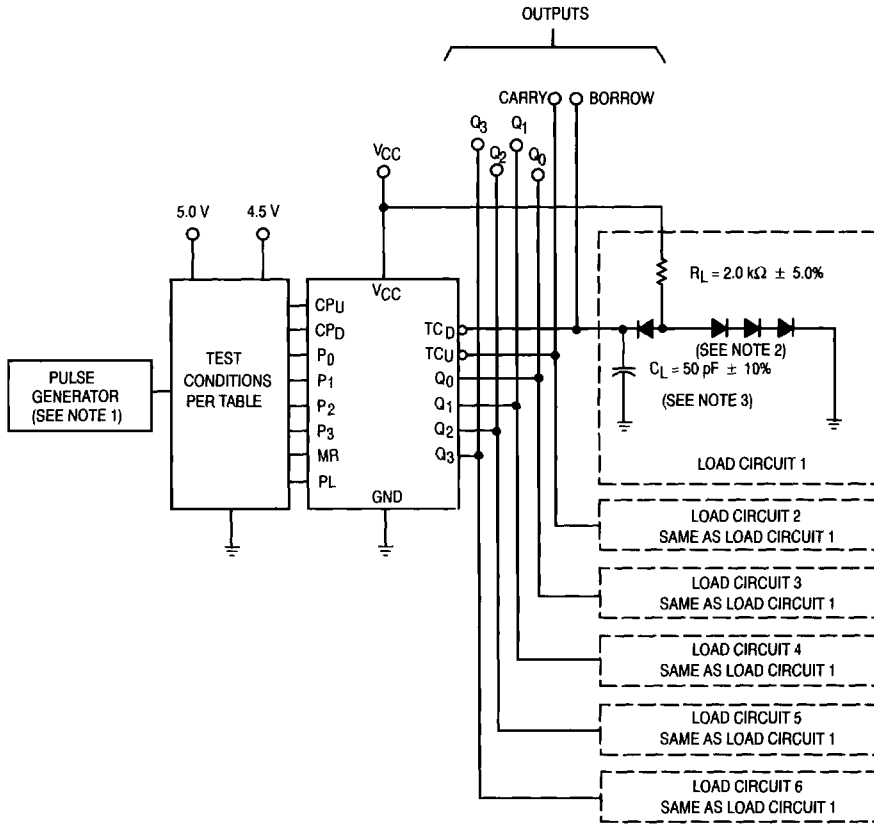
Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (\overline{PL}) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM

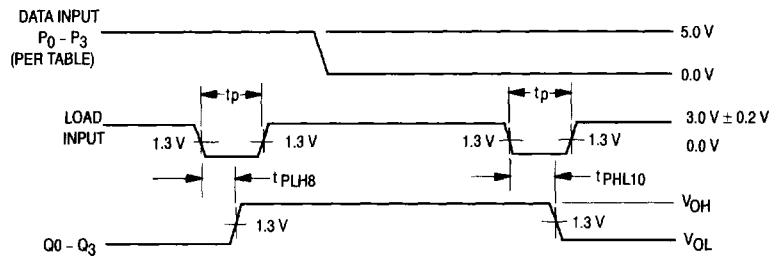


54LS192

AC TEST CIRCUIT

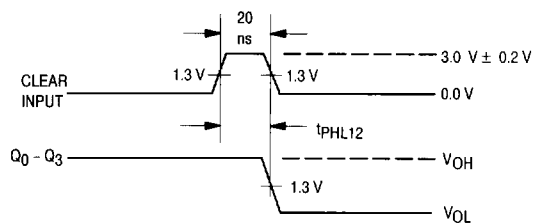


WAVEFORMS

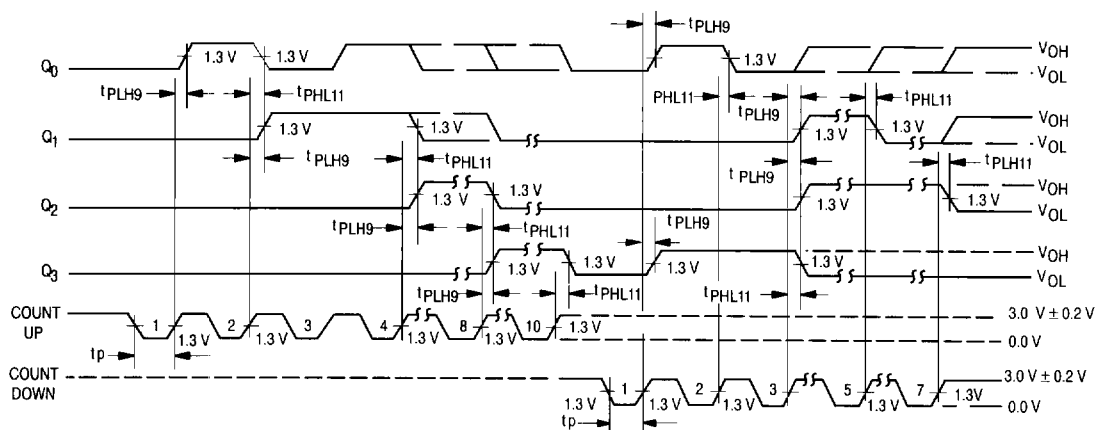


REFERENCE NOTES ON PAGE 5-265

CLEAR SWITCHING VOLTAGE WAVEFORM



SERIAL LOADED VOLTAGE WAVEFORMS



NOTES:

- The load and count pulse generators have the following characteristics:
 $V_{gen} = 3.0 \text{ V}$, $t_p = 0.5 \mu\text{s}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$
 between 0.7 V and 2.7 V and $PRR \leq 1.0 \text{ MHz}$, $Z_{OUT} = 50 \Omega$.
- All diodes are 1N3064, or equivalent.
- $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
- Voltage values are with respect to ground terminal.
- f_{MAX} : $t_r = t_f \leq 6.0 \text{ ns}$.
- The clear pulse generator has the following characteristics:
 $V_{gen} = 3.0 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$ between 0.7 V and 2.7 V, $t_w(\text{clear}) = 20 \text{ ns}$.
- $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.

54LS192

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = - 0.4 mA, V _{IN} = 2.0 V, other inputs are open, MR & \overline{PL} = 0.7 V.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IN} = 0.7 V, other inputs are open, P ₀ , P ₃ & MR = 0.7 V or 2.0 V.
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open, MR & \overline{PL} = 5.5 V or 2.7 V.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are open.
I _{IL}	Logical "0" Input Current	- 120	- 360	- 120	- 360	- 120	- 360	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, \overline{PL} & MR = GND, other inputs are open.
I _{IL}	Logical "0" Input Current	- 120	- 360	- 120	- 360	- 120	- 360	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V (\overline{PL}), other inputs are open.
I _{IL}	Logical "0" Input Current	- 120	- 360	- 120	- 360	- 120	- 360	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V (\overline{TC} & MR), other inputs are open.
I _{OS}	Output Short Circuit Current	-15	- 100	-15	-100	-15	- 100	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are open, V _{OUT} = GND.
I _{CC}	Power Supply Current Off		34		34		34	mA	V _{CC} = 5.5 V, V _{IN} = GND (\overline{PL} & MR), other inputs are open.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

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54LS192

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
	Min	Max	Min	Max	Min	Max			
t _{PHL10} t _{PHL10}	Propagation Delay /Data-Output P _L to Q Outputs	3.0 —	45 40	3.0 —	63 58	3.0 —	63 58	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH8} t _{PLH8}	Propagation Delay /Data-Output P _L to Q Outputs	3.0 —	45 40	3.0 —	63 58	3.0 —	63 58	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PHL11} t _{PHL11}	Propagation Delay C _{PD} or C _{PJ} to Q Outputs	3.0 —	52 47	3.0 —	72 68	3.0 —	72 68	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH9} t _{PLH9}	Propagation Delay C _{PD} or C _{PJ} to Q Outputs	3.0 —	43 38	3.0 —	60 55	3.0 —	60 55	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PHL12} t _{PHL12}	Propagation Delay MR (Clear) to Q Outputs	3.0 —	40 35	3.0 —	56 51	3.0 —	56 51	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PHL13} t _{PHL13}	Propagation Delay Counter to Carry	3.0	29	3.0	41	3.0	41	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PLH13} t _{PLH13}	Propagation Delay Counter to Carry	3.0	31	3.0	45	3.0	45	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PHL14} t _{PHL14}	Propagation Delay Counter to Carry	3.0	29	3.0	41	3.0	41	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PLH14} t _{PLH14}	Propagation Delay Counter to Carry	3.0	29	3.0	45	3.0	45	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
f _{MAX}	Input Clock Frequency	22		22		22		MHz	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
f _{MAX}	Input Clock Frequency	25						MHz	V _{CC} = 5.0 V, C _L = 15 pF.

NOTE:

- The limit specified for C_L = 15 pF are guaranteed but not tested.