Old Company Name in Catalogs and Other Documents

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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)
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MOS FIELD EFFECT TRANSISTOR 2SJ324,324-Z

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ324 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

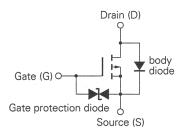
- · Low On-state Resistance
 - $R_{DS(on)} = 0.18 \Omega \text{ TYP. (Vgs} = -10 \text{ V, Ip} = -1.0 \text{ A)}$
 - $R_{DS(on)}$ = 0.36 Ω TYP. (V_{GS} = -4 V, I_D = -0.8 A)
- Low Ciss: Ciss = 330 pF TYP.
- · Built-in G-S Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

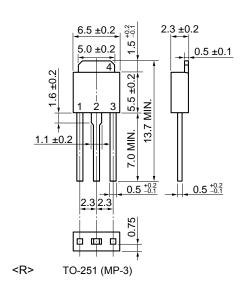
Drain to Source Voltage	V _{DSS}	-30	V
Gate to Source Voltage (AC)	V _{GSS}	∓20	V
Gate to Source Voltage (DC)	V _{GSS}	-20, +10	V
Drain Current (DC)	I _{D(DC)}	∓2.0	Α
Drain Current (pulse) Note	I _{D(pulse)}	∓8.0	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	20	W
Total Power Dissipation (T _A = 25°C)	P_{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

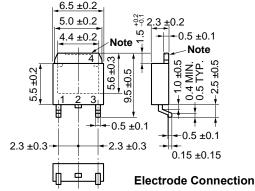
Note PW \leq 10 μ s, Duty Cycle \leq 1%

EQUIVALENT CIRCUIT



PACKAGE DRAWINGS (Unit: mm)





1. Gate

TO-252 (MP-3Z)

Drain
 Source

4. Drain Fin

Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

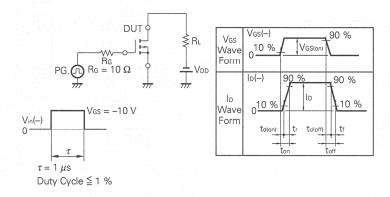
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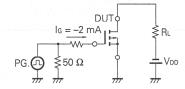
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS		
Drain to Source On-state Resistance	RDS(on)		0.18	0.25	Ω	Vgs = -10 V, ID = -1.0 A		
Drain to Source On-state Resistance	Ros(on)		0.36	0.52	Ω	Vgs = -4 V, Ip = -0.8 A		
Gate to Source Cutoff Voltage	V _{GS(off)}	-1.0	-1.5	-2.0	V	V _{DS} = −10 V, I _D = −1 mA		
Forward Transfer Admittance	y fs	1.0	1.9		S	V _{DS} = -10 V, I _D = -1.0 A		
Drain Leakage Current	Ipss			-10	μΑ	Vps = -30 V, Vgs = 0		
Gate to Source Leakage Current	Igss			±10	μΑ	Vgs = ∓16 V, Vps = 0		
Input Capacitance	Ciss		330		pF	Vps = -10 V		
Output Capacitance	Coss		290		pF	Vgs = 0		
Reverse Transfer Capacitance	Crss		105		pF	f = 1 MHz		
Turn-On Delay Time	td(on)		. 7		ns	VGS(on) = -10 V VDD = -15 V		
Rise Time	tr		35		ns			
Turn-Off Delay Time	td(off)		40		ns	$ID = -1.0 \text{ A, Rg} = 10 \Omega$ $RL = 15 \Omega$		
Fall Time	t _f		30	ei 7	ns			
Total Gate Charge	Qg		12		nC	Vgs = -10 V		
Gate to Source Charge	Qgs		1.5		nC	I _D = -2.0 A		
Gate to Drain Charge	QgD		4.5		nC	VDD = -24 V		
Body Diode Forward Voltage	VF		0.9		V	IF = 2.0 A, VGS = 0		
Reverse Recovery Time	trr		50		ns	I _F = 2.0 A, V _{GS} = 0 di/dt = 50 A/μs		
Reverse Recovery Charge	Qrr		40		nC			
ESD	Vesd		±130	14 200 440	V	C = 200 pF, R = 0, Single Pul		

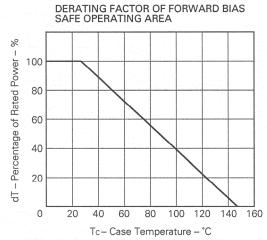
Test Circuit 1: Switching Time

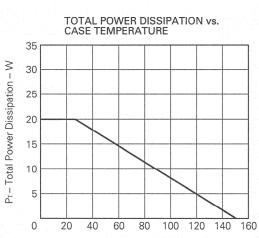


Test Circuit 2: Gate Charge

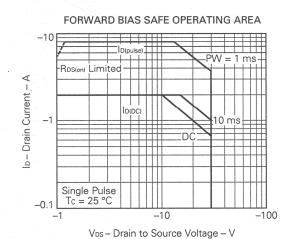


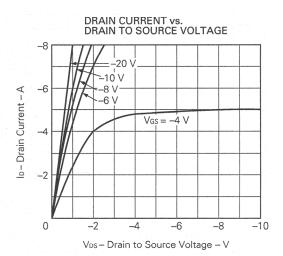
TYPICAL CHARACTERISTICS (Ta = 25 °C)

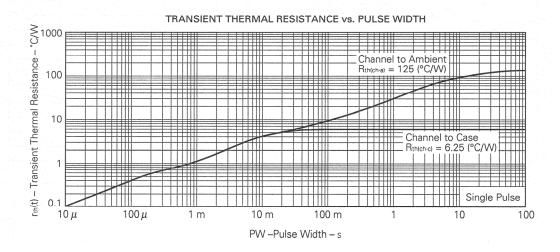


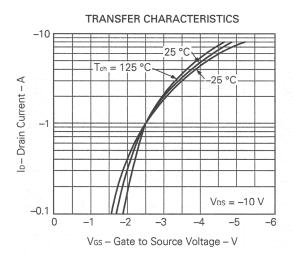


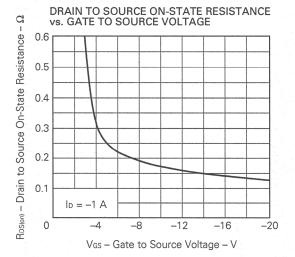
Tc - Case Temperature - °C

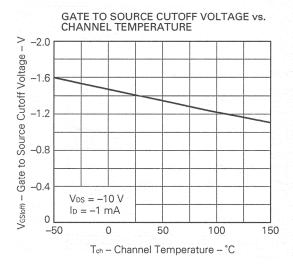




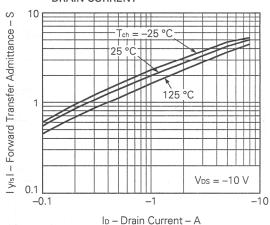




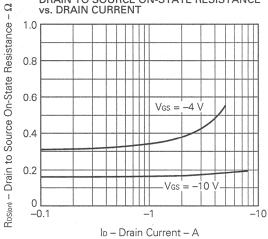




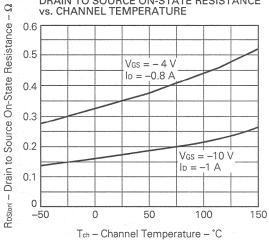


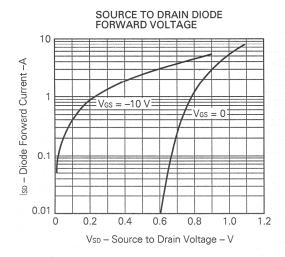


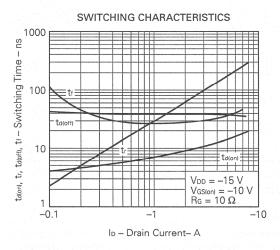
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

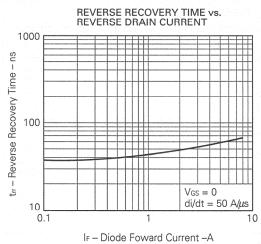


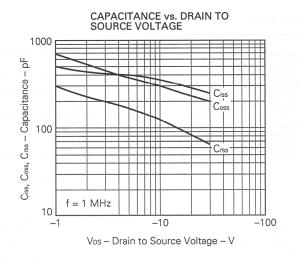
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

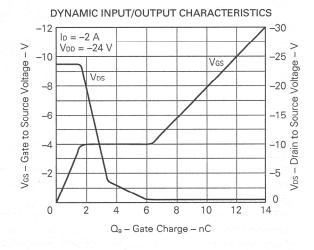












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