XICOR®

16K X20C16 2K x 8 Bit

High Speed AUTOSTORE™ NOVRAM

FEATURES

- **Fast access time: 35ns, 45ns, 55ns**
- **High reliability**
  - **—Endurance: 1,000,000 nonvolatile store operations**
  - **—Retention: 100 years minimum**
- **AUTOSTORE NOVRAM**
  - **—Automatically stores RAM data into the EEPROM array when V_{CC} low threshold is detected**
  - **—User enabled option**
  - **—Open drain autostore status output pin**
- **Power-on recall**
  - **—EEPROM data automatically recalled into RAM upon power-up**
- **Software data protection**
  - **—Locks out inadvertent store operations**
- **Low power CMOS**
  - **—Standby: 250µA**
- **Infinite EEPROM array recall, and RAM read and write cycles**

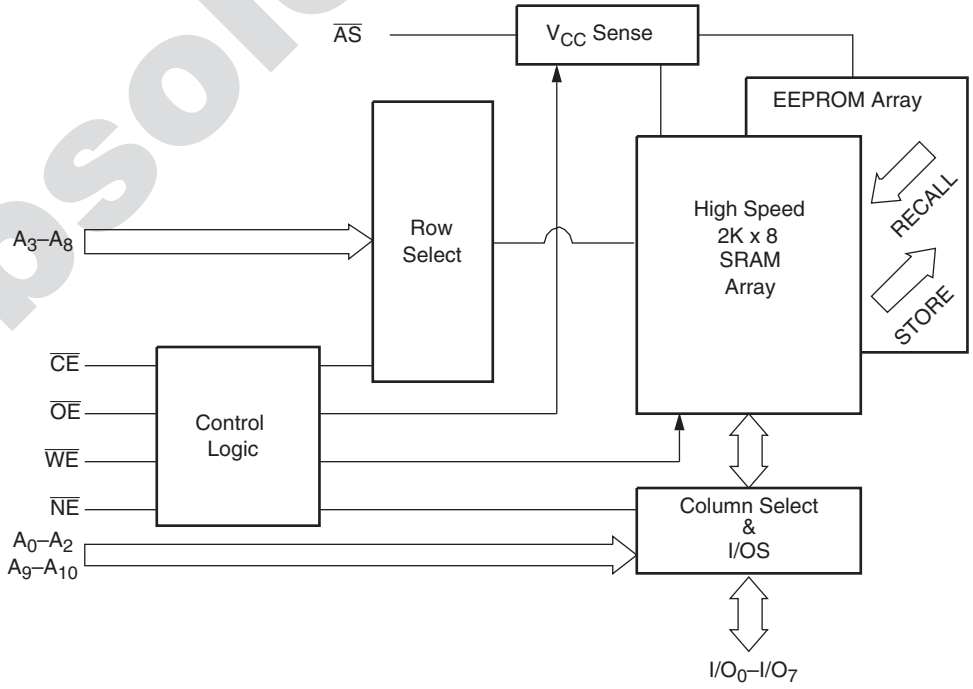
DESCRIPTION

The Xicor X20C16 is a 2K x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a non-volatile electrically erasable PROM (EEPROM) and the AUTOSTORE feature which automatically saves the RAM contents to EEPROM at power-down. The X20C16 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C16 features a compatible JEDEC approved pinout for byte-wide memories, for industry standard RAMs, ROMs, EPROMs, and EEPROMs.

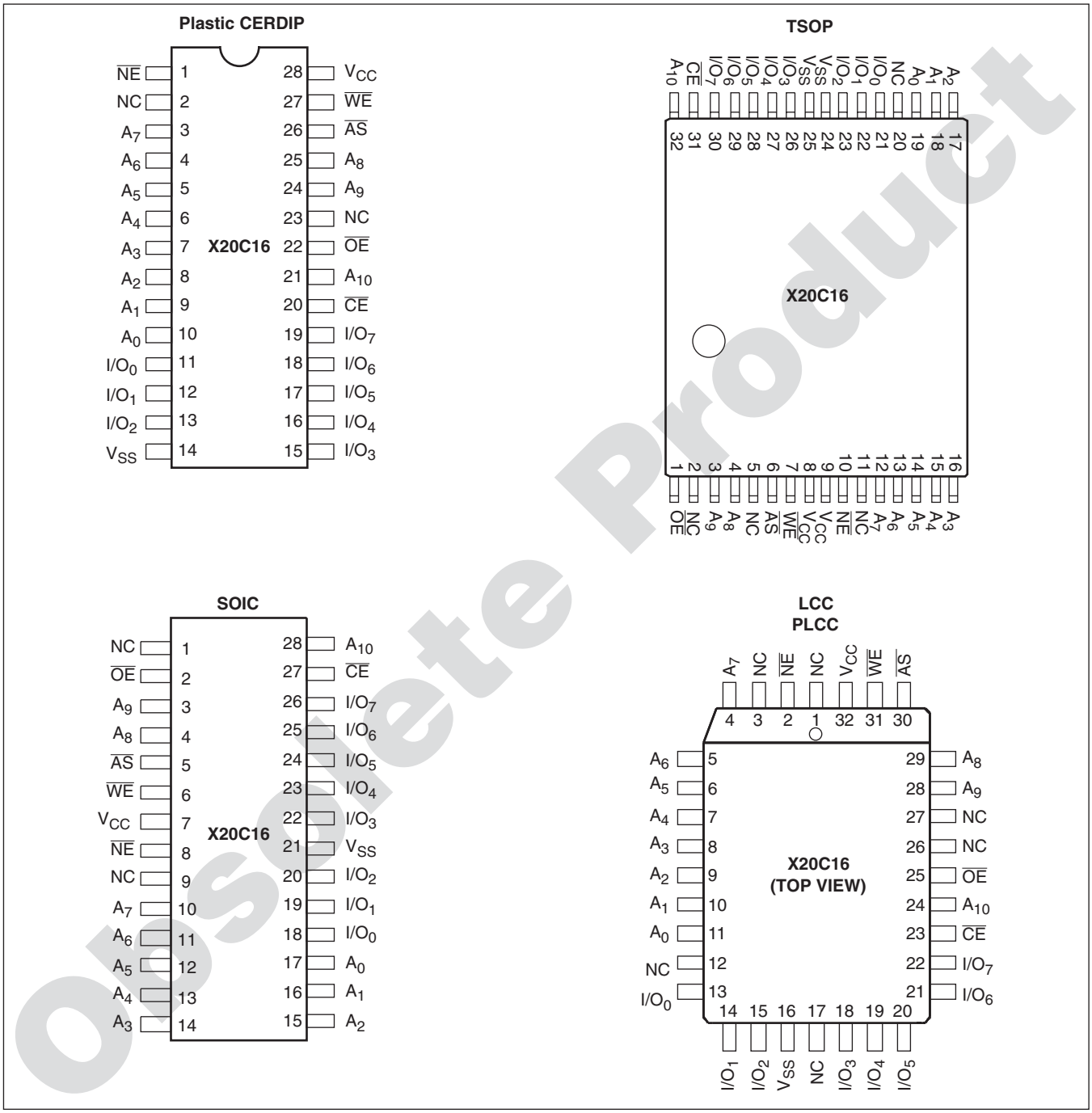
The NOVRAM design allows data to be easily transferred from RAM to EEPROM (store) and EEPROM to RAM (recall). The store operation is completed in 5ms or less and the recall operation is completed in 10µs or less. An automatic array recall operation reloads the contents of the EEPROM into RAM upon power-up.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from EEPROM, and a minimum 1,000,000 store operations to the EEPROM. Data retention is specified to be greater than 100 years.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Symbol	Description
A_0–A_{10}	Address inputs
I/O_0–I/O_7	Data input/output
$\overline{WE}$	Write enable
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{NE}$	Nonvolatile enable
$\overline{AS}$	AUTOSTORE output
V_{CC}	+5V
V_{SS}	Ground
NC	No connect

PIN DESCRIPTIONS

Addresses (A_0–A_{10})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$, or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C16 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the static RAM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls the recall function to the EEPROM array.

AUTOSTORE Output ($\overline{AS}$)

$\overline{AS}$ is an open drain output which, when asserted indicates V_{CC} has fallen below the AUTOSTORE threshold (V_{ASTH}). $\overline{AS}$ may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller.

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X20C16 operation. The X20C16 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C16.

Memory Transfer Operations

There are two memory transfer operations: a recall operation whereby the data stored in the EEPROM array is transfered to the RAM array; and a store operation which causes the entire contents of the RAM array to be stored in the EEPROM array.

Recall operations are performed automaticaly upon power-up and under host system control when $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. The recall operation takes a maximum of 5µs.

SDP (Software Data Protection)

There are two methods on initiating a store operation. The first is the software store command. This command takes the place of the hardware store employed on the X20C04. This command is issued by entering into the special command mode: $\overline{NE}$, $\overline{CE}$, and $\overline{WE}$ strobe LOW while at the same time a specific address and data combination is sent to the device. This is a three step operation: the first address/data combination is 555[H]/AA[H]; the second combination is 2AA[H]/55[H]; and the final command conbination is 555[H]/33[H]. This sequence of pseudo write operations will immediately initiate a store operation. Refer to the software command timing diagrams for details on set and hold times for the various signals.

The second method of storing data is with the AUTOSTORE command. When enable, data is automatically stored for the RAM into the EEPROM array whenever V_{CC} falls below the preset Autostore threshold. This feature is enabled by performing the first two steps for the software store with the command combination being 555[H]/CC[H].

The AUTOSTORE feature is disable by issuing the three step command sequence with the command combination being 555[H]/CD[H]. The AUTOSTORE feature will also be reset if V_{CC} falls below the power-up reset threshold (approximately 3.5V) and is then raised back into the operation range.

Write Protection

The X20C16 supports two methods of protecting the nonvolatile data.

– If after power-up the AUTOSTORE feature is not enabled, no AUTOSTORE can occur.

– V_{CC} Sense—All functions are inhibited when V_{CC} is 3.0V typical.

The following symbol table provides a key to understanding the conventions used in the device timing diagrams. The diagrams should be used in conjunction with the device timing specifications to determine actual device operation and perfomance, as well as device suitability for user's application.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... –65°C to +135°C
Storage temperature ..... –65°C to +150°C
Voltage on any pin with
respect to V_{SS} .....–1V to +7V
D.C. output current 10mA
Lead temperature (soldering, 10 seconds)..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any conditions other than those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

Supply Voltage	Limits
X20C16	5V ±10%

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{CC1}	V_{CC} current (active)		100	mA	$\overline{NE}$ = $\overline{WE}$ = V_{IH}, $\overline{CE}$ = $\overline{OE}$ = V_{IL} Address inputs = 0.4V/2.4V levels @ f = 20MHz All I/Os = open
I_{CC2}	V_{CC} current during store		5	mA	All inputs = V_{IH} All I/Os = open
I_{CC3}(2)	V_{CC} current during AUTOSTORE		2.5	mA	
I_{SB1}	V_{CC} standby current (TTL input)		10	mA	$\overline{CE}$ = V_{IH}, All other inputs = V_{IH} All I/Os = open
I_{SB2}	V_{CC} standby current (CMOS input)		250	µA	All inputs = V_{CC} – 0.3V All I/Os = open
I_{LI}	Input leakage current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 4mA
V_{OLAS}	AUTOSTORE output		0.4	V	I_{OLAS} = 1mA
V_{OH}	Output HIGH voltage	2.4		V	I_{OH} = –4mA

POWER-UP TIMING

Symbol	Parameter	Max.	Unit
t_{PUR}(2)	Power-up to RAM operation	100	µs
t_{PUW}(2)	Power-up to nonvolatile operation	5	ms

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
$C_{I/O}$[2]	Input/output capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}[2]	Input capacitance	6	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

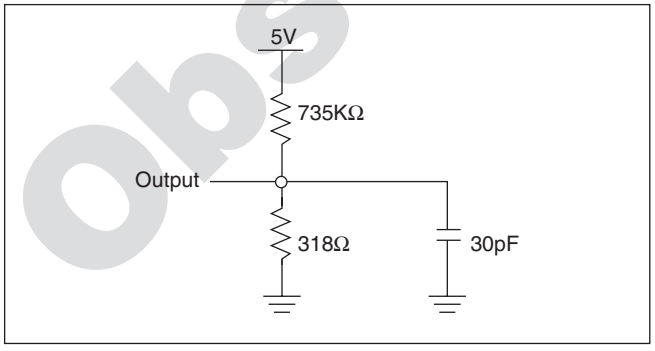
ENDURANCE AND DATA RETENTION

Parameter	Min.	Unit
Endurance	100,000	Data changes per bit
Store cycles	1,000,000	Store cycles
Data retention	100	Years

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not selected	Output high Z	Standby
L	H	H	L	Read RAM	Output data	Active
L	L	H	H	Write “1” RAM	Input data high	Active
L	L	H	H	Write “0” RAM	Input data low	Active
L	H	L	L	Array recall	Output high Z	Active
L	L	L	H	Software command	Input data	Active
L	H	H	H	Output Disabled	Output high Z	Active
L	L	L	L	Not allowed	Output high Z	Active
L	H	L	H	No operation	Output high Z	Active

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input pulse levels	0V to 3V
Input rise and fall times	5ns
Input and output timing levels	1.5V

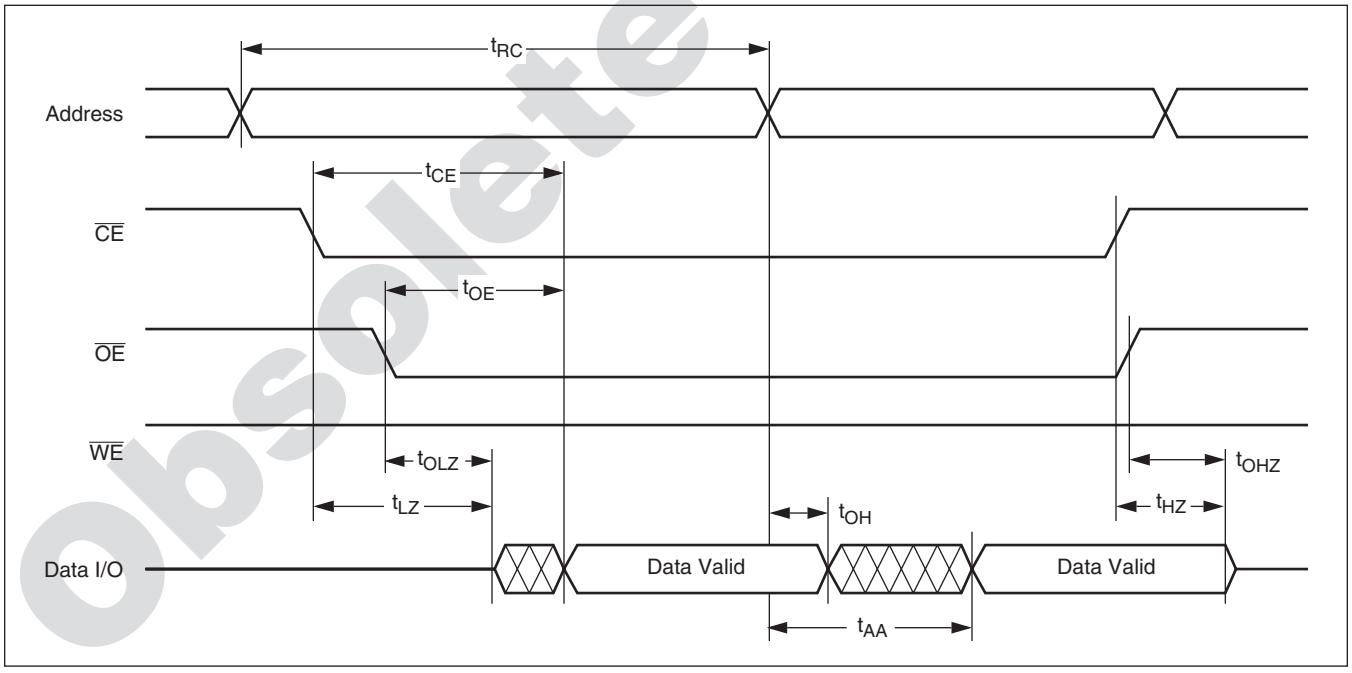
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C16-35 –40 to +85°C		X20C16-45		X20C16-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	35		45		55		ns
t_{CE}	Chip enable access time		35		45		55	ns
t_{AA}	Address access time		35		45		55	ns
t_{OE}	Output enable access time		20		25		30	ns
t_{LZ}(3)	Chip enable to output in low Z	0		0		0		ns
t_{OLZ}(3)	Output enable to output in low Z	0		0		0		ns
t_{HZ}(3)	Chip disable to output in high Z	0	15	0	20	0	25	ns
t_{OHZ}(3)	Output disable to output in high Z	0	15	0	20	0	25	ns
t_{OH}	Output hold from address change	0		0		0		ns

Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outptus are no longer driven.

Read Cycle

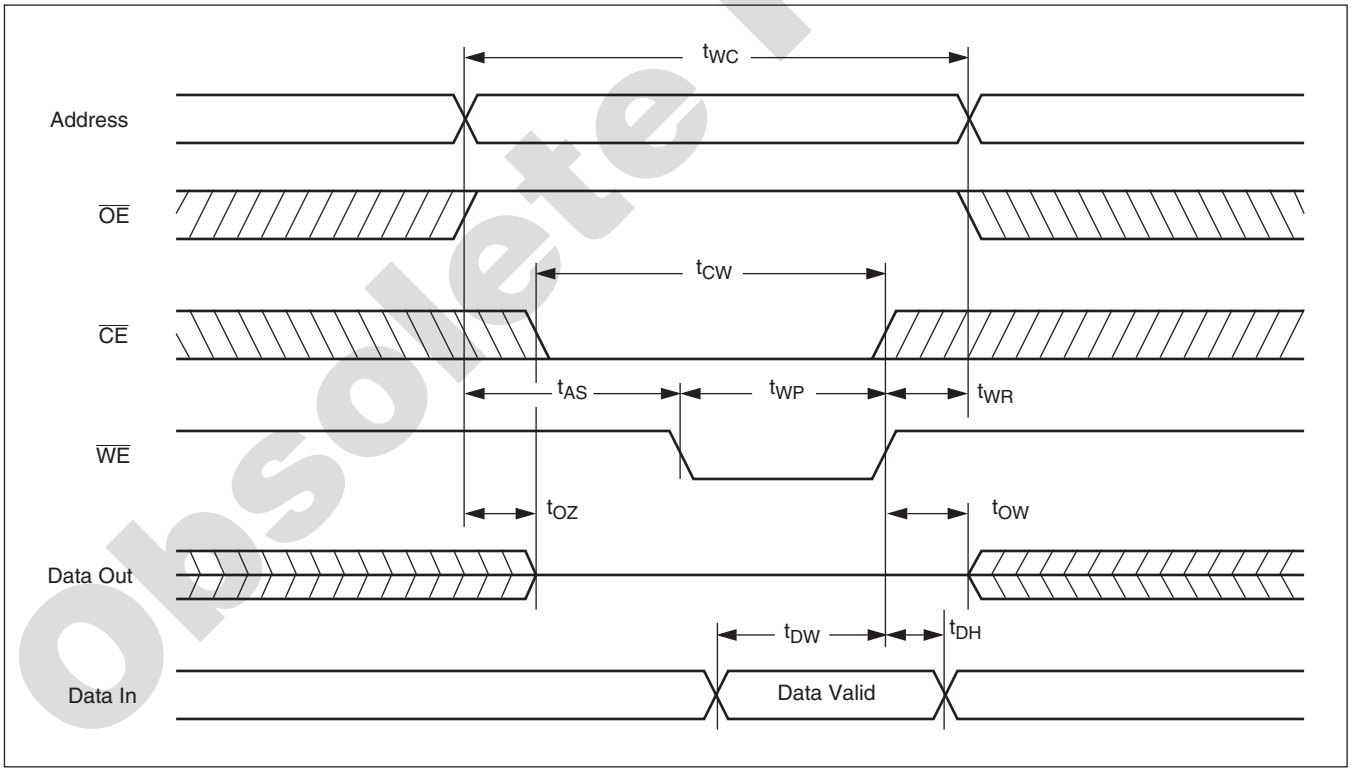


Write Cycle Limits

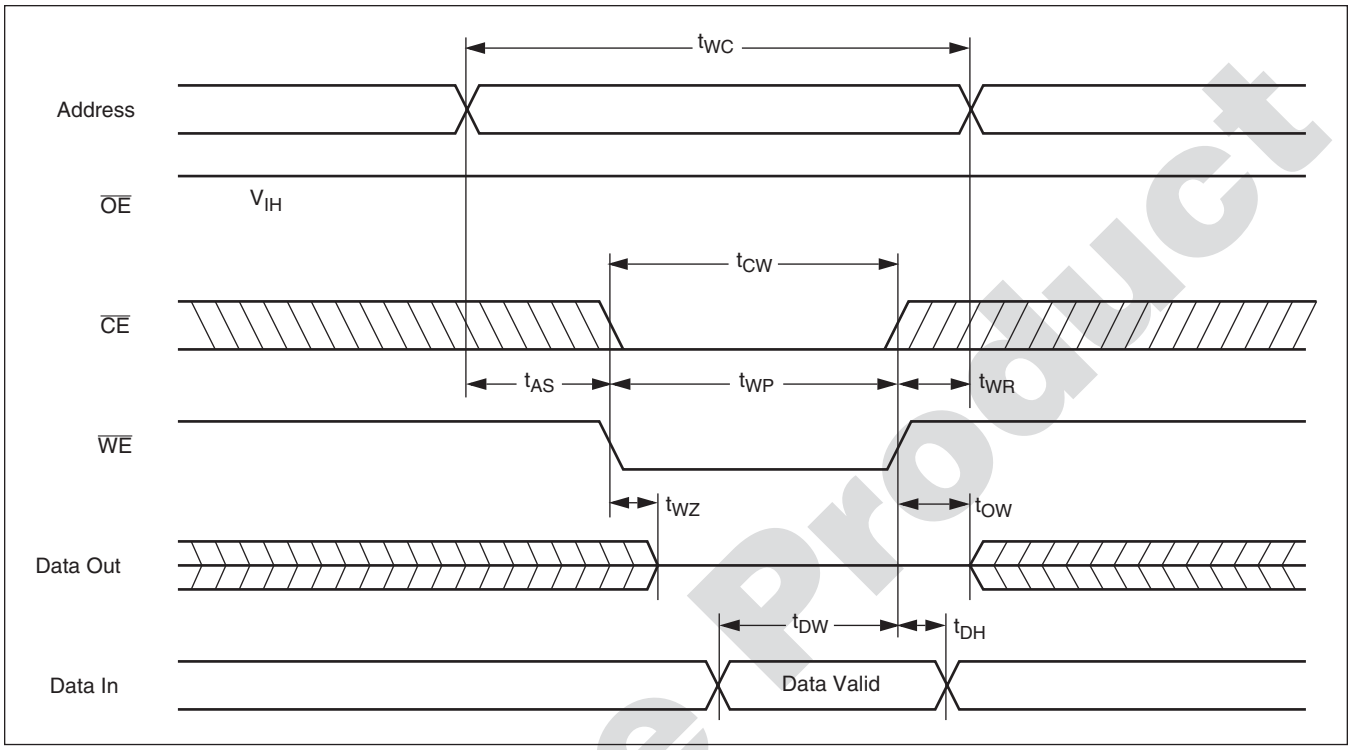
Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write cycle time	35		45		55		ns
t_{CW}	Chip enable to end of write input	30		35		40		ns
t_{AS}	Address setup time	0		0		0		ns
t_{WP}	Write pulse width	30		35		40		ns
t_{WR}	Write recovery time	0		0		0		ns
t_{DW}	Data setup to end of write	15		20		25		ns
t_{DH}	Data hold time	3		3		3		ns
$t_{WZ}^{(4)}$	Write Enable to output in high Z		15		20		25	ns
$t_{OW}^{(4)}$	Output active from end of write	5		5		5		ns
$t_{OZ}^{(4)}$	Output enable to output in high Z		15		20		25	ns

Note: (4) t_{WZ}, t_{OW}, t_{OZ} are periodically sampled and not 100% tested.

$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle

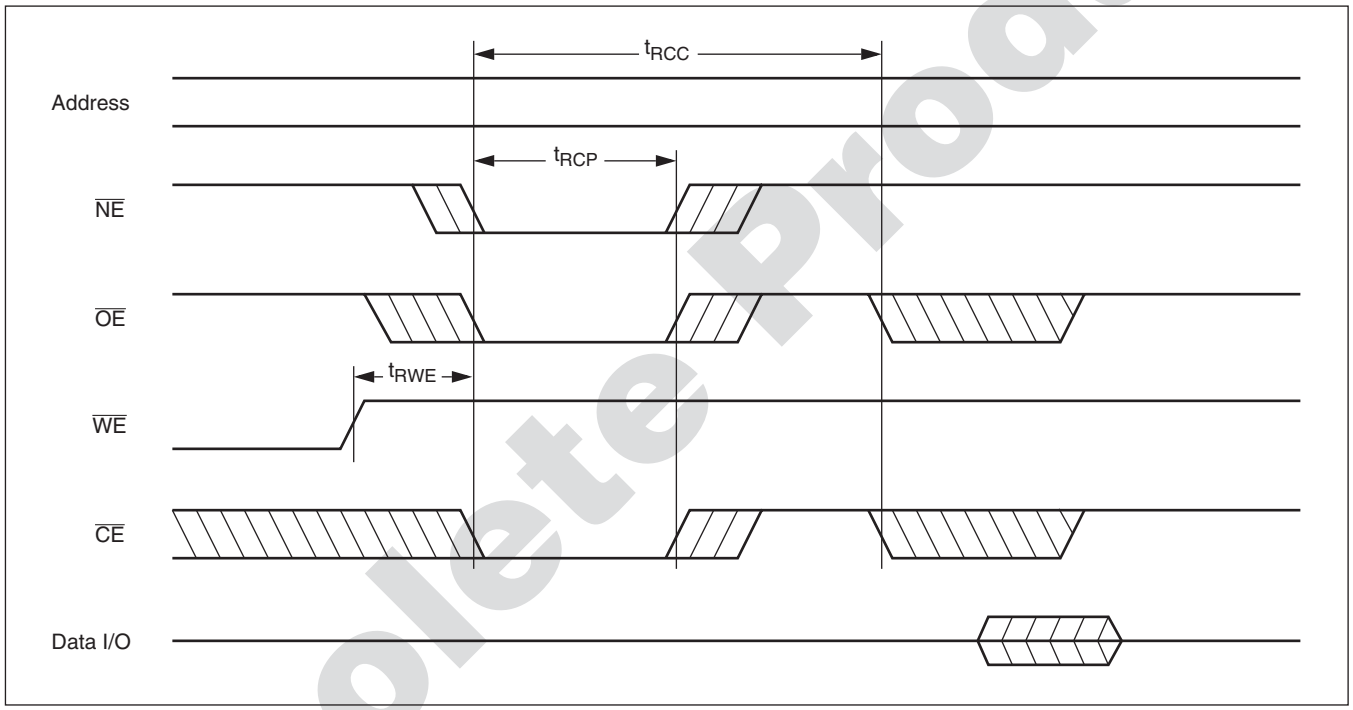


ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array recall cycle time		10		10		10	µs
t_{RCP}(5)	Recall pulse width to initiate recall	0.6	1000	40	1000	50	1000	ns
t_{RWE}	$\overline{WE}$ setup time to $\overline{NE}$	0		0		0		ns

Note: (5) The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously to insure data integrity, $\overline{NE}$ and $\overline{CE}$.

Array Recall Cycle

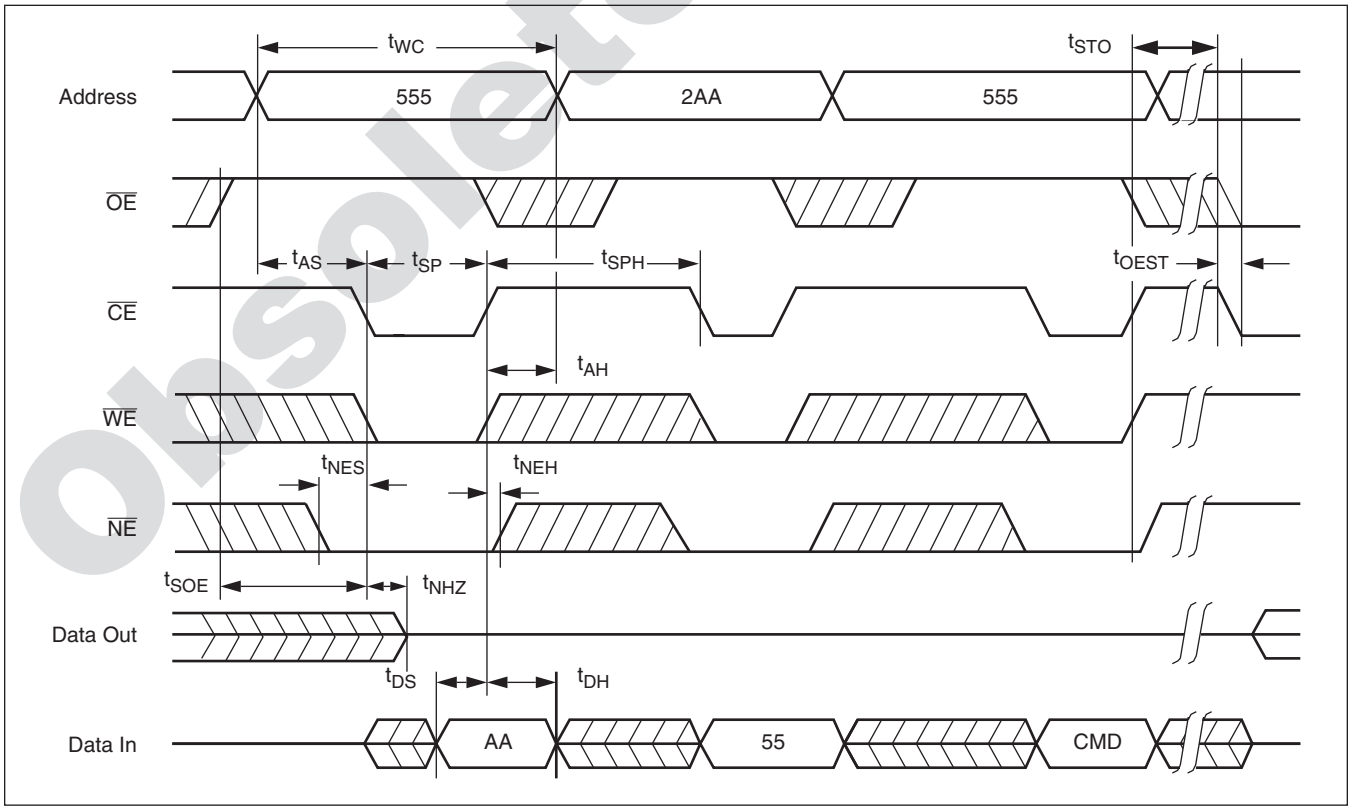


Software Command Timing Limits

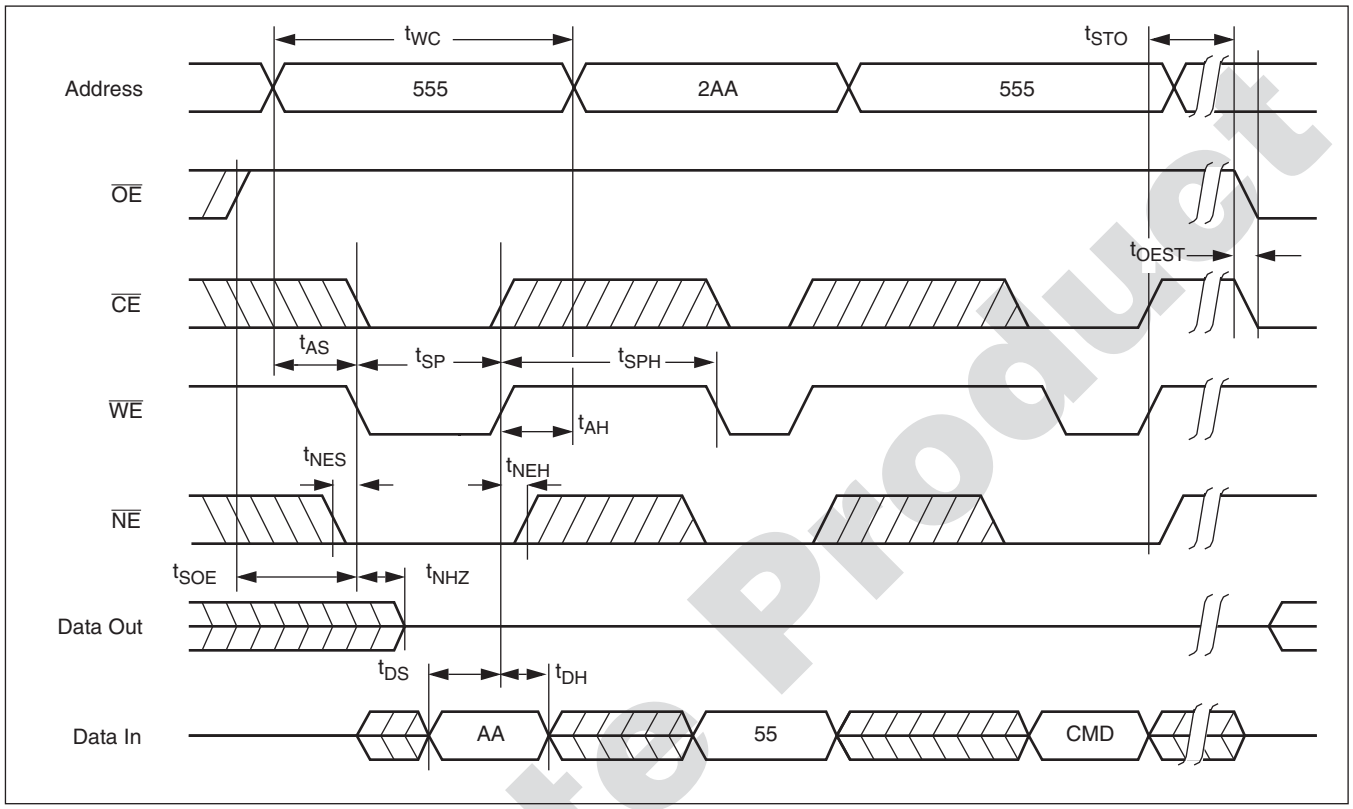
Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{STO}	Store cycle time		5		5		5	ms
t_{SP}[6]	Store pulse width	30		40		50		ns
t_{SPH}	Store pulse hold time	35		45		55		ns
t_{WC}	Write cycle time	35		45		55		ns
t_{AS}	Address setup time	0		0		0		ns
t_{AH}	Address hold time	0		0		0		ns
t_{DS}	Data setup time	15		20		25		ns
t_{DH}	Data hold time	3		3		3		ns
t_{SOE}[7]	$\overline{OE}$ disable to store function	20		20		20		ns
t_{OEST}[7]	Output enable from end of store	10		10		10		ns
t_{NHZ}[7]	Nonvolatile enable to output in high Z		15		20		25	ns
t_{NES}	$\overline{NE}$ setup time	5		5		5		ns
t_{NEH}	$\overline{NE}$ hold time	5		5		5		ns

Notes: (6) The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously.
(7) t_{SOE}, t_{OEST} and t_{NHZ} are periodically sampled and not 100% tested.

$\overline{CE}$ Controlled Software Command Sequence



$\overline{WE}$ Controlled Software Command Sequence

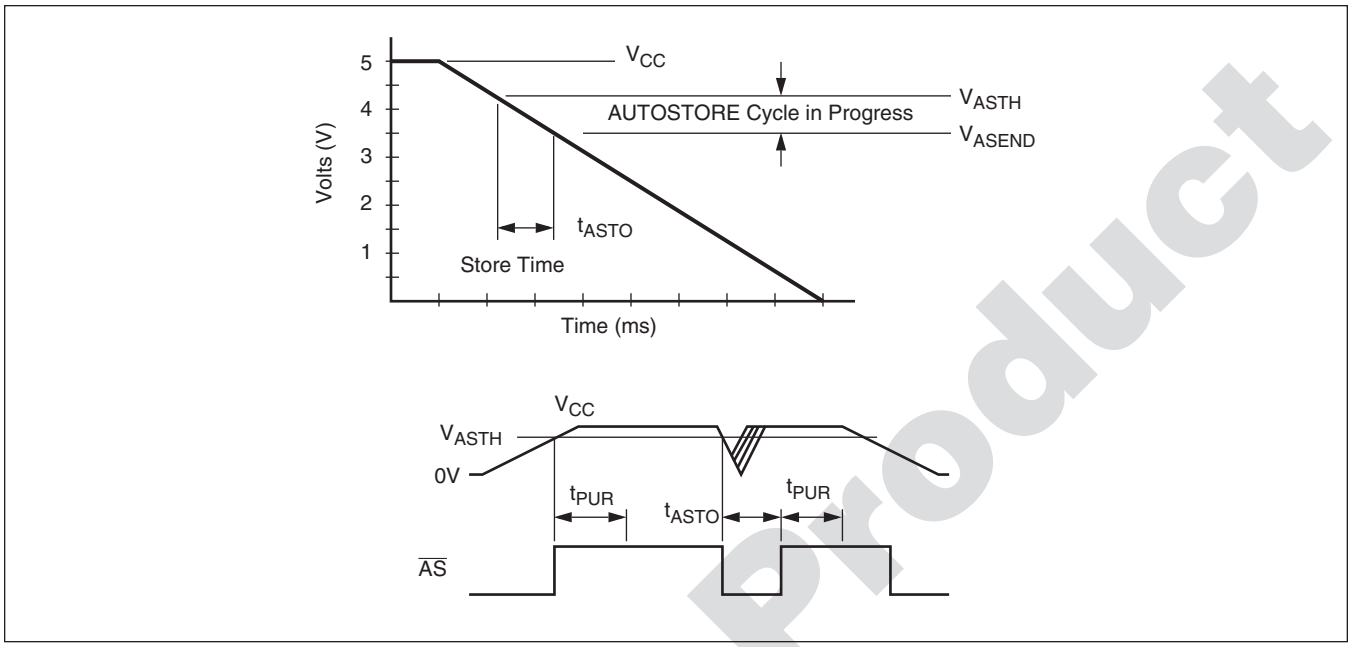


AUTOSTORE Feature

The AUTOSTORE feature automatically saves the contents of the X20C16's static RAM to the on-board bit-for-bit shadow EEPROM at power-down. This circuitry insures that no data is lost during accidental power-downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The AUTOSTORE instruction (EAS) to the SDP register sets the AUTOSTORE enable latch, allowing the X20C16 to automatically perform a store operation whenever V_{CC} falls below the AUTOSTORE threshold (V_{ASTH}). V_{CC} must remain above the AUTOSTORE Cycle End Voltage (V_{ASEND}) for the duration of the store cycle (t_{ASTO}). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagram, below. Once the AUTOSTORE cycle is initiated, all other device func-tions are inhibited.

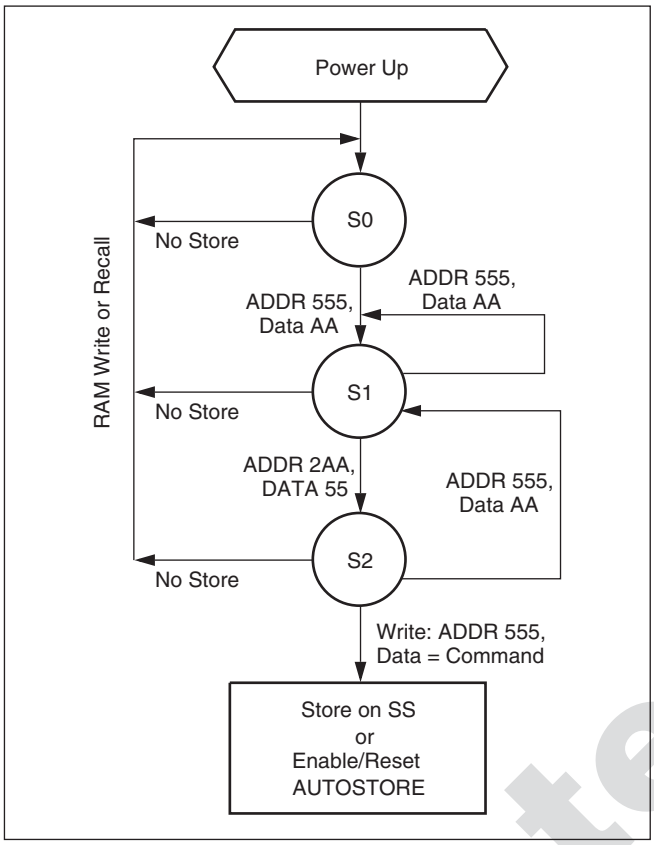
AUTOSTORE CYCLE Timing Diagrams



AUTOSTORE CYCLE LIMITS

Symbol	Parameter	X20C16		Unit
		Min.	Max.	
t_{ASTO}	AUTOSTORE cycle time		2.5	ms
V_{ASTH}	AUTOSTORE threshold voltage	4.0	4.3	V
V_{ASEND}	AUTOSTORE cycle end voltage	3.5		V

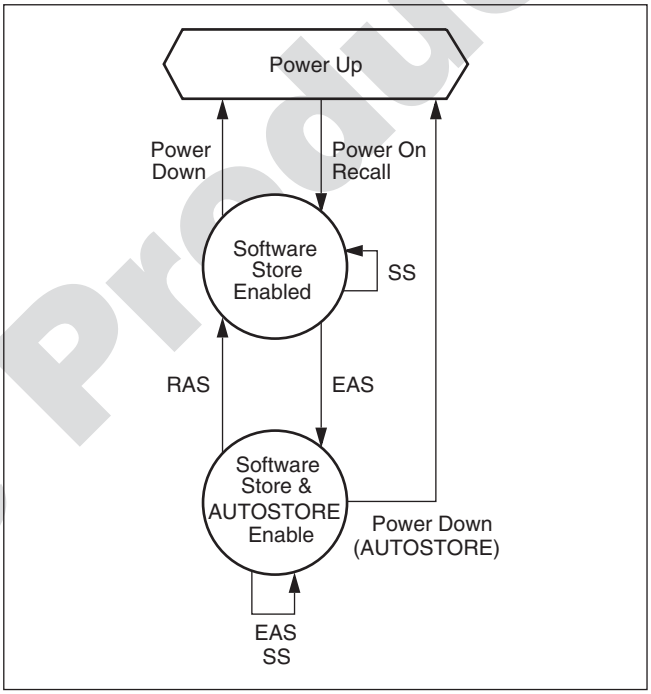
SDP (Software Data Protection)



SOFTWARE DATA PROTECTION COMMANDS

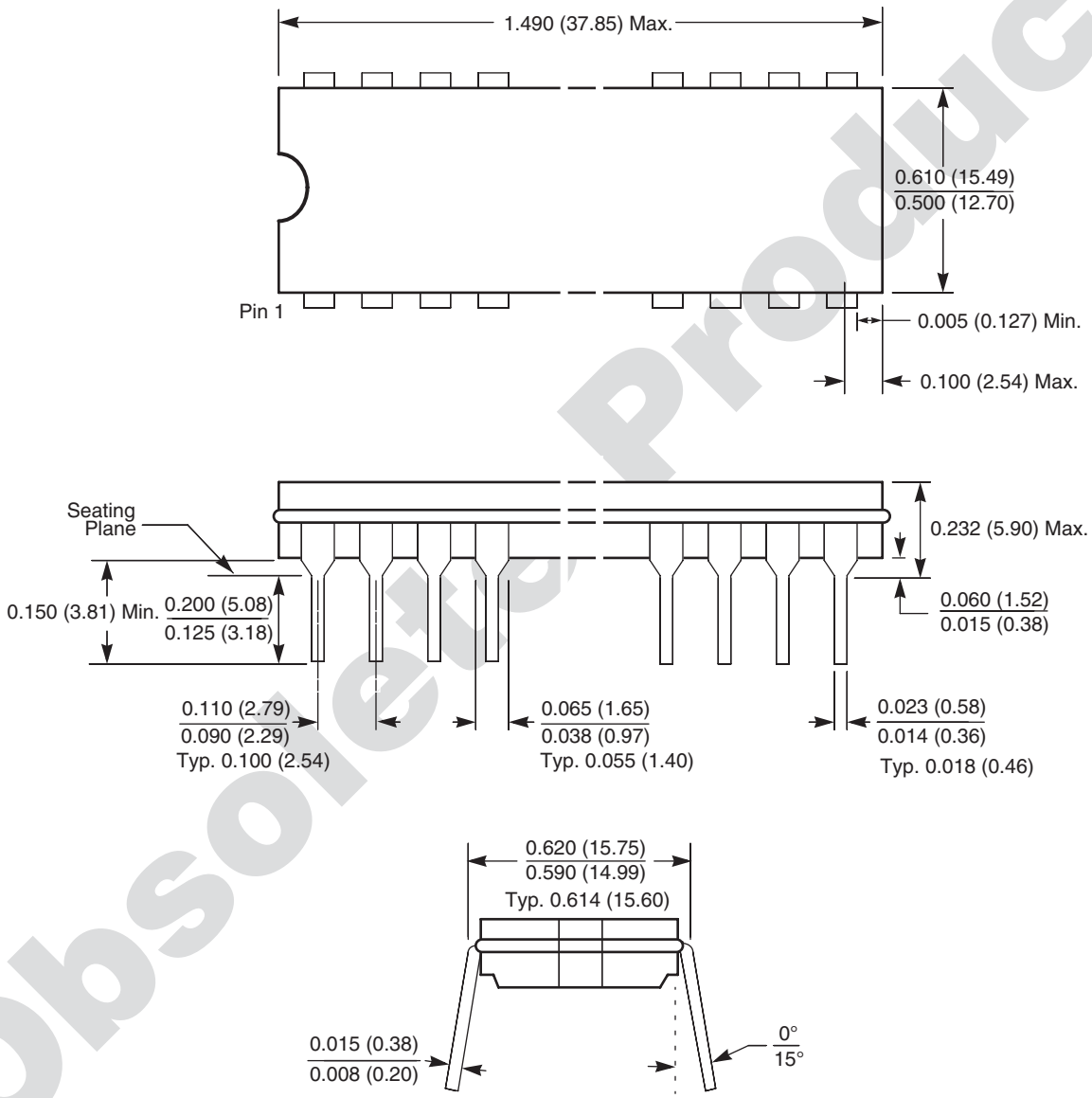
Command		Data
EAS	Enable AUTOSTORE	CC[H]
RAS	Reset AUTOSTORE	CD[H]
SS	Software Store	33[H]

Store State Diagram



PACKAGING INFORMATION

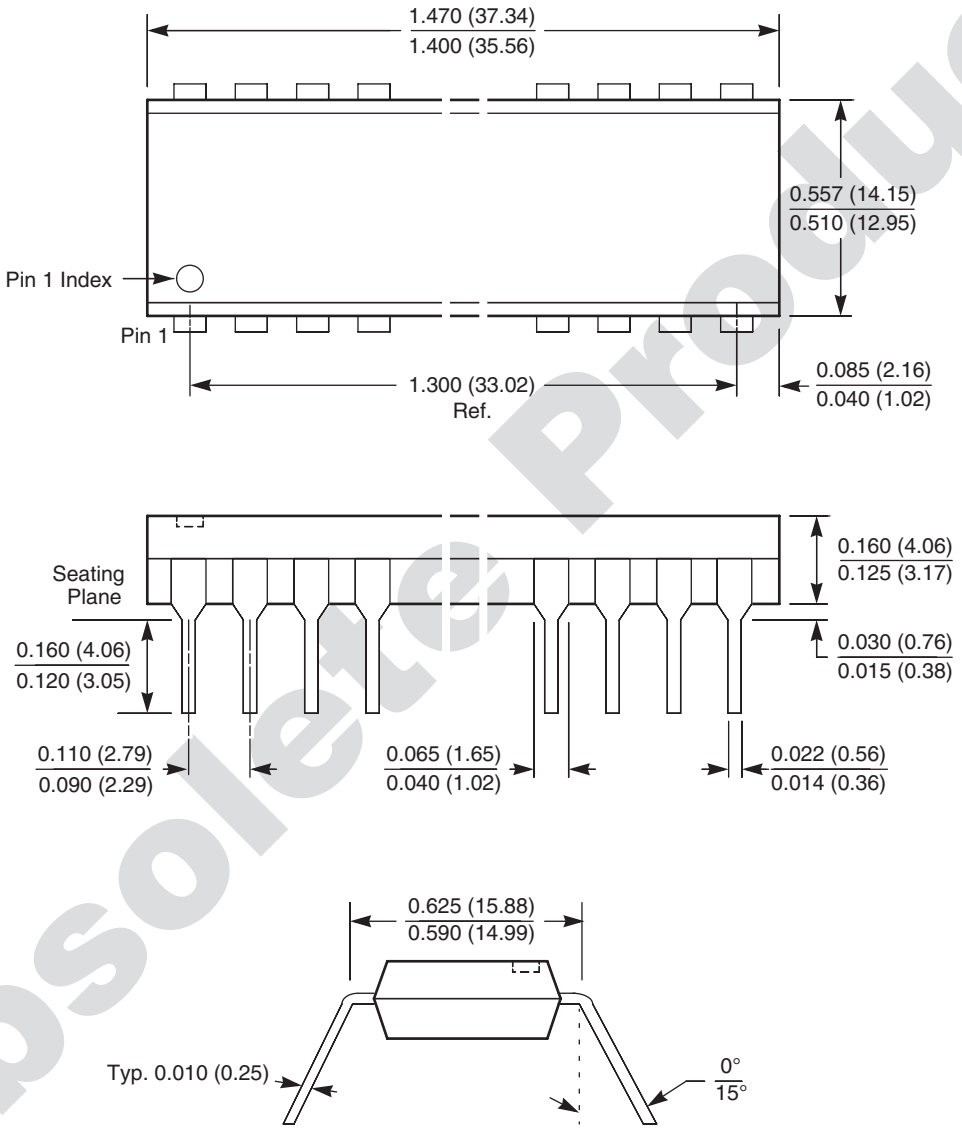
28-Lead Hermetic, CerDIP, Package Code D28



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

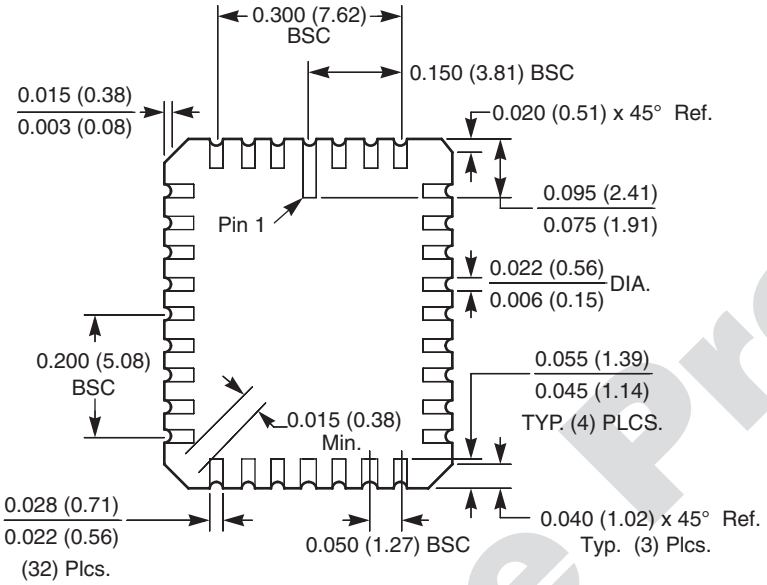
28-Lead Plastic, PDIP, Package Code P28

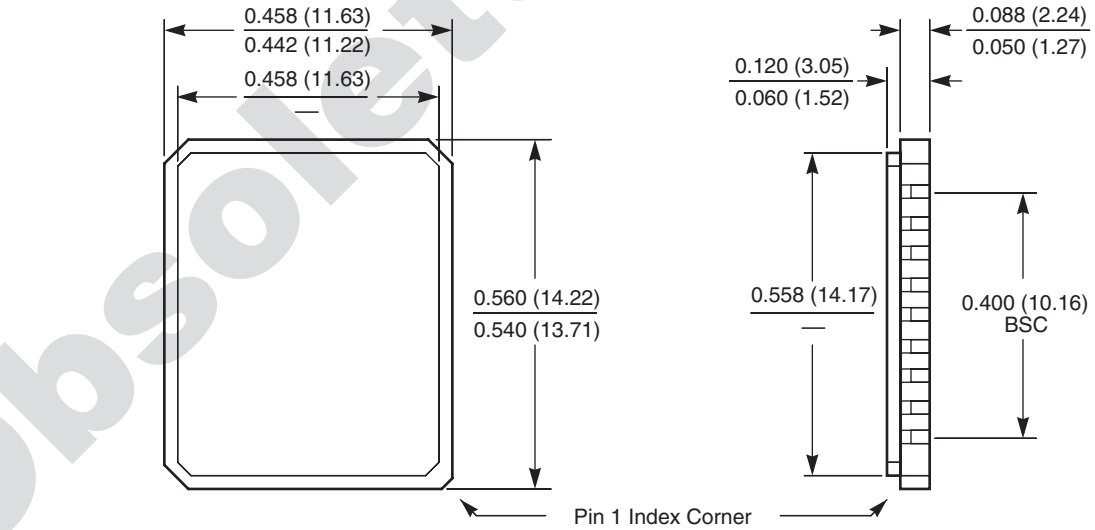


NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

PACKAGING INFROMATION

32-Pad Hermetic, LCC, Package Code E32

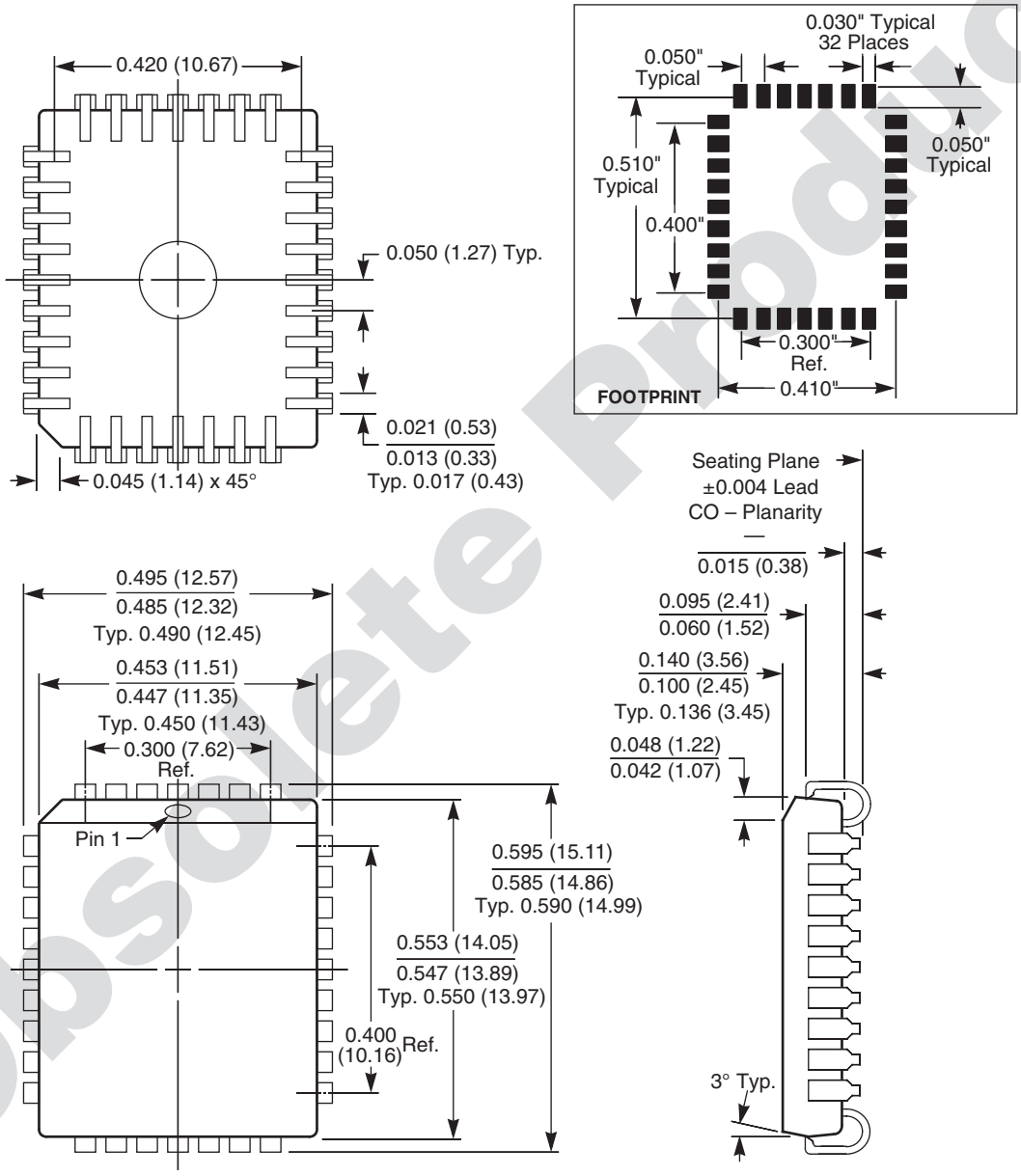




NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)

PACKAGING INFORMATION

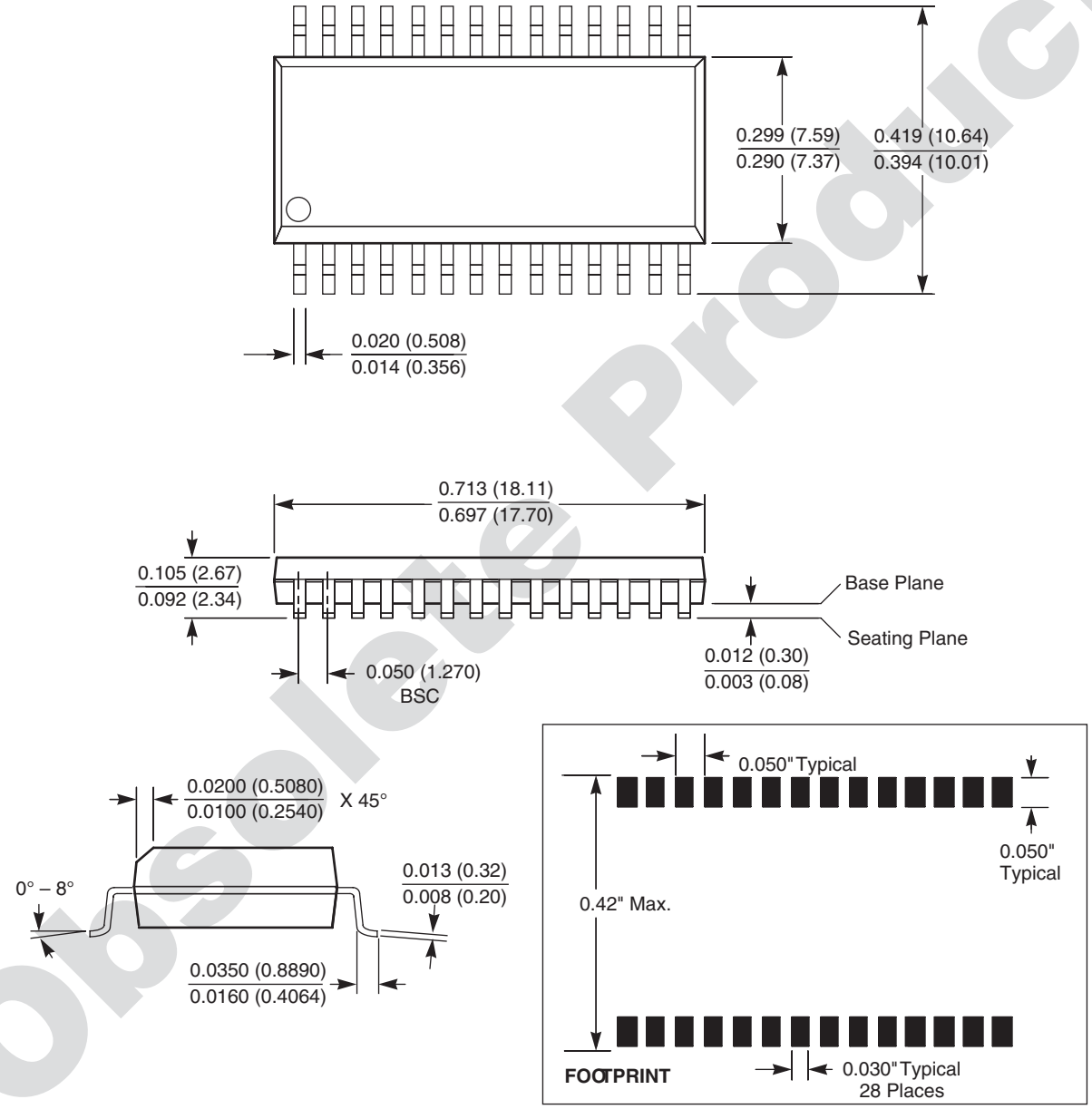
32-Lead Plastic, PLCC, Package Code J32



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

PACKAGING INFORMATION

28-Lead Plastic, SOIC, Package Code S28



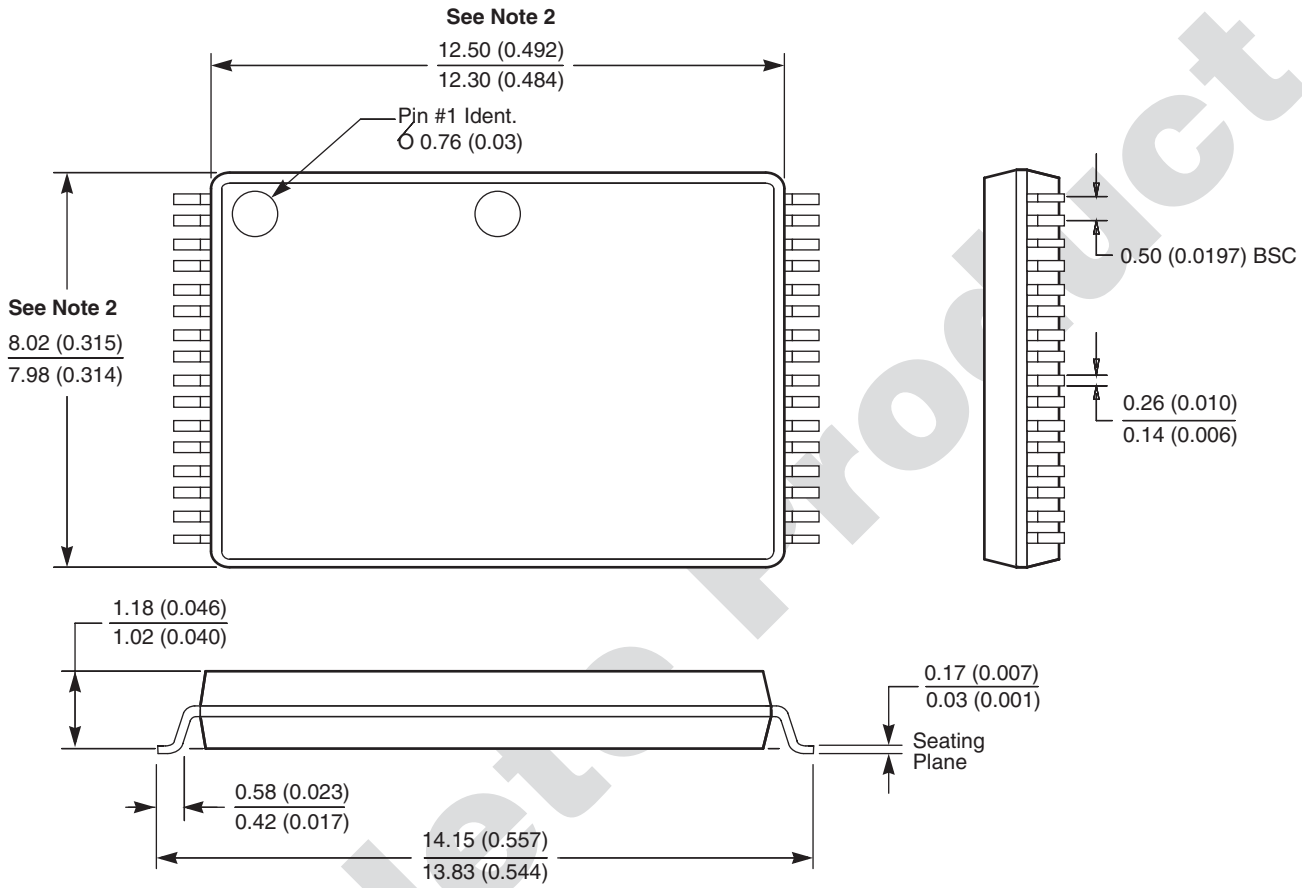
NOTES:

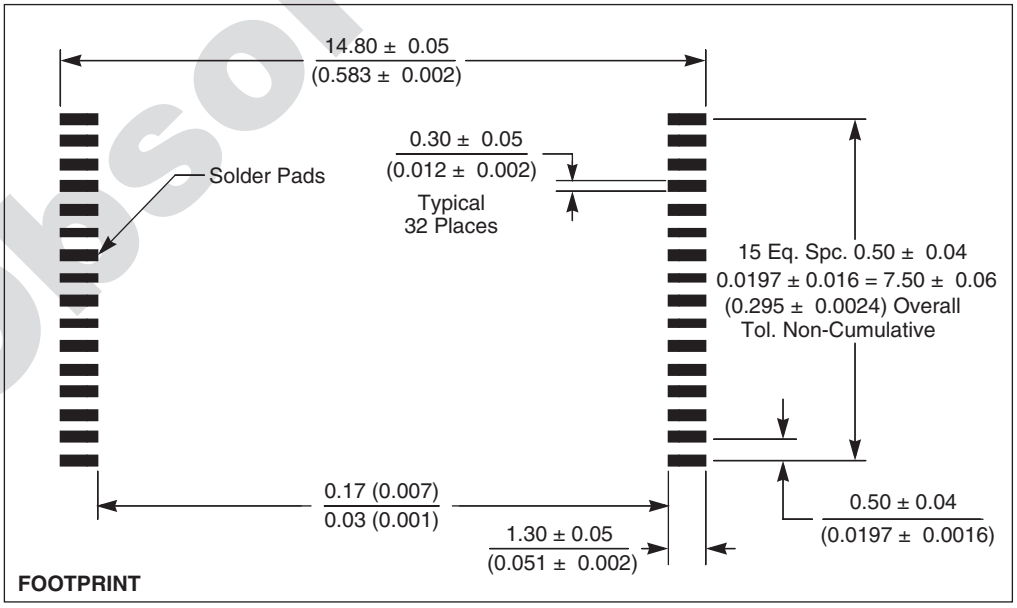
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

PACKAGING INFORMATION

32-Lead, TSOP, Package Code T32





NOTE:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).

Ordering Information