PRELIMINARY

Integrated Circuit Systems, Inc.

# ICS87952I

## LOW SKEW, 1-TO-11 LVCMOS / LVTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

## GENERAL DESCRIPTION

The ICS87952I is a low voltage, low skew LVCMOS/LVTTL clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. With output frequencies up to 180MHz, the ICS87952I is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS87952I contains frequency configurable outputs and an external feedback input for regenerating clocks with "zero delay".

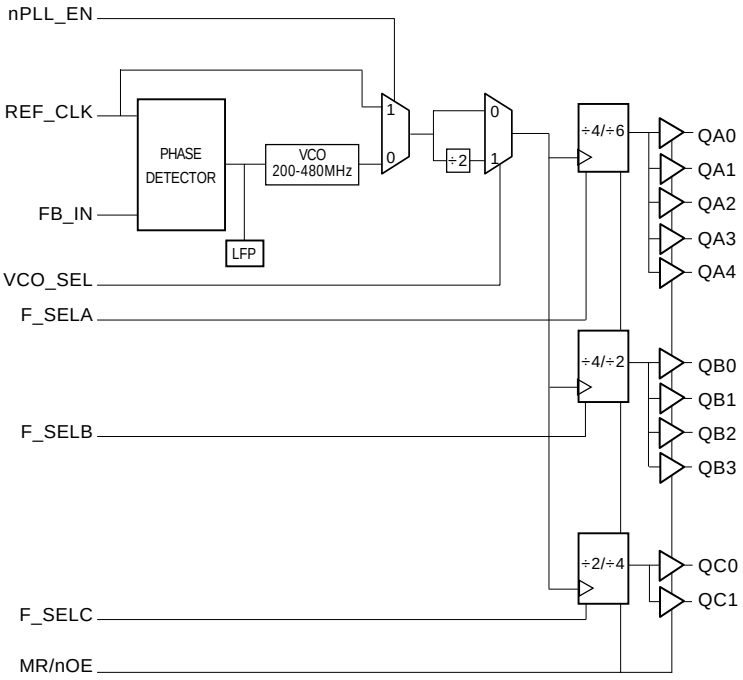
For test and system debug purposes, the nPLL_EN input allows the PLL to be bypassed. When HIGH, the MR/nOE input resets the internal dividers and forces the outputs to the high impedance state.

The low impedance LVCMOS/LVTTL outputs of the ICS87952I are designed to drive terminated transmission lines. The effective fanout of each output can be doubled by utilizing the ability of each output to drive two series terminated transmission lines.

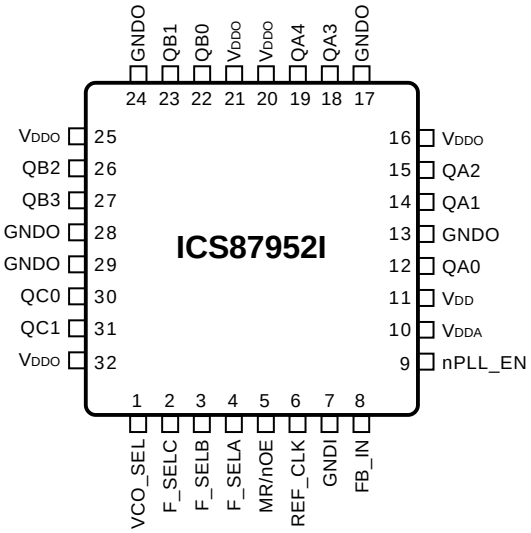
## FEATURES

- Fully integrated PLL
- 11 LVCMOS / LVTTL outputs, 7Ω typical output impedance
- LVCMOS / LVTTL REF_CLK input
- Output frequency range up to 180MHz at $V_{DD}$ = 3.3V ± 5%
- VCO range: 200MHz to 480MHz
- External feedback for "zero delay" clock regeneration
- Cycle-to-cycle jitter: 100ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Compatible with MPC952

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**32-Lead LQFP**
7mm x 7mm x 1.4mm package body
**Y package**
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | VCO_SEL | Input | Pulldown | VCO select input. |
| 2 | F_SELC | Input | Pulldown | Determines output divider values for Bank C as described in Table 3. LVCMOS / LVTTL interface levels. |
| 3 | F_SELB | Input | Pulldown | Determines output divider values for Bank B as described in Table 3. LVCMOS / LVTTL interface levels. |
| 4 | F_SELA | Input | Pulldown | Determines output divider values for Bank A as described in Table 3. LVCMOS / LVTTL interface levels. |
| 5 | MR/nOE | Input | Pulldown | Master Reset and output enable. When LOW, the output drivers are enabled. When HIGH, the output drivers are in HiZ and dividers are reset. LVCMOS / LVTTL interface levels. |
| 6 | REF_CLK | Input | Pulldown | Clock input. LVCMOS / LVTTL interface levels. |
| 7 | GNDI | Power | | Internal power supply ground. |
| 8 | FB_IN | Input | Pulldown | Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTL interface levels. |
| 9 | nPLL_EN | Input | Pulldown | PLL select input. Selects between REF_CLK and the PLL. When HIGH, selects REF_CLK. When LOW, selects PLL. LVCMOS / LVTTL interface levels. |
| 10 | $V_{DDA}$ | Power | | Analog supply pin. |
| 11 | $V_{DD}$ | Power | | Core supply pin. |
| 12, 14, 15, 18, 19 | QA0, QA1, QA2, QA3, QA4 | Output | | Bank A clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels. |
| 13, 17, 24, 28, 29 | GNDO | Power | | Output power supply ground. |
| 16, 20, 21, 25, 32 | $V_{DDO}$ | Power | | Output supply pins. |
| 22, 23, 26, 27 | QB0, QB1, QB2, QB3 | Output | | Bank B clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels. |
| 30, 31 | QC0, QC1 | Output | | Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels. |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 4 | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | KΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | KΩ |
| $C_{PD}$ | Power Dissipation Capacitance (per output) | $V_{DDA}$, $V_{DD}$, $V_{DDO}$ = 3.465V | | 25 | | pF |
| $R_{OUT}$ | Output Impedance | | | 7 | | Ω |

**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

| Input | Output | Input | Output | Input | Output |
|---|---|---|---|---|---|
| F_SELA | QA0:QA4 | F_SELB | QB0:QB3 | F_SELC | QC0:QC1 |
| 0 | ÷4 | 0 | ÷4 | 0 | ÷2 |
| 1 | ÷6 | 1 | ÷2 | 1 | ÷4 |

**TABLE 3B. CONTROL SELECT FUNCTION TABLE**

| Control Input | Logic 0 | Logic 1 |
|---|---|---|
| VCO_SEL | fVCO | fVCO/2 |
| MR/nOE | Output Enable | HiZ |
| nPLL_EN | Enable PLL | Disable PLL |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5 V |
| Outputs, $V_O$ | -0.5V to $V_{DDO}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Core Power Supply Current | | | | 160 | mA |
| $I_{DDA}$ | Analog Supply Current | | | 15 | 20 | mA |

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | VCO_SEL, nPLL_EN, FB_IN, F_SELA:F_SELC, MR/nOE | | -0.3 | | 0.8 | V |
| | | REF_CLK | | -0.3 | | 1.3 | V |
| $I_{IH}$ | Input High Current | REF_CLK, MR/nOE, FB_IN, VCO_SEL, F_SELA:F_SELC, nPLL_EN | $V_{DD} = V_{IN}$ = 3.465V | | | 120 | µA |
| $I_{IL}$ | Input Low Current | REF_CLK, MR/nOE, FB_IN, VCO_SEL, F_SELA:F_SELC, nPLL_EN | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -120 | | | µA |
| $V_{OH}$ | Output High Voltage | | $I_{OH}$ = -20mA | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | | $I_{OL}$ = 20mA | | | 0.5 | V |

**TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A$ = -40°C TO 85°C

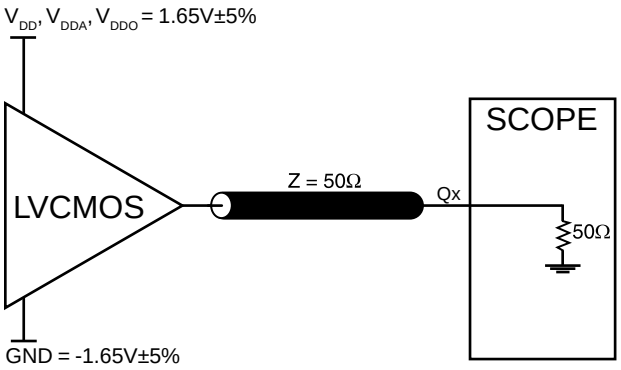
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{REF}$ | Input Reference Frequency<br>NOTE: Input reference frequency is limited by the divider selection and the VCO lock range. | | | | 100 | MHz |

**TABLE 6. AC CHARACTERISTICS,** $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A$ = -40°C TO 85°C

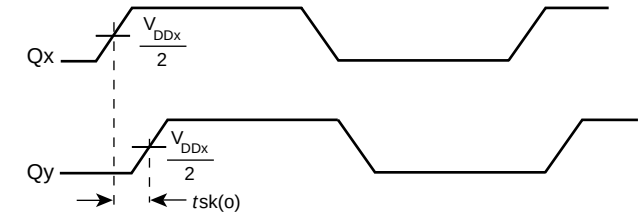
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Output Frequency (PLL Mode) | QC, QB (÷2) | | 180 | | | MHz |
| | | QA, QB, QC (÷4) | | 120 | | | MHz |
| | | QA (÷6) | | 80 | | | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | | | -200 | 0 | 200 | ps |
| $f_{VCO}$ | PLL VCO Lock Range | | | 200 | | 480 | MHz |
| *t*sk(o) | Output Skew; NOTE 2, 3 | Excluding QA0 | Same Frequency | | | 350 | ps |
| | | All Outputs | Same Frequency | | | 450 | ps |
| | | All Outputs | Different Frequency | | | 550 | ps |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 3 | | | | 100 | | ps |
| $t_L$ | PLL Lock Time | | | | 10 | | mS |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 0.8V to 2.0V | 0.10 | | 1.0 | ns |
| $t_{PW}$ | Output Pulse Width | | | $t_{Period}/2$ - 750 | $t_{Period}/2$ - 500 | $t_{Period}/2$ + 750 | ps |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | | | 2 | | 8 | ns |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | | | 2 | | 10 | ns |

All parameters measured at $f_{MAX}$ unless noted otherwise.
All outputs loaded at 50Ω to $V_{DDO}/2$.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

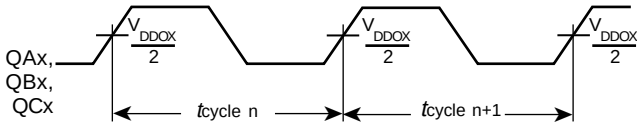
# PARAMETER MEASUREMENT INFORMATION




**3.3V OUTPUT LOAD AC TEST CIRCUIT**



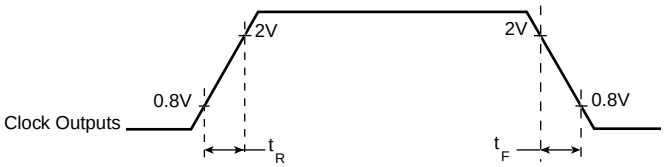

**OUTPUT SKEW**



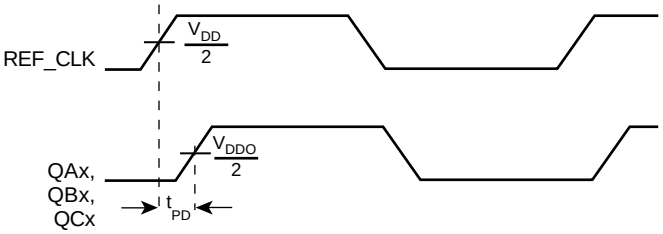

$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

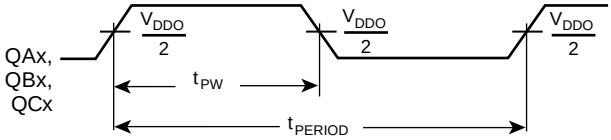
**CYCLE-TO-CYCLE JITTER**




**OUTPUT RISE/FALL TIME**




**PROPAGATION DELAY**




**$t_{PW}$ & $t_{PERIOD}$**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87952I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD}$, $V_{DDA}$ and $V_{DDO}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10mF and a .01mF bypass capacitor should be connected to each $V_{DDA}$ pin.

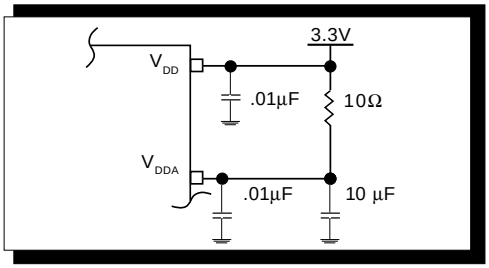



**FIGURE 1. POWER SUPPLY FILTERING**

# RELIABILITY INFORMATION

**TABLE 7. $\theta_{JA}$ VS. AIR FLOW TABLE**

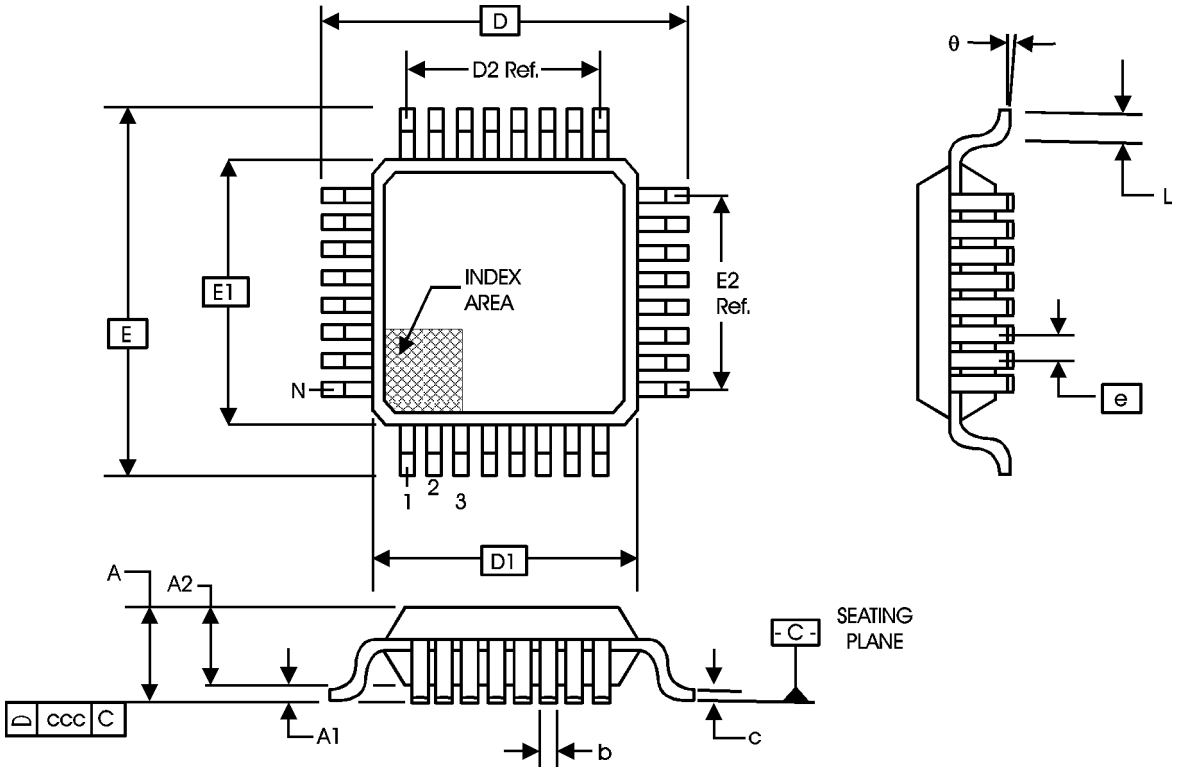
| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## TRANSISTOR COUNT

The transistor count for ICS87952I is: 2882

## PACKAGE OUTLINE - Y SUFFIX




### TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|---|---|---|---|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | | 32 | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | | 9.00 BASIC | |
| D1 | | 7.00 BASIC | |
| D2 | | 5.60 Ref. | |
| E | | 9.00 BASIC | |
| E1 | | 7.00 BASIC | |
| E2 | | 5.60 Ref. | |
| e | | 0.80 BASIC | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS87952AYI | ICS87952AYI | 32 Lead LQFP | 250 per tray | -40°C to 85°C |
| ICS87952AYIT | ICS87952AYI | 32 Lead LQFP on Tape and Reel | 1000 | -40°C to 85°C |